HardCopy® IV GX and HardCopy IV E Device Family Pin Connection Guidelines

Preliminary PCG-01009-1.0

The pin connection guidelines are considered preliminary. These pin connection guidelines should only be used as a recommendation, not as a specification. The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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HardCopy IV GX Pin Name	HardCopy IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins				
CLK[1,3,8,10]p	CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
CLK[1,3,8,10]n	CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
CLK[0,2,9,11]p	CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
CLK[0,2,9,11]n	CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
CLK[4:7, 12:15]p	CLK[4:7, 12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
CLK[4:7, 12:15]n	CLK[4:7, 12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[L1, L4, R1, R4]_CLKp	PLL_[L1, L4, R1, R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively. OCT Rd is not supported on these pins.	Connect unused pins to GND.
PLL_[L1, L4, R1, R4]_CLKn	PLL_[L1, L4, R1, R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively. OCT Rd is not supported on these pins.	Connect unused pins to GND.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[L1, L2, L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	PLL_[L1, L2, L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock		These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[T1, T2, B1, B2]_FBp/CLKOUT1	PLL_[T1, T2, B1, B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[T1, T2, B1, B2]_FBn/CLKOUT2	PLL_[T1, T2, B1, B2]_FBn/CLKOUT2	I/O, Clock		These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[T1, T2, B1, B2]_CLKOUT[3,4]	PLL_[T1, T2, B1, B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.

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HardCopy IV GX Pin Name	HardCopy IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
PLL_[T1, T2, B1, B2]_CLKOUT0p	PLL_[T1, T2, B1, B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
PLL_[T1, T2, B1, B2]_CLKOUT0n	PLL_[T1, T2, B1, B2]_CLKOUT0n	I/O, Clock		These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up resistor enabled, or as outputs driving GND.
Dedicated Configuration / JTAG Pins				
nIO_PULLUP	nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high turns off the weak pull-ups, while a logic low turns them on.	The nIO-PULLUP can be tied directly to VCCPGM, use a 1 KΩ pull-up resistor or tied directly to GND depending on the use desired for the device. The user I/O pins with internal pull-ups controlled by the nIO_PULLUP are nCSO, ASDO, DATA[7:0], CLKUSR, INIT_DONE, DEV_OE, and DEV_CLRn.
TEMPDIODEp	TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy IV device.	If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy IV device.	If the temperature sensing diode is not used then connect this pin to GND.
MSEL[0:2]	MSEL[0:2]	Input	Pins are configuration inputs for Stratix IV FPGA only, they set the FPGA prototype configuration scheme. MSEL[0:2] are NC (No Connection) pins for HardCopy IV devices, but they preserve the pin assignment and direction from the Stratix IV prototype, allowing drop-in replacement.	The connection to the board on these pins are "don't care" for HardCopy IV. In the prototype stage using the Stratix IV these pins are internally connected through a 5-KΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used these pins should be tied to VCCPGM or GND. Refer to the "Configuring Stratix IV Devices" chapter in the Stratix IV Handbook. If only JTAG configuration is used, connect these pins to GND. See Note 15.
nCE	nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	If multi-devices are on a board, the configuration data stored in the FPGA device must be updated to exclude the configuration data for the HardCopy device. The nCE pin of the HardCopy IV device must be connected to GND. The nCE pin of the FPGA that was driven by the HardCopy IV nCEO pin must now be driven by the nCEO pin of the FPGA that precedes the HardCopy IV device in the chain. In single HardCopy device, nCE pin must be connected to GND. In the prototype stage using the Stratix IV in a multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. However, in single device configuration and JTAG programming, nCE should be connected to GND. See Note 15.
nCONFIG	nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy IV to enter a reset state and tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.	For HardCopy IV devices, the nCONFIG pin is designed with weak internal resistor pulled up to VCCPGM. The board can be designed to have additional switching capability to this pin to allow pulsing the nCONFIG in order to restart the HardCopy IV device. In the prototype stage using the Stratix IV nCONFIG should be connected directly to the configuration controller when the FPGA uses a passive configuration scheme, or through a 10-KΩ resistor tied to VCCPGM when using an active serial configuration scheme. If this pin is not used, it requires a connection directly or through a 10-KΩ resistor to VCCPGM. See Note 15.
CONF_DONE	CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. When this pin is driven high it indicates that the device is entering user mode.	For HardCopy IV devices, the CONF_DONE pin is designed with weak internal resistor pulled up to VCCPGM. In the prototype stage using the Stratix IV when internal pull-up resistors on the configuration controller or enhanced configuration device are used, external 10-KΩ pull-up resistors should not be used on this pin. Otherwise an external 10-KΩ pull-up resistor to VCCPGM should be used. When using Passive configuration schemes this pin should also be monitored by the configuration controller. See Note 15.

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HardCopy IV GX Pin Name	HardCopy IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
nCEO	nCEO	Output	Output that drives low when device configuration is complete.	nCEO is left floating for HardCopy IV devices. In the prototype stage using the Stratix IV with multi-device configuration, this pin feeds the nCE pin of a subsequent device. During single device configuration, leave this pin unconnected. See Note 15.
nSTATUS	nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. When the HardCopy IV device drives nSTATUS low, it indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.	For HardCopy IV devices, nSTATUS pin is designed with weak internal resistor pulled up to VCCPGM. In the prototype stage using the Stratix IV if internal pull-up resistors on the enhanced configuration device are used, external 10-KΩ pull-up should not be used on these pins. Otherwise, an external 10-KΩ pull-up resistors to VCCPGM should be used. When using Passive configuration schemes this pin should also be monitored by the configuration controller. See Note 15.
PORSEL	PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.	The PORSEL pin should be tied directly to VCCPGM or GND.
TCK	TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-KΩ pull-down resistor to GND.
TMS	TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 10-KΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TMS to VCCPD via a 1-KΩ resistor.
TDI	TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 10-KΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TDI to VCCPD via a 1-KΩ resistor.
TDO	TDO	Output	Dedicated JTAG test data output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected.
TRST	TRST	Input	Dedicated active low JTAG test reset input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.	Utilization of TRST is optional. When using this pin ensure that TMS is held high or TCK is static when TRST is changed from low to high. If not using TRST, tie this pin to a 1-KΩ pull-up resistor to VCCPD. To disable the JTAG circuitry, tie this pin to GND.
Optional/Dual Purpose Configuration Pins				
nCSO	nCSO	Output	Dedicated control signal from the Stratix IV device to the serial configuration device in AS mode that enables the configuration device. This pin is kept in HardCopy IV for compatibility reasons.	When this pin is not used as an output then it is recommended to leave the pin unconnected. If Erasable Programmable Configuration Serial (EPCS) is used in user mode as a boot-up RAM or data access for a Nios II processor, DCLK, DATA[0], ASDO, and nCSO need to be connected to the EPCS device.
ASDO	ASDO	Output	Dedicated control signal from the Stratix IV device to the serial configuration device in AS mode used to read out configuration data. This pin is kept in HardCopy IV for compatibility reasons.	When this pin is not used as an output then it is recommended to leave the pin unconnected. If Erasable Programmable Configuration Serial (EPCS) is used in user mode as a boot-up RAM or data access for a Nios II processor, DCLK, DATA[0], ASDO, and nCSO need to be connected to the EPCS device.
DCLK	DCLK	Input(PS, FPP) Output (AS)	Dedicated configuration clock pin on the Stratix IV device. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface. This pin is kept in HardCopy IV for compatibility reasons.	For HardCopy IV leave this pin unconnected. If Erasable Programmable Configuration Serial (EPCS) is used in user mode as a boot-up RAM or data access for a Nios II processor, DCLK, DATA[0], ASDO, and nCSO need to be connected to the EPCS device. In the prototype stage using the Stratix IV do not leave this pin floating. Drive this pin ether high or low. See Note 15.

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HardCopy IV GX Pin Name	HardCopy IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
CRC_ERROR	CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits on the Stratix IV device. This pin is optional and is used when the CRC error detection circuit is enabled in the Stratix IV FPGA.	For HardCopy IV, the pin retains the same I/O functions from Stratix IV prototype, but not CRC_ERROR because no device programming is needed. See Note 10. In the prototype stage using the Stratix IV connect this pin to an external 10-KΩ pull-up resistor to VCCPGM. See Note 15.
DEV_CLRn	DEV_CLRn	I/O, Input	Optional pin for Stratix IV FPGA that allows designers to override all clears on all device registers. In this case, when this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.	For HardCopy IV, this pin is an I/O function only. See Note 10. In the prototype stage using the Stratix IV when DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground. See Note 15.
DEV_OE	DEV_OE	I/O, Input	Optional pin for Stratix IV FPGA that allows designers to override all tri-states on the device. In this case, when the pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.	For HardCopy IV, this pin is an I/O function only. See Note 10. In the prototype stage using the Stratix IV when DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground. See Note 15.
DATA[0]	DATA[0]	I/O, Input	Dual-purpose configuration data input pin for Stratix IV FPGA. In this case, the DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.	When this pin is not used as an output then it is recommended to leave the pin unconnected. If Erasable Programmable Configuration Serial (EPCS) is used in user mode as a boot-up RAM or data access for a Nios II processor, DCLK, DATA[0], ASDO, and nCSO need to be connected to the EPCS device. SeeNote 10. In the prototype stage using the Stratix IV when DATA0 is not used and this pin is not used as an I/O then it is recommended to leave this pin unconnected. See Note 15.
DATA[1:7]	DATA[1:7]	I/O, Input	Dual-purpose configuration data input pin for Stratix IV FPGA. In this case the DATA[0:7] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	For HardCopy IV, these pins are I/O functions only. See Note 10. In the prototype stage using the Stratix IV when DATA[1:7] is not used and this pin is not used as an I/O then it is recommended to leave these pins unconnected. See Note 15.
INIT_DONE	INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE in Stratix IV FPGA. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	For HardCopy IV, this pin is an I/O function only. See Note 10. In the prototype stage using the Stratix IV connect this pin to an external 10-KΩ pull-up resistor to VCCPGM. See Note 15.
CLKUSR	CLKUSR	I/O, Input	Optional user-supplied clock input in Stratix IV FPGA. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	For HardCopy IV, this pin is an I/O function only. See Note 10. In the prototype stage using the Stratix IV if the CLKUSR is not used as a configuration clock input and this pin is not used as an I/O then it is recommended to leave this pin to GND. See Note 15.

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HardCopy IV GX Pin Name	HardCopy IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Differential I/O Pins				
DIFFIO_RX[##]p, DIFFIO_RX[##]n	DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.
DIFFOUT_[##]p, DIFFOUT_[##]n	DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with a "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in Quartus II software.
External Memory Interface Pins				
DQS[1:38][T,B], DQS[1:34][L,R]	DQS[1:38][T,B], DQS[1:34][L,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in Quartus II software.
DQSn[1:38][T,B], DQSn[1:34][L,R]	DQSn[1:38][T,B], DQSn[1:34][L,R]	I/O, DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in Quartus II software.
DQ[1:38][T,B], DQ[1:34][L,R]	DQ[1:38][T,B], DQ[1:34][L,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in Quartus II software.
CQ[1:38][T,B], CQ[1:34][L,R]	CQ[1:38][T,B], CQ[1:34][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.	Connect unused pins as defined in Quartus II software.

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CQn[1:38][T,B], CQn[1:34][L,R]	CQn[1:38][T,B], CQn[1:34][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.	Connect unused pins as defined in Quartus II software.
Reference Pins				
RUP[1:8]A, RUP[3:8]C	RUP[1:8]A, RUP[3:8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to the VCCIO of the bank in which the RUP pin resides or GND. When using OCT tie these pins to the required banks VCCIO through either a 25 Ω or 50 Ω resistor, depending on the desired I/O standard. Refer to the HardCopy IV handbook for the desired resistor value for the I/O standard used.
RDN[1:8]A, RDN[3:8]C	RDN[1:8]A, RDN[3:8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to GND. When using OCT tie these pins to GND through either a 25 Ω or 50 Ω resistor depending on the desired I/O standard. Refer to the HardCopy IV handbook for the desired resistor value for the I/O standard used.
DNU	DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, ground or any other signal. These pins must be left floating.
NC	NC	No Connect	Do not drive signals into these pins.	When designing for device migration these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.
Supply Pins ***(See Notes 12 and 13)***				
VCC	VCC	Power	VCC supplies power to the core and periphery.	All VCC pins require a 0.9 V supply. Use the HardCopy IV Early Power Estimator to determine the current requirements for VCC and other power supplies. These pins may be tied to the same 0.9 V plane as VCCHIP. With a proper isolation filter VCCD_PLL may be sourced from the same regulator as VCC. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 4 ,9, and 13.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]].	You are required to connect these pins to 0.9 V, even if the PLL is not used. With a proper isolation filter these pins may be sourced from the same regulator as VCC and/or VCCHIP. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 4 and 9.
VCCPT	VCCPT	Power	Power supply for the programmable power technology in the Stratix IV FPGA. VCCPT is a NC (No Connection) pin of HardCopy IV devices.	The connection to the board on this pin is a "don't care" for HardCopy IV. In the prototype stage using the Stratix IV VCCPT can be connected to a 1.5 V linear or low noise switching power supply. When VCCPT is sourced from a regulator that is shared with other voltage rails, VCCPT must be isolated from the other voltage rails. For data rates ≤ 6.5 Gbps where VCCH_GXB requires 1.5 V the VCCPT supply may be sourced from the same regulator as VCCH_GXB with the use of a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 4, 9, 11, 14, and 15.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. It is advised to keep this pin isolated from other VCC for better jitter performance.	You are required to connect these pins to 2.5 V, even if the PLL is not used. Use an isolated linear or low noise switching power supply. With a proper isolation filter these pins may be sourced from the same linear regulator as VCCAUX. For data rates ≤ 4.25 Gbps where VCCA_[L,R] is 2.5 V these pins may also be tied to the same regulator as VCCA_[L,R] with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 4, 9, 11, and 14.

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Preliminary PCG-01009-1.0

You should create a Quartus II design, enter your device I/O assignments and compile the design. The Quartus II software will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

HardCopy IV GX Pin Name	HardCopy IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCAUX	VCCAUX	Power	Auxiliary supply for the programmable power technology.	Connect these pins to an isolated 2.5 V linear or low noise switching power supply. With a proper isolation filter these pins may be sourced from the same linear regulator as VCCA_PLL. For data rates ≤ 4.25 Gbps where VCCA_[L,R] is 2.5 V these pins may also be tied to the same linear regulator as VCCA_[L,R] with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 4, 9, 11, and 14.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	VCCIO[1:8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTL 3.3 V I/O standards.	Connect these pin to 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.0 V supplies, depending on the I/O standard connected to the specified bank. When these pins require 2.5 V they may be tied to the same regulator as VCC_CLKIN, VCCPGM, and VCCPD, but only if each of these supplies require 2.5 V sources. VCC_CLKIN has a set voltage of 2.5 V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPGM and/or VCCPD as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 4 and 9.
VCCPGM	VCCPGM	Power	Configuration pins power supply.	Connect this pin to either 1.8 V, 2.5 V, or 3.0 V power supply. When these pins require 2.5 V they may be tied to the same regulator as VCC_CLKIN, VCCIO and VCCPD, but only if each of these supplies require 2.5 V sources. VCC_CLKIN has a set voltage of 2.5 V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPD and/or VCCIO as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 4 and 9.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	VCCPD[1:8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 3.0 V or 2.5 V. For 3.3 V or 3.0 V I/O standard connect VCCPD to 3.0 V, and for 1.2 V, 1.5 V, 1.8 V, or 2.5V I/O standards connect VCCPD to 2.5V.	The VCCPD pins require 2.5 V or 3.0 V and must ramp-up from 0 V to 2.5 V or 3.0 V within 100 ms to ensure successful configuration. When these pins require 2.5 V they may be tied to the same regulator as VCC_CLKIN, VCCPGM, and VCCIO, but only if each of these supplies require 2.5 V sources. VCC_CLKIN has a set voltage of 2.5 V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPGM and/or VCCIO as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 4 and 9.
VCC_CLKIN[3,4,7,8]C	VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.	Connect these pins to 2.5 V power source. These pins may be tied to the same regulator as VCCIO, VCCPGM and VCCPD, but only if each of these supplies require 2.5 V sources. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 4.
VCCBAT	VCCBAT	Power	Battery back-up power supply for design security volatile key register for Stratix IV FPGA only. VCCBAT is a NC (No Connection) pin of HardCopy IV devices.	The connection to the board on this pin is a "don't care" for the HardCopy IV. In the prototype stage using the Stratix IV when not using the volatile key, tie this to a 3.0 V supply or GND. Do not share this source with other FPGA power supplies. See Note 15.
GND	GND	Ground	Device ground pins.	All GND pins should be connected to the board ground plane.
VREF[1:8][A,C], VREF[2,3,4,5,7,8]B	VREF[1:8][A,B,C]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.	If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 4.
Transceiver Pins ***(See Notes 12 through 14)***				
VCCHIP_[L,R]	NA	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.	All VCCHIP_[L,R] pins require a 0.9 V supply. When not using HIP these pins may be connected to GND. These pins may be tied to the same 0.9 V plane as VCC. With a proper isolation filter these pins may be sourced from the same regulator as VCCD_PLL. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 4 and 9.

You should create a Quartus II design, enter your device I/O assignments and compile the design. The Quartus II software will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

HardCopy IV GX Pin Name	HardCopy IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCR_[L,R]	NA	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.	Connect VCCR_[L,R] to a 1.1 V linear or low noise switching regulator. VCCR_L pins must be tied to the same linear regulator as VCCT_L. Also, VCCR_R pins must be tied to the same linear regulator as VCCT_R. For data rates ≤ 6.5 Gbps these pins may be tied to the same 1.1 V plane as VCCL_GXB[L,R]. However, for better jitter performance at high data rates this plane should be isolated from all other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 4, 8, 9, 11, and 14.
VCCT_[L,R]	NA	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.	Connect VCCT_[L,R] to a 1.1 V linear or low noise switching regulator. VCCR_L pins must be tied to the same linear regulator as VCCT_L. Also, VCCR_R pins must be tied to the same linear regulator as VCCT_R. For data rates ≤ 6.5 Gbps these pins may be tied to the same 1.1 V plane as VCCL_GXB[L,R]. However, for better jitter performance at high data rates this plane should be isolated from all other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 4, 8, 9, 11, and 14.
VCCL_GXB[L,R][0,2]	NA	Power	Analog power, block level clock distribution.	Connect VCCL_GXB[L,R][] to a 1.1 V linear or low noise switching regulator. These pins may be tied to the same 1.1 V plane as VCCT_[L,R] and/or VCCR_[L,R]. However, for better jitter performance at high data rates this plane should be isolated from all other power supplies. For the best jitter performance, provide each quad its own power source. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 4, 8, 9, 11, and 14.
VCCH_GXB[L,R][0,2]	NA	Power	Analog power, block level TX buffers.	Connect VCCH_GXB[L,R] to a 1.4 V or 1.5 V linear or low noise switching regulator. Connect these pins to 1.5 V if the transmitter channel data rate is≤ 6.5 Gbps. For data rates ≤ 6.5 Gbps it is possible to use 1.4 V from a source that is already utilized on the board as long as VCCH_GXB is properly isolated from the other supply. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 4, 8, 9, 11, and 14.
VCCA_[L,R]	NA	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.	Connect VCCA_[L,R] to a 2.5 V or 3.0 V linear or low noise switching regulator. Connect these pins to 3.0 V if the TX PLL and/or RX CDR are configured at a base data rate > 4.25 Gbps. Connect these pins to 2.5 V or 3.0 V if the TX PLL and/or RX CDR are configured at a base data rate≤ 4.25 Gbps (See Note 12). For data rates ≤ 4.25Gbps, if VCCA_[L,R] is 2.5 V these pins may be sourced from the same linear regulator as VCCAUX and/or VCCA_PLL with a proper isolation filter. Decoupling depends on the design decoupling requirements of the specific board design. See Notes 4, 8, 9, 11, and 14.
GXB_RX_[L,R][0:11]p	NA	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. (Note 5) Connect all unused GXB_RXp pins either individually to GND through a 10-KΩ resistor or tie all unused pins together through a single 10-KΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible.
GXB_RX_[L,R][0:11]n	NA	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. (Note 5) Connect all unused GXB_RXn pins either individually to GND through a 10-KΩ resistor or tie all unused pins together through a single 10-KΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible.
GXB_TX_[L,R][0:11]p	NA	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXp pins floating.

You should create a Quartus II design, enter your device I/O assignments and compile the design. The Quartus II software will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

HardCopy IV GX Pin Name	HardCopy IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
GXB_TX_[L,R][0:11]n	NA	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXn pins floating.
REFCLK_[L,R][0:5]p, GXB_CMURX_[L,R][0:5]p	NA	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.	These pins may be used for either reference clocks or CMU receiver channels. Switching between the two functions requires reprogramming the entire device. These pins should be AC-coupled when used as reference clocks (see Note 6). These pins may be AC-coupled or DC-coupled when used as CMU receiver channels (Note 5). Connect all unused GXB_CMURX_[L,R][]p/n pins either individually to GND through a 10-KΩ resistor or tie all unused pins together through a single 10-KΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Notes 2 and 3.
REFCLK_[L,R][0:5]n, GXB_CMURX_[L,R][0:5]n	NA	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.	These pins may be used for either reference clocks or CMU receiver channels. Switching between the two functions requires reprogramming the entire device. These pins should be AC-coupled when used as reference clocks (see Note 6). These pins may be AC-coupled or DC-coupled when used as CMU receiver channels (Note 5). Connect all unused GXB_CMURX_[L,R][]p/n pins either individually to GND through a 10-KΩ resistor or tie all unused pins together through a single 10-KΩ resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Notes 2 and 3.
GXB_CMUTX_[L,R][0:5]p, GXB_CMUTX_[L,R][0,5]n	NA	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_CMUTX_[L,R][]p and GXB_CMUTX_[L,R][]n floating. See Note 3.

HardCopy® IV GX and HardCopy IV E Device Family Pin Connection Guidelines
Preliminary PCG-01009-1.0

You should create a Quartus II design, enter your device I/O assignments and compile the design. The Quartus II software will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this document or the device handbook.

HardCopy IV GX Pin Name	HardCopy IV E Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
RREF_[L,R][0:1]	NA	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.	If any REFCLK pin or transceiver channel on one side (left or right) of the device is used, you must connect each RREF pin on that side of the device to its own individual 2.00-KΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

Notes:

1) This pin connection guideline is created based on the HardCopy IV GX and HardCopy IV E. Shaded cells indicate pin name differences between the HardCopy IV GX and HardCopy IV E devices.

2) Dual purpose CMU receiver channels. Can be used either as reference clock or CMU receiver channels in devices with 5th and 6th transceiver channels.

3) Only available in devices with CMU receiver channels. Devices with CMU receiver channels are indicated in the part number by either "H", "K", or "N" in the "Transceiver Count" position in the ordering code.

4) Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage drop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as innerplane capacitance with low inductance should be considered for higher frequency decoupling.

5) For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.

6) In PCI Express configuration, DC-coupling is allowed on REFCLK if the selected REFCLK I/O standard is HCSL (High-Speed Current Steering Logic).

7) The transmitter channel data rate could be equal to the TX PLL base data rate, or half of the TX PLL data rate, or quarter of the TX PLL base data rate depending on the local clock divider setting of 1, 2, or 4. For example, if the TX PLL base data rate is configured to support 6.0 Gbps and the local divider value of 2 is used, the transmitter channel runs at 3 Gbps. In this case, the VCCA_[L,R] pins must be connected to 3.0 V as the TX PLL base data rate > 4.25 Gbps.

8) If one or more transceivers are used on a particular side of the device (left [L] or right [R]) all of the transceiver power pins on that side of the device must be connected to its required power supply, except for VCCHIP which may be connected to GND if not using the HIP. For any unused quad VCCH_GXB may be tied to either 1.4 V or 1.5 V.
In addition, if none of the transceivers are used on one side then the transceiver power pins on that side may be tied to GND.

9) Use the HardCopy IV Early Power Estimator to determine the current requirements for VCC and other power supplies.

10) These pins are dual purpose configuration pins of Stratix® IV devices.

11) These supplies may share power planes across multiple HardCopy IV devices.

12) Examples 1 - 2 and Figures 1 - 2 illustrate power supply sharing guidelines that are data rate dependent. Example 3 and Figure 3 illustrate the power supply sharing guidelines for the HardCopy IV E.
Example 1 and Figure 1, "Power Regs <= 4.25 Gbps", show recommendations for designs that will not exceed 4.25 Gbps.
Example 2 and Figure 2, "4.25 Gbps<Data Rates<=6.5 Gbps", show recommendations for designs that are between 4.25 Gbps and 6.5 Gbps.
Example 3 and Figure 3, "Power Regs HardCopy IV E", show recommendations for designs that use the non-transceiver based HardCopy IV E.

13) Power pins should not share breakout vias from the BGA. Each ball on the BGA needs to have its own dedicated breakout via. VCC must not share breakout vias.

14) Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has fast transient response.
Line Regulation < 0.4%.
Load Regulation < 1.2%.

15) The guidelines provided within this document apply for both the Stratix IV prototype and HardCopy IV except when there is a different recommendation. In this case, the guideline will include a section highlighting where the prototype stage using the Stratix IV device requires different guidelines.

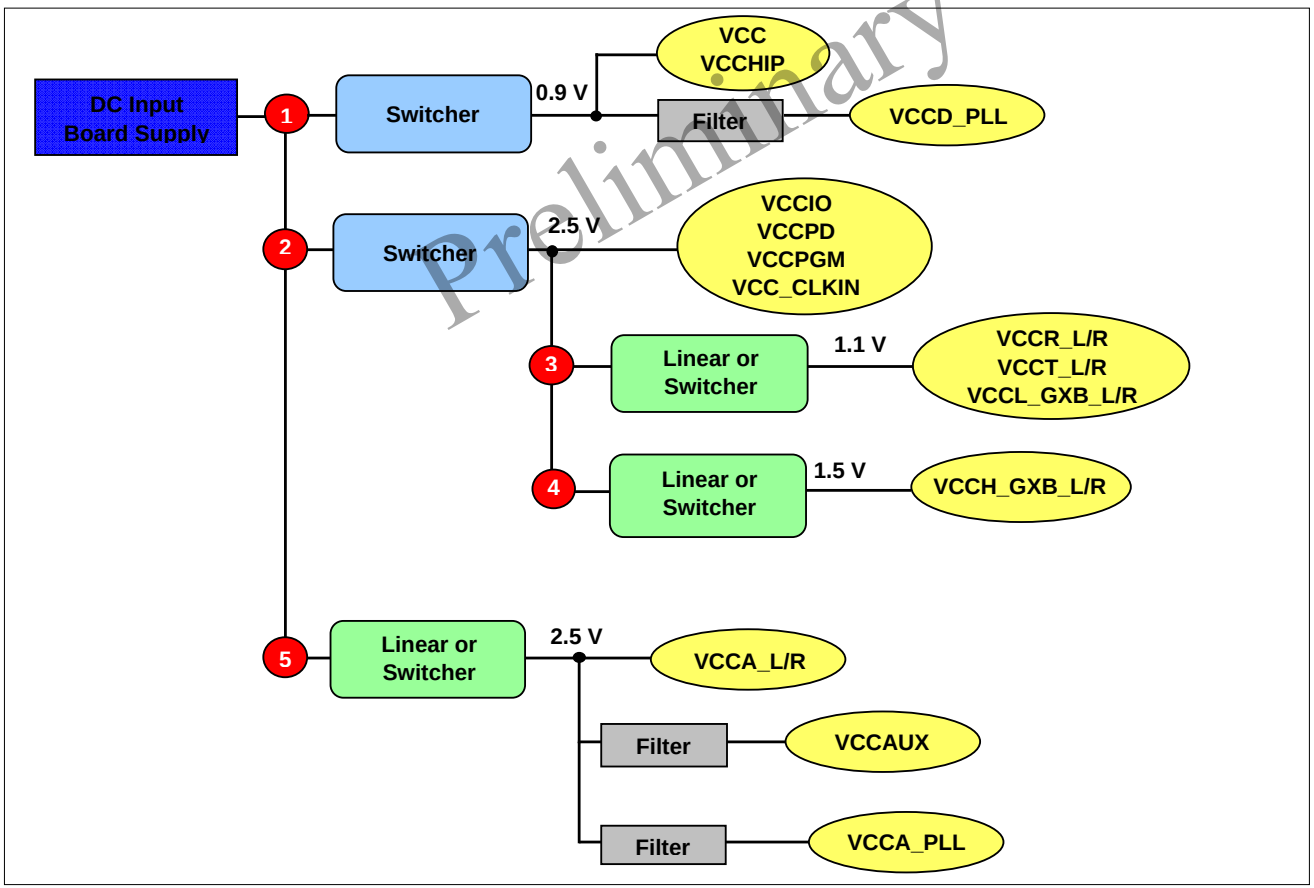
Example 1. HardCopy IV GX Power Supply Sharing Guidelines for Data Rates <= 4.25 Gbps

Example Requiring 5 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCHIP_[L,R]	1	0.9	± 30 mV	Switcher	Share	VCC and VCCHIP may share regulators. If not using HIP, VCCHIP may be tied to GND.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	May be able to share VCCD_PLL with VCC and VCCHIP with a proper isolation filter. If not sharing the regulator with VCC and/or VCCHIP the VCCD_PLL supply should not exceed a tolerance of ± 5%.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B VCCPGM	2	Varies	± 5%	Switcher	Share if 2.5 V	If all of these supplies require 2.5 V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, any other voltage requires a 2.5 V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCC_CLKIN[3,4,7,8]C		2.5				
VCCR_[L,R] VCCT_[L,R] VCCL_GXB[L,R][0:3]	3	1.1	± 5%	Linear or Switcher (*)	Share	HardCopy IV devices connect VCCR_L and VCCT_L together, and connect VCCR_R and VCCT_R together. Therefore, VCCR_L and VCCT_L must be sourced from the same linear or low noise switching regulator and VCCR_R and VCCT_R must be sourced from the same regulator. The left [L] and [R] may share the same regulator. Depending on the regulator capabilities this supply may be shared with multiple HardCopy IV devices. Use the EPE (Early Power Estimation) tool within Quartus II to assist in determining the power required for your specific design.
VCCH_GXB[L,R][0:3]	4	1.5	± 50 mV	Linear or Switcher (*)	Share	Depending on the regulator capabilities this supply may be shared with multiple HardCopy IV devices. Use the EPE tool to assist in determining the power required for your specific design. If not sharing a regulator the VCCH_GXB supply should not exceed a tolerance of ± 5%.
VCCA_[L,R] VCCAUX VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	5	2.5	± 5%	Linear or Switcher (*)	Share	May be able to share VCCA_PLL with VCCAUX and VCCA with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple HardCopy IV devices. Use the EPE tool to assist in determining the power required for your specific design.

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in Note 14.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram is provided in Figure 1.

Figure 1. Example HardCopy IV GX Power Supplies Block Diagram for Data Rates <=4.25 Gbps



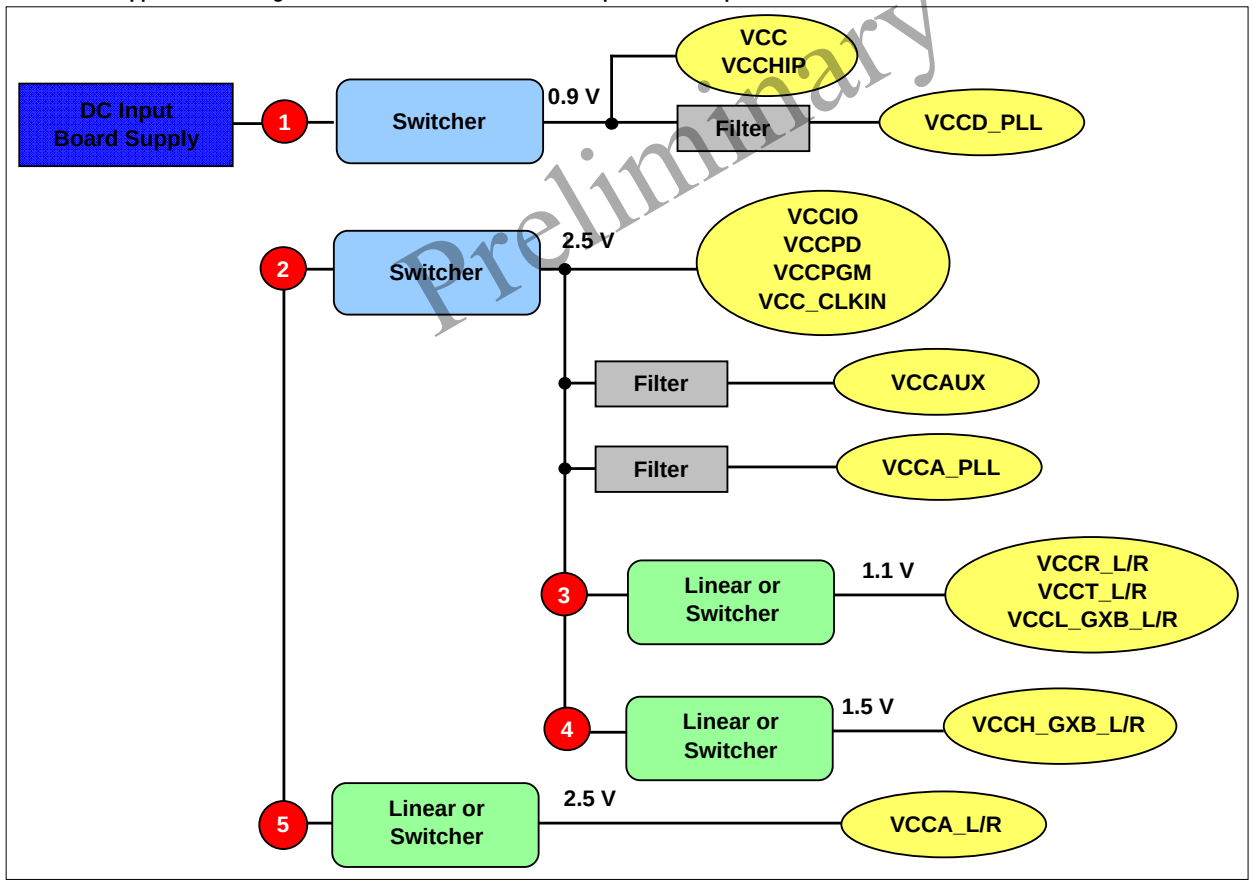
Example 2. HardCopy IV GX Power Supply Sharing Guidelines for Data Rates Between 4.25 Gbps and 6.5 Gbps

Example Requiring 5 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCHIP_[L,R]	1	0.9	± 30 mV	Switcher	Share	VCC and VCCHIP may share regulators. If not using HIP, VCCHIP may be tied to GND.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	May be able to share VCCD_PLL with VCC and VCCHIP with a proper isolation filter. If not sharing the regulator with VCC and/or VCCHIP the VCCD_PLL supply should not exceed a tolerance of ± 5%.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B VCCPGM VCC_CLKIN[3,4,7,8]C	2	Varies	± 5%	Switcher	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, any other voltage requires a 2.5V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCAUX VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]		2.5			Isolate/share	VCCAUX and VCCA_PLL may be able to share a regulator with a proper isolation filter.
VCCR_[L,R] VCCT_[L,R] VCCL_GXB[L,R][0:3]	3	1.1	± 5%	Linear or Switcher (*)	Share	HardCopy IV devices connect VCCR_L and VCCT_L together, and connect VCCR_R and VCCT_R together. Therefore, VCCR_L and VCCT_L must be sourced from the same linear or low noise switching regulator and VCCR_R and VCCT_R must be sourced from the same regulator. The left [L] and [R] may share the same regulator. Depending on the regulator capabilities this supply may be shared with multiple HardCopy IV devices. Use the EPE (Early Power Estimation) tool within Quartus II to assist in determining the power required for your specific design.
VCCH_GXB[L,R][0:3]	4	1.5	± 50 mV	Linear or Switcher (*)	Isolate	Depending on the regulator capabilities this supply may be shared with multiple HardCopy IV devices. Use the EPE tool to assist in determining the power required for your specific design. If not sharing a regulator for the VCCH_GXB supply should not exceed a tolerance of ± 5%.
VCCA_[L,R]	5	3	± 5%	Linear or Switcher (*)	Isolate	Depending on the regulator capabilities this supply may be shared with multiple HardCopy IV devices. Use the EPE tool to assist in determining the power required for your specific design.

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in Note 14.
Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram is provided in Figure 2.

Figure 2. Example HardCopy IV GX Power Supplies Block Diagram for Data Rates Between 4.25 Gbps and 6.5 Gbps



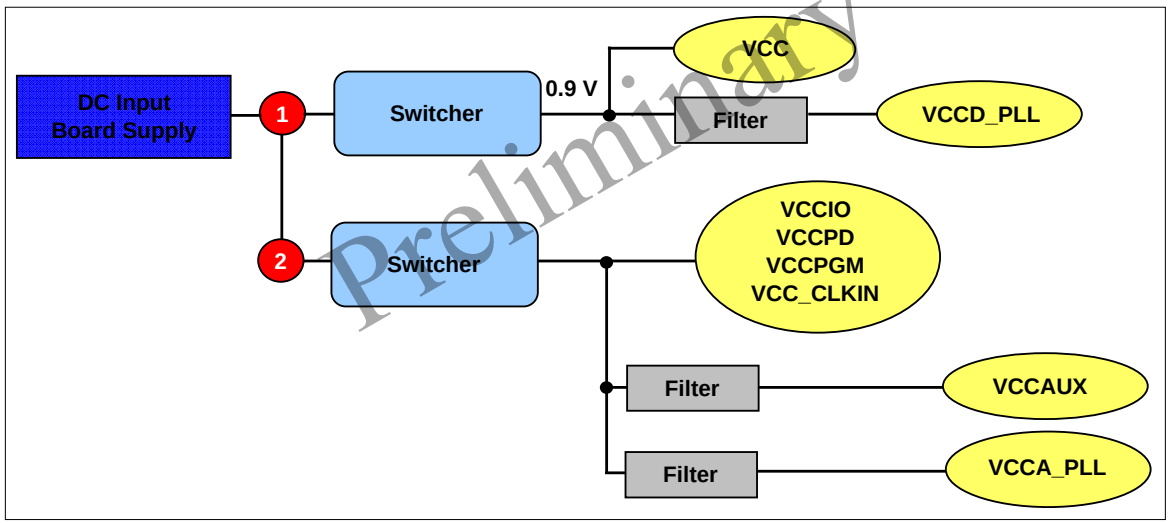
Example 3. HardCopy IV E Power Supply Sharing Guidelines (non-transceiver device)

Example Requiring 2 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	1	0.9	± 3 0mV	Switcher	Share Isolate	May be able to share VCCD_PLL with VCC with a proper isolation filter. If not sharing the regulator with VCC the VCCD_PLL supply should not exceed a tolerance of ± 5%.
VCCAUX	2	2.5	± 5%	Switcher	Isolate	May be able to share VCCA_PLL with VCCAUX with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple HardCopy IV devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]					Isolate	
VCC_CLKIN[3,4,7,8]C					Share	
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B		Varies			Share if 2.5 V	If all of these supplies require 2.5 V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, any other voltage requires a 2.5 V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B						
VCCPGM						

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram is provided in Figure 3.

Figure 3. Example HardCopy IV E Power Supplies Block Diagram



HardCopy® IV GX and HardCopy IV E Device Family Pin Connection Guidelines Preliminary PCG-01009-1.0		
Revision History		
Revision	**Description of Changes**	**Date**
1.0	Initial Release.	11/13/2009