HardCopy® III Device Family Pin Connection Guidelines

Preliminary PCG-01010-1.0

The pin connection guidelines are considered preliminary. These pin connection guidelines should only be used as a recommendation, not as a specification. The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins			
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively. OCT Rd is not supported on these pins.	Connect unused pins to GND.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively. OCT Rd is not supported on these pins.	Connect unused pins to GND.
PLL_[L1:L4,R1:R4]_CLKOUT0n PLL_[L1:L4,R1:R4]_FB_CLKOUT0p	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1 PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
PLL_[T1,T2,B1,B2]_CLKOUT0p PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	I/O pins that may be used as two single-ended clock output pins or one differential clock output pair.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
Dedicated Configuration/JTAG Pins			
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high turns off the weak pull-ups, while a logic low turns them on.	The nIO_PULLUP can be tied directly to VCCPGM, use a 1 KΩ pull-up resistor or tied directly to GND depending on the use desired for the device. The user I/O pins with internal pull-ups controlled by the nIO_PULLUP are nCSO, ASDO, DATA[7:0], CLKUSR, INIT_DONE, DEV_OE, and DEV_CLRn.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy III device.	If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy III device.	If the temperature sensing diode is not used then connect this pin to GND.

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Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
MSEL[2:0]	Input	Pins are configuration inputs for Stratix III FPGA only, they set the FPGA prototype configuration scheme. MSEL[0:2] are NC (No Connection) pins for HardCopy III devices but they preserve the pin assignment and direction from the Stratix III prototype, allowing drop-in replacement.	The connection to the board on these pins are "don't care" for HardCopy III. In the prototype stage using the Stratix III these pins are internally connected through a 5-KΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used these pins should be tied to VCCPGM or GND. Refer to chapter 11, "Configuring Stratix III Devices", of the Stratix III Handbook. If only JTAG configuration is used then connect these pins to ground. See Note 3.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	If multi-device are on a board, the configuration data stored in the FPGA device must be updated to exclude the configuration data for the HardCopy III device. The nCE pin of the HardCopy III device must be connected to GND. The nCE pin of the FPGA that was driven by the HardCopy III nCEO pin must now be driven by the nCEO pin of the FPGA that precedes the HardCopy III device in the chain. In single HardCopy III device, nCE pin must be connected to GND. In the prototype stage using the Stratix III in a multi-device configuration, nCE of the first device is tied directly to GND while its nCEO pin drives the nCE of the next device in the chain. However, in single device configuration and JTAG programming, nCE should be connected directly to GND. See Note 3.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy III to enter a reset state and tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.	For HardCopy III devices, nCONFIG pin is designed with weak internal resistor pulled up to VCCPGM. The board can be designed to have additional switching capability to this pin to allow pulsing the nCONFIG in order to restart the HardCopy III device. In the prototype stage using the Stratix III nCONFIG should be connected directly to the configuration controller when the FPGA uses a passive configuration scheme, or through a 10-KΩ resistor tied to VCCPGM when using an active serial configuration scheme. If this pin is not used, it requires a connection directly or through a 10-KΩ resistor to VCCPGM. See Note 3.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. When this pin is driven high it indicates that the devic is entering user mode.	For HardCopy III devices, CONF_DONE pin is designed with weak internal resistor pulled up to VCCPGM. In the prototype stage using the Stratix III nCONFIG should be connected directly to the configuration controller when the FPGA uses a passive configuration scheme, or through a 10-KΩ resistor tied to VCCPGM when using an active serial configuration scheme. If this pin is not used, it requires a connection directly or through a 10-KΩ resistor to VCCPGM. See Note 3.
nCEO	Output	Output that drives low when device configuration is complete.	nCEO is left floating for HardCopy III devices. In the prototype stage using the Stratix III with multi-device configuration, this pin feeds the nCE pin of a subsequent device. During single device configuration, leave this pin unconnected. See Note 3.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy III drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. This pin is not available as a user I/O pin.	For HardCopy III devices, nSTATUS pin is designed with weak internal resistor pulled up to VCCPGM. In the prototype stage using the Stratix III if internal pull-up resistors on the enhanced configuration device are used, external 10-KΩ pull-up should not be used on these pins. Otherwise, an external 10-KΩ pull-up resistors to VCCPGM should be used. When using Passive configuration schemes this pin should also be monitored by the configuration controller. See Note 3.

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PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.	The PORSEL pin should be tied directly to VCCPGM or GND.
TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-KΩ pull-down resistor to GND. To disable the JTAG circuitry connect TCK to GND via a 1-KΩ resistor. TCK is powered by VCCPD1A.
TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 10-KΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TMS to VCCPD via a 1-KΩ resistor. TMS is powered by VCCPD1A.
TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 10-KΩ pull-up resistor to VCCPD. To disable the JTAG circuitry connect TDI to VCCPD via a 1-KΩ resistor. TDI is powered by VCCPD1A.
TDO	Output	Dedicated JTAG test data output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected. TDO is powered by VCCPD1A.
TRST	Input	Dedicated active low JTAG test reset input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.	Utilization of TRST is optional. When using this pin ensure that TMS is held high or TCK is static when TRST is changed from low to high. If not using TRST, tie this pin to a 1-KΩ pull-up resistor to VCCPD. To disable the JTAG circuitry, tie this pin to GND. TRST is powered by VCCPD1A.
Optional/Dual-Purpose Configuration Pins			
nCSO	Output	Dedicated control signal from Stratix III devices to the serial configuration device in AS mode that enables the configuration device. This pin is kept in HardCopy III for compatibility reasons.	When this pin is not used as an output then it is recommended to leave the pin unconnected. If Erasable Programmable Configuration Serial (EPCS) is used in user mode as a boot-up RAM data access for a Nios II processor, DCLK, DATA[0], ASDO, and nCSO need to be connected to the EPCS device.
ASDO	Output	Dedicated control signal from Stratix III devices to the serial configuration device in AS mode used to read out configuration data. This pin is kept in HardCopy III for compatibility reasons.	When this pin is not used as an output then it is recommended to leave the pin unconnected. If Erasable Programmable Configuration Serial (EPCS) is used in user mode as a boot-up RAM data access for a Nios II processor, DCLK, DATA[0], ASDO, and nCSO need to be connected to the EPCS device.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix III devices. This pin is kept in HardCopy III for compatibility reasons.	For HardCopy III leave this pin unconnected. If Erasable Programmable Configuration Serial (EPCS) is used in user mode as a boot-up RAM data access for a Nios II processor, DCLK, DATA[0], ASDO, and nCSO need to be connected to the EPCS device. In the prototype stage using the Stratix III do not leave this pin floating. Drive this pin ether high or low. See Note 3.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits on the Stratix III device. This pin is optional and is used when the CRC error detection circuit is enabled in the Stratix III FPGA.	For HardCopy III, this pin retains the same I/O functions from Stratix III prototype, but not CRC_ERROR because no device programming is needed. See Note 2. In the prototype stage using the Stratix III connect this pin to an external 10-KΩ pull-up resistor to VCCPGM. See Note 3.
DEV_CLRn	I/O, Input	Optional pin for Stratix III FPGA that allows designers to override all clears on all device registers. In this case, when this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.	For HardCopy III, this pin retains the same I/O function from Stratix III device. See Note 2. In the prototype stage using the Stratix III when DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground. See Note 3.
DEV_OE	I/O, Input	Optional pin for Stratix III FPGA that allows designers to override all tri-states on the device. In this case, when the pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.	For HardCopy III, the pin retains the same I/O function from Stratix III device. See Note 2. In the prototype stage using the Stratix III when DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground. See Note 3.

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Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
DATA0	I/O, Input	Dual-purpose configuration data input pin for Stratix III FPGA. In this case, the DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.	For HardCopy III, these pins are I/O functions only. If Erasable Programmable Configuration Serial (EPCS) is used in user mode as a boot-up RAM or data access for a Nios II processor, DCLK, DATA[0], ASDO, and nCSO need to be connected to the EPCS device. See Note 2. In the prototype stage using the Stratix III when DATA0 is not used and this pin is not used as an I/O then it is recommended to leave this pin unconnected. See Note 3.
DATA[1:7]	I/O, Input	Dual-purpose configuration data input pin for Stratix III FPGA. In this case the DATA[0:7] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.	For HardCopy III, these pins are I/O functions only. See Note 2. In the prototype stage using the Stratix III when DATA[1:7] is not used and this pin is not used as an I/O then it is recommended to leave these pins unconnected. See Note 3.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE in Stratix III FPGA. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	For HardCopy III, this pin retains the same I/O function from Stratix III device. See Note 2. In the prototype stage using the Stratix III connect this pin to an external 10-KΩ pull-up resistor to VCCPGM. See Note 3.
CLKUSR	I/O, Input	This pin is an optional user-supplied clock input and it can be used as a user I/O pin in Stratix III FPGA. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	For HardCopy III, this pin retains the same I/O function from Stratix III device. See Note 2. In the prototype stage using the Stratix III if the CLKUSR is not used as a configuration clock input and this pin is not used as an I/O then it is recommended to leave this pin to GND. See Note 3.
Differential I/O Pins			
DIFFIO_RX[##]p/n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up.
DIFFIO_TX[##]p/n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up.
DIFFOUT_[##]p/n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up.
External Memory Interfaces Pins			
DQS[1:44][T,B], DQS[1:40][L,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up.
DQSn[1:44][T,B], DQSn[1:40][L,R]	I/O, DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up.
DQ[1:44][T,B], DQ[1:40][L,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up.

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CQ[1:44][T,B], CQ[1:40][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up.
CQn[1:44][T,B], CQn[1:40][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.	Unused pins can be tied to GND or unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull-up.
Reference Pins			
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, ground or any other signal. These pins must be left floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.
RUP[1:8]A (RUP[3,8]C - Stratix III only)	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to the VCCIO of the bank in which the RUP pin resides or GND. When using OCT tie these pins to the required banks VCCIO through either a 25 Ω or 50 Ω resistor, depending on the desired I/O standard. Refer to the HardCopy III handbook for the desired resistor value for the I/O standard used.
RDN[1:8]A (RDN[3,8]C - Stratix III only)	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to GND. When using OCT tie these pins to GND through either a 25 Ω or 50 Ω resistor depending on the desired I/O standard. Refer to the HardCopy III handbook for the desired resistor value for the I/O standard used.
Supply and Reference Pins			
VCCL	Power	VCCL supplies power to the core voltage power supply pins.	Connect these pins to 0.9 V and use a common plane for both VCCL and VCC power supplies. With proper isolation VCCD_PLL may share the same regulator as VCCL and VCC. For the best jitter performance on your PLL dedicated output clock use separate power planes and voltage regulators for VCCD_PLL and VCCL/VCC. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 1.
VCC	Power	VCC supplies power to the periphery circuitry.	Connect these pins to 0.9 V and use a common plane for both VCCL and VCC power supplies. With proper isolation VCCD_PLL may share the same regulator as VCCL and VCC. For the best jitter performance on your PLL dedicated output clock use separate power planes and voltage regulators for VCCD_PLL and VCCL/VCC. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 1.
VCCD_PLL[L,R][1:4] VCCD_PLL[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to 0.9 V, even if the PLL is not used.	Connect these pins to 0.9 V, even if the PLL is not used. With proper isolation VCCD_PLL may share the same regulator as VCCL and VCC. For better jitter performance on your PLL dedicated output clock use separate power planes and voltage regulators for VCCD_PLL and VCCL/VCC. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 1.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to 2.5 V, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.	You are required to connect these pins to 2.5 V, even if the PLL is not used. Use an isolated linear or low noise switching power supply. Power on the PLLs operating at the same frequency should be decoupled. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 1.
VCC_CLKIN[3,4,7,8]	Power	Differential clock input power supply for top and bottom I/O bank. Connect to 2.5 V.	Connect these pins to 2.5 V power source. These pins may be tied to the same regulator as VCCIO, VCCPGM and VCCPD, but only if each of these supplies require 2.5 V sources. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 1.

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You should create a Quartus II design, enter your device I/O assignments and compile the design. The Quartus II software will check your pin connections with respect to I/O assignment and placement rules to ensure proper device operation. These rules are dependent on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description	Connection Guidelines
VCCPD[1:8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 3.0 V or 2.5 V. For 3.0 V I/O standard connect VCCPD to 3.0 V, and for 1.2V, 1.8 V, or 2.5 V I/O standards connect VCCPD to 2.5 V.	The VCCPD pins require 2.5 V or 3.0 V and must ramp-up from 0 V to 2.5 V or 3.0 V within 100 ms to ensure successful configuration. When these pins require 2.5 V they may be tied to the same regulator as VCC_CLKIN, VCCPGM and VCCIO, but only if each of these supplies require 2.5 V sources. VCC_CLKIN has a set voltage of 2.5 V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPGM and/or VCCIO as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 1.
VCCIO[1:8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTL 3.0 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V), 3.0 V PCI/PCI-X and LVTTL 3.0 V I/O standards.	You are required to connect these pins to 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.0 V supplies, depending on the I/O standard connected to the specified banks. When these pins require 2.5 V they may be tied to the same regulator as VCC_CLKIN, VCCPGM and VCCPD, but only if each of these supplies require 2.5 V sources. VCC_CLKIN has a set voltage of 2.5 V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPGM and/or VCCPD as long as they all require the same voltage. Decoupling depends on the design decoupling requirements of the specific board. See Note 1.
VCCPGM	Power	Configuration pins power supply. Can be connected to 1.8 V, 2.5 V, or 3.0 V depending on the particular design	Connect this pin to either 1.8 V, 2.5 V, or 3.0 V power supply. When these pins require 2.5 V they may be tied to the same regulator as VCC_CLKIN, VCCIO and VCCPD, but only if each of these supplies require 2.5 V sources. VCC_CLKIN has a set voltage of 2.5 V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPD and/or VCCIO as long as they all require the same voltage. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 1.
VREF[1:8][A,B,C]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.	If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 1.
VCCPT	Power	Stratix III FPGA Power supply for the programmable power technology. Some of the VCCPT pins are NC (No Connection) pins in HardCopy III devices. The remaining pins are used for the Temperature Sensing Diode (TSD) and Power on Reset (POR), and these pins must be connected to 2.5 V. To determine the exact pins for each case compare the pin assignments for VCCPT in the Stratix III and HardCopy III pin tables.	Four of the eight VCCPT pins from Stratix III are re-assigned as NC in the HardCopy III device and are treated as "don't care" pins. Therefore, these pins may be left unconnected on the board. The remaining VCCPT pins, labeled as such, in HardCopy III must be connected to an isolated 2.5 V supply. In the prototype stage using the Stratix III use an isolated 2.5 V power supply for these pins. The voltage on these pins must ramp-up from 0 V to 2.5 V within 5 ms to ensure successful configuration. Decoupling depends on the design decoupling requirements of the specific board. See Note 3.
VCCBAT	Power	Battery back-up power supply for design security volatile key register for Stratix III FPGA only. VCCBAT is a NC (No Connection) pin of HardCopy III devices.	The connection to the board on this pin is "don't care" for the HardCopy III. In the prototype stage using the Stratix III when not using the volatile key, tie this to a 3.0 V supply or GND. Do not share this source with other FPGA power supplies. See Note 3.
GND	Ground	Device ground pins.	All GND pins should be connected to the board ground plane.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

Notes:

1) Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage drop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as innerplane capacitance with low inductance should be considered for higher frequency decoupling.

2) These pins are dual purpose configuration pins of Stratix® III devices.

3) The guidelines provided within this document apply for both the Stratix III prototype and HardCopy III except when there is a different recommendation. In this case, the guideline will include a section highlighting where the prototype stage using the Stratix III device requires different guidelines.

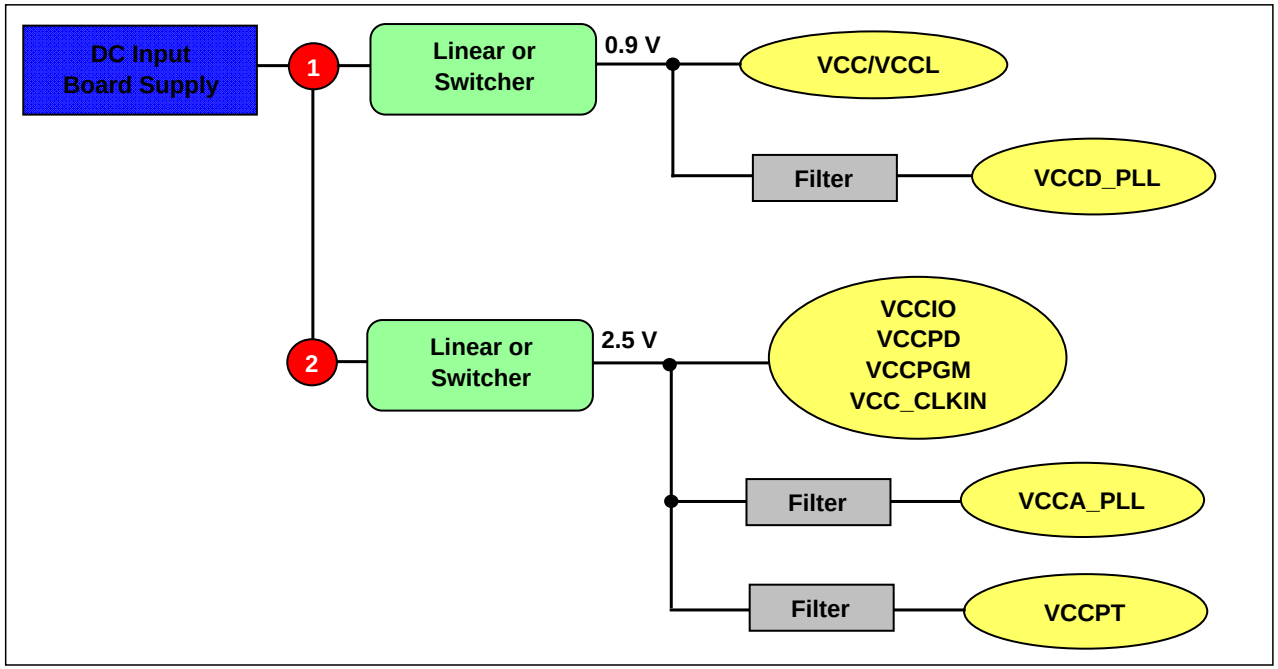
Example 1. HardCopy III Power Supply Sharing Guidelines

Example Requiring 2 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC VCCL	1	0.9	± 30mV	Switcher	Share	May be able to share VCCD_PLL with VCC/VCCL with a proper isolation filter. If not sharing the regulator with VCC/VCCL the VCCD_PLL supply should not exceed a tolerance of ± 5%.
VCCD_PLL[L,R][1:4], VCCD_PLL[T,B][1:2]					Isolate	
VCCPT	2	2.5	± 5%		Isolate	With proper isolation VCCPT and VCCA_PLL may be share a regulator. Depending on the regulator capabilities this supply may be shared with multiple HardCopy III devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]					Isolate	
VCC_CLKIN[3,4,7,8]					Share	
VCCIO[1:8][A,B,C]		Varies			Share if 2.5 V	If all of these supplies require 2.5 V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require a 2.5 V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD[1:8][A,B,C]						
VCCPGM						

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram is provided in Figure 1.

Figure 1. Example HardCopy III Power Supplies Block Diagram



HardCopy® III Device Family Pin Connection Guidelines Preliminary PCG-01010-1.0		
Revision History		
Revision	**Description of Changes**	**Date**
1.0	Initial Release.	11/13/2009