Cyclone V Device Family Advance Information Brief

Cyclone® V FPGAs are designed to simultaneously meet shrinking power consumption, cost, and time-to-market requirements and increasing bandwidth requirements for high-volume, cost-sensitive applications. Built on TSMC's 28-nm Low-Power (28LP) process and including an abundance of hard IP, Cyclone V FPGAs deliver up to 40% lower power compared to the previous generation. A new 8-input adaptive logic module (ALM), up to 12M of memory, and variable precision digital signal processing (DSP) blocks improve logic integration and differentiation capabilities. New 3G and 5G transceivers and hard memory controllers combine to meet increasing bandwidth needs. Cyclone V devices are ideal for cost and power sensitive, small form factor applications in wireless, wireline, military, broadcast, industrial, consumer, and communications industries.

The Cyclone V family comes in three targeted variants:

- **Cyclone V E FPGA**—Optimized for lowest system cost and power for a wide spectrum of general logic and DSP applications
- **Cyclone V GX FPGA**—Optimized for lowest cost and power for 614 Mbps to 3.125 Gbps transceiver applications
- **Cyclone V GT FPGA**—FPGA industry's lowest cost and power for 5.0 Gbps transceiver applications

In addition to transceivers, key hard IP blocks include:

- Hard memory controllers supporting 400 MHz DDR3 and DDR2 SDRAM, LPDDR, and LPDDR2 SDRAM
- PCI Express Gen2 with multi-function, supporting up to eight peripherals
- Variable precision DSP blocks

Cyclone V FPGAs support all mainstream single-ended and differential I/O standards, including 3.3 V at up to 16 mA drive strengths. Cyclone V devices also offer the lowest system cost by requiring only two core voltages to operate the devices and are available in low-cost wirebond packaging. Cyclone V devices also support innovative cost saving features such as Configuration via Protocol (CvP) and partial reconfiguration. To protect your valuable IP investments, Cyclone V FPGAs also provide comprehensive design protection features.

101 Innovation Drive
San Jose, CA 95134
www.altera.com

With these innovations, Cyclone V devices deliver ideal performance and capability for a wide range of applications. Table 1 lists the many Cyclone V device features.

Table 1. Features Summary

- Technology:
  - 28-nm TSMC low-power process technology
  - 1.1-V core voltage
- Low-power serial transceivers:
  - 614 Mbps to 5.0 Gbps integrated transceivers
  - Transmit pre-emphasis and receiver equalization
  - Dynamic partial reconfiguration of individual channels
- General purpose I/Os (GPIOs):
  - 875 Mbps LVDS (receiver), 840 Mbps LVDS (transmitter)
  - 400 MHz/800 Mbps external memory interface
  - On-chip termination (OCT)
  - 3.3-V support with up to 16 mA drive strength
- Embedded transceiver I/O hard IP:
  - Basic mode (up to 5.0 Gbps)
  - PCIe Gen2 x1, x2 and Gen1 x1, x2, or x4; with multi-function, endpoint, and root port
  - Gigabit Ethernet (GbE) and XAUI PCS
  - Serial RapidIO® (SRIO) PCS
  - Common Public Radio Interface (CPRI) PCS
  - JESD204A PCS
  - OBSAI PCS
  - SATA PCS
  - SDI SD/HD and 3G-SDI PCS
  - DisplayPort PCS
  - Vx1 PCS
- High-performance core fabric:
  - Enhanced 8-input ALM with four registers
- Variable precision DSP blocks hard IP:
  - Natively support three signal processing precision ranging from three 9 × 9s, two 18 × 19s, or one 27 × 27 in the same variable precision DSP block
  - 64-bit accumulator and cascade
  - Embedded internal coefficient memory
  - Pre-adder/subtractor improves efficiency
- Internal memory blocks:
  - M10K, 10-Kbit with soft error correction code (ECC)
  - Memory logic array block (MLAB), 640-bit distributed LUTRAM—up to 25% of the ALMs can be used as MLAB memory
- DDR3, DDR2, LPDDR, and LPDDR2 memory controller hard IP
- Partial and dynamic reconfiguration of the FPGA
- PLLs:
  - Precision clock synthesis, clock delay compensation, and zero delay buffering
  - Integer mode and fractional mode
- Clock networks:
  - 625 MHz global clock network
  - Global, quadrant, and peripheral clock networks
  - Unused clock networks can be powered down to reduce dynamic power
- Configuration:
  - Configuration via Protocol (CvP)
  - Active Serial (x1 and x4), Fast Passive Parallel (x8 and x16), Passive Serial, and JTAG options
  - Enhanced advanced encryption standard (AES) design security features
  - Tamper protection
- Packaging:
  - Wirebond halogen-free packages
  - Multiple device densities with compatible package footprints for seamless migration between different device densities
  - Lead and RoHS-compliant options

Cyclone V Family Plan

Table 2 lists the Cyclone V device family features:

Table 2. Cyclone V Device Family Features

Family	Device	Core Fabric						Interconnect			Hard IP	
		KLEs	Block Memory (Kb)	MLAB (Kb)	DSP Blocks	18×19 Mults	PLLs	XCVRs (3G, 5G)	GPIO	LVDS	PCIe Blocks	Memory Control-lers
Cyclone V E	5CEA2	25	1,560	Yes	39	78	4	—	300	48	—	1
	5CEA5	48	3,120	Yes	78	156	4	—	300	100	—	1
	5CEA8	75	4,620	Yes	132	264	4	—	360	100	—	2
	5CEB5	150	6,160	Yes	220	440	4	—	488	122	—	2
	5CEB9	300	12,760	Yes	406	812	4	—	488	122	—	2
Cyclone V GX	5CGXC3	25	1,200	Yes	40	80	5	3, 0	194	48	1	1
	5CGXC4	50	2,920	Yes	70	140	6	6, 0	360	100	1	2
	5CGXC5	75	4,620	Yes	132	264	6	6, 0	360	100	1	2
	5CGXC7	150	6,160	Yes	220	440	7	9, 0	488	122	1	2
	5CGXC9	300	12,760	Yes	406	812	8	12, 0	688	122	1	2
Cyclone V GT	5CGTD3	75	4,620	Yes	132	264	6	0, 6	360	100	2	2
	5CGTD5	150	6,160	Yes	220	440	7	0, 9	488	122	2	2
	5CGTD8	300	12,760	Yes	406	812	8	0, 12	688	122	2	2

Table 3 lists the Cyclone V package plan, associated available user I/O, and package migration capability.

Table 3. Cyclone V Package Plan

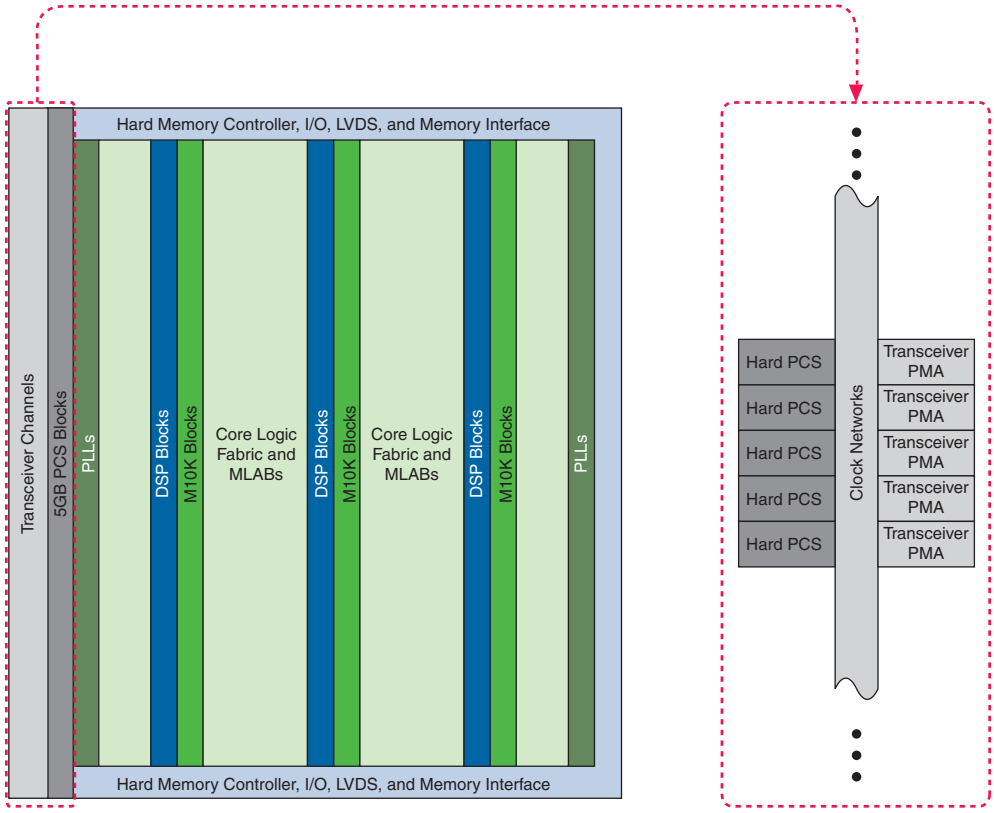
Family	Device	KLEs	E144 22×22	F256 17×17	F324 19×19	U484 19×19	F484 23×23	F672 25×25	F896 31×31	F1152 35×35
Cyclone V E	5CEA2	25	90	140	—	300	300	—	—	—
	5CEA5	48	90	140	—	300	300	—	—	—
	5CEA8	75	—	—	—	260	260	360	—	—
	5CEB5	150	—	—	—	—	260	345	488	—
	5CEB9	300	—	—	—	—	—	345	488	—
Cyclone V GX	5CGXC3	25	—	97 / 3	114 / 3	194 / 3	194 / 3	—	—	—
	5CGXC4	50	—	—	120 / 6	238 / 6	238 / 6	360 / 6	—	—
	5CGXC5	75	—	—	120 / 6	238 / 6	238 / 6	360 / 6	—	—
	5CGXC7	150	—	—	—	—	230 / 6	345 / 9	488 / 9	—
	5CGXC9	300	—	—	—	—	—	345 / 9	488 / 9	688 / 12
Cyclone V GT	5CGTD3	75	—	—	—	238 / 6	238 / 6	360 / 6	—	—
	5CGTD5	150	—	—	—	—	230 / 6	345 / 9	488 / 9	—
	5CGTD8	300	—	—	—	—	—	345 / 9	488 / 9	688 / 12

Low-Power Serial Transceivers

Cyclone V devices deliver the industry's lowest power 5.0 Gbps transceivers at 88 mW maximum power consumption per channel. Cyclone V transceivers are designed to be compliant for a wide range of protocols and data rates.

The transceivers are positioned on the left outer edge of the device, as shown in Figure 1.

Figure 1. Cyclone V Device Chip View ***(Note 1)***



Note to Figure 1:

(1) Figure 1 represents a given variant of a Cyclone V device with transceivers. Other variants may have a different floor plan than the one shown here.

PMA Support

The PMA block is isolated from the rest of the chip to prevent core and I/O noise from coupling into the transceivers, ensuring optimal signal integrity. The transceiver channels consist of the physical medium attachment (PMA), physical coding sublayer (PCS), and clock networks. You can also use the unused transceivers PMA channels as additional transmit PLLs. Table 4 lists the transceiver PMA features.

Table 4. Transceiver PMA Features

Features	Capability
Chip-to-chip support	5.0 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable deserialization and word alignment	Flexible deserialization width and configurable word alignment patterns
Equalization and pre-emphasis	Pre-emphasis (1 post-tap) and equalization (1 EQ stage) (No DFE)
Ring oscillator transmit PLLs	614 Mbps to 5.0 Gbps
Input reference clock range	20 MHz to 400 MHz
Dynamic Partial Reconfiguration (DPRIO)	Allows reconfiguration of single channels without affecting operation of other channels.

PCS Support

The Cyclone V core logic connects to the PCS through an 8-, 10-, 16-, 20-, 32-, or 40-bit interface, depending on the transceiver data rate and protocol. Cyclone V devices contain PCS hard IP to support PCIe Gen1 and Gen2, XAUI, GbE, SRIO, and CPRI. All other standard and proprietary protocols from 614 Mbps to 5.0 Gbps are supported through 5G Basic (up to 5.0 Gbps) and 3G Basic (up to 3.125 Gbps) transceiver PCS hard IP. Table 5 lists the transceiver PCS features.

Table 5. Transceiver PCS Features (Part 1 of 2)

PCS Support	Data Rates (Gbps)	Transmit Data Path	Receiver Data Path
3G and 5G Basic	0.614 to 5.0	Phase compensation FIFO, byte serializer, 8B/10B encoder, bit-Slip channel bonding	Word aligner, de-skew FIFO, rate match FIFO, 8B/10B decoder, byte deserializer, byte ordering
×1, ×2, ×4 PCIe Gen1 and Gen2 ×1, ×2	2.5 and 5.0	Same as 3G and 5G Basic plus PIPE 2.0 interface to the core logic	Same as 3G and 5G Basic plus PIPE 2.0 interface to the core logic
GbE	1.25	Same as 1G Basic plus the Gbe state machine	Same as 1G Basic plus the Gbe state machine
XAUI	3.125	Same as 3G Basic plus the XAUI state machine for bonding four channels	Same as 3G Basic plus the XAUI state machine for re-aligning four channels
SRIO	1.25 to 3.125	Same as 1G and 3G Basic plus the SRIO V2.1-compliant ×2 and ×4 channel bonding	Same as 1G and 3G Basic plus the SRIO V2.1-compliant ×2 and ×4 deskew state machine
SDI, SD/HD, 3G-SDI	0.27, 1.485, 2.97	Phase compensation FIFO, byte serializer	Word aligner, byte deserializer

Table 5. Transceiver PCS Features (Part 2 of 2)

PCS Support	Data Rates (Gbps)	Transmit Data Path	Receiver Data Path
SATA	1.5 and 3.0	Phase compensation FIFO, byte serializer, electrical idle	Word aligner, byte deserializer, signal detect, wider spread of asynchronous SSC
CPRI	0.6144 to 4.9152	Same as 1G and 5G Basic plus the transmitter (TX) deterministic latency	Same as 1G and 5G Basic plus the receiver (RX) deterministic latency
OBSAI	0.768 to 3.072	Same as 1G and 5G Basic plus the transmitter (TX) deterministic latency	Same as 1G and 5G Basic plus the receiver (RX) deterministic latency
Vx1	Up to 3.75	Phase compensation FIFO, byte serializer, electrical idle	Word aligner, byte deserializer, signal detect, wider spread of asynchronous SSC
Display Port	Up to 2.7	Phase compensation FIFO, byte serializer, electrical idle	Word aligner, byte deserializer, signal detect, wider spread of asynchronous SSC
JESD204A	0.3125 to 3.125	Self-clocked 8B/10B encoder	Self-clocked 8B/10B decoder, CDR

External Memory and General Purpose I/Os

Cyclone V devices offer highly configurable general purpose I/Os. The many features of the general purpose I/Os are:

- Programmable bus hold and weak pull up
- LVDS output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis
- Dynamic on-chip parallel termination for all I/O banks with OCT calibration to limit termination impedance variation to ± 15%
- On-chip dynamic termination (ability to swap between serial and parallel termination depending on whether reading of writing on a common bus) for signal integrity
- Unused voltage reference (VREF) pins can be configured as a user I/O
- Easy timing closure support using the hard read FIFO in the input register path and delay-locked loop (DLL) delay chain with fine and coarse architecture

Cyclone V devices support up to two hard memory controllers for DDR3, DDR2, LPDDR, and LPDDR2 devices. Each controller supports 8- to 32-bit components up to 4 Gb in density with two-chip select and optional ECC.

Cyclone V devices also support soft memory controllers DDR3, DDR2, LPDDR2, and LPDDR for maximum flexibility. Table 6 lists external memory interface block performance.

Table 6. External Memory Interface Performance (Part 1 of 2)

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)
DDR3	1.5	400	300
DDR2	1.8	400	300

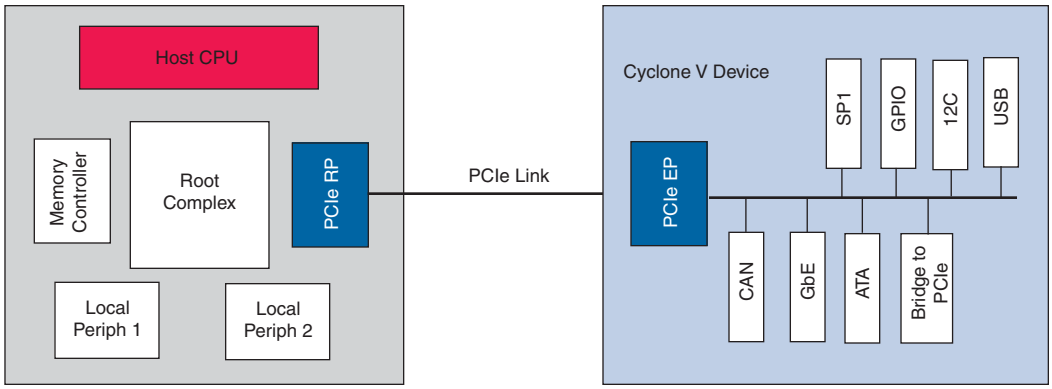
Table 6. External Memory Interface Performance (Part 2 of 2)

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)
DDRII+ SRAM	—	—	333
LPDDR2 SDRAM	—	333	300
LPDDR SDRAM	—	200	200

PCIe Gen1 and Gen2 Hard IP

Cyclone V devices have PCIe hard IP designed for performance, ease-of-use, and increased functionality. The PCIe hard IP consists of the PCS, data link, and transaction layers. It supports Gen2 end point and root port (×1 and ×2 lanes configuration) and Gen1 end point and root port up to ×4 lane configuration. PCIe endpoint support includes multifunction support for up to eight functions, as shown in Figure 2. The integrated multifunction support reduces the FPGA logic requirements by up to 20 KLEs for PCIe designs needing multiple peripherals.

Figure 2. PCIe Multifunction



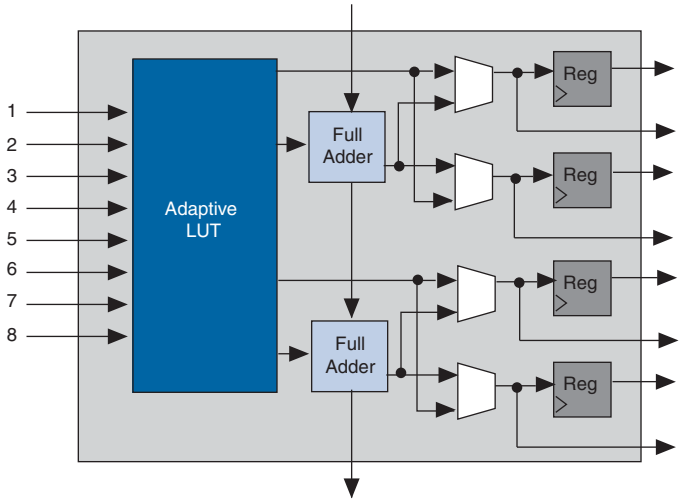
The Cyclone V PCIe hard IP operates independently from the core logic that allows the PCIe link to wake up and complete link training in less than 100 ms while the Cyclone V device completes loading the programming file for the rest of the device. In addition, the Cyclone V device PCIe hard IP has improved end-to-end data path protection using ECC, as compared to the previous generation.

Adaptive Logic Module

Cyclone V devices use a new 28 nm ALM as the basic building block of the logic fabric. The ALM shown in Figure 3 uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve even higher design packing capability than previous generations.

You can configure up to 25% of the ALMs in Cyclone V devices as distributed memory (MLABs). For more information, refer to "Embedded Memory" on page 9.

Figure 3. Cyclone V Device ALM



Variable Precision DSP Block

The variable precision DSP block is adaptable to meet a wide range of application requirements, including support for different multiplier precision widths and integrating features to improve performance of common functions such as FIR filters. Because FPGAs implement DSP processing in parallel, higher performance is achieved at all bit precision levels (9- through 27-bits or higher) when compared to stand-alone DSP ASSPs. This flexibility results in increased system performance, reduced power consumption, and reduced architecture constraints on system algorithm designers.

Cyclone V devices feature a variable precision DSP block that you can configure to natively support signal processing with precision ranging from 9 × 9, 18 × 19, and 27 × 27 bits.

You can independently configure each DSP block at compile time as three 9 × 9s, two 18 × 19s, or a single 27 × 27 multiply. With a dedicated 64-bit cascade bus, you can cascade multiple variable precision DSP blocks to implement even higher precision DSP functions efficiently. Table 7 lists how different precision is accommodated within a DSP block or by using multiple blocks.

Table 7. Variable Precision DSP Block Configurations

Multiplier Size (Bit)	DSP Block Resources	Expected Usage
Three 9 × 9	1 variable precision DSP block	Low precision fixed point for video applications
Two 18 × 19	1 variable precision DSP block	Medium precision fixed point in FIR filters
Two 18 × 19 with accumulate	1 variable precision DSP block	FIR filters and general DSP usage
27 × 27 with accumulate	1 variable precision DSP block	High precision fixed-point or floating-point implementations

Table 8 lists the resource counts by bit precision.

Table 8. Resource Counts by Bit Precision

Family	Devices	27×27	18×19	9×9
Cyclone V E	5CEA2	39	78	117
	5CEA5	78	156	234
	5CEA8	132	264	396
	5CEB5	220	440	660
	5CEB9	406	812	1,218
Cyclone V GX	5CGXC3	40	80	120
	5CGXC4	70	140	210
	5CGXC5	132	264	396
	5CGXC7	220	440	660
	5CGXC9	406	812	1,218
Cyclone V GT	5CGTD3	132	264	396
	5CGTD5	220	440	660
	5CGTD8	406	812	1,218

Other new variable precision DSP block features include:

- 64-bit accumulator, the largest in the industry
- Hard pre-adder, available in both 18- and 27-bit modes. The 18 × 19 multiplier allows use of 18-bit data with the pre-adder in 18-bit and 27-bit modes.
- Cascaded output adders, for efficient systolic FIR filters
- Internal coefficient register banks, 8 deep, for each multiplier in 18-bit or 27-bit mode
- Fully independent multiplier operation
- Second accumulator feedback register to accommodate complex multiply-accumulate functions
- Efficient support for single- and double-precision floating point arithmetic
- Inferability of all modes by the Quartus II design software

Embedded Memory

The Cyclone V embedded memories were designed to provide an optimal amount of small- and large-sized memory arrays. Cyclone V devices contain two types of embedded memory blocks: MLAB (640 bit) and M10K (10 Kbit).

- MLAB blocks—Ideal for wide and shallow memory arrays (number of ports)
- M10K blocks—Ideal for larger memory arrays while still providing a large number of independent ports

The M10K embedded memory operates up to 380 MHz, while the MLAB operates up to 300 MHz. These memory blocks are flexible and support a number of memory configurations, as shown in Table 9.

Table 9. Embedded Memory Block Configuration

MLAB (Bits)	M10K (Bits)
32 × 1, 2, 4, 8, 9, 10, 16, 18, or 20	256 × 40 or 32
	512 × 20 or 16
	1K × 10 or 8
	2K × 5 or 4
	4K × 2
	8K × 1

Partial and Dynamic Reconfiguration

Dynamic reconfiguration enables transceiver data rates or encoding schemes to be changed dynamically while maintaining data transfer on adjacent transceiver channels in Cyclone V devices. Dynamic reconfiguration is ideal for applications requiring on-the-fly multi-protocol or multi-rate support. You can reconfigure the PMA and PCS blocks with dynamic reconfiguration.

Partial reconfiguration allows you to reconfigure part of the device while other sections remain running. This is required in systems where uptime is critical because it allows you to make updates or adjust functionality without disrupting services. While lowering power and cost, partial reconfiguration also increases the effective logic density because device functions that do not operate simultaneously do not need to be uploaded into the FPGA. Instead, you can store these functions in external memory and load them as required. This reduces the size of the device by allowing multiple applications on a single device, potentially saving board space and reducing power.

To date, partial reconfiguration solutions have been time-intensive tasks that required you to know all of the intricate device architecture details. Altera is simplifying the partial reconfiguration process by building the capability on top of the proven incremental compile design flow in its Quartus II design software.

Partial reconfiguration is supported through the FPP ×16 I/O or CvP interfaces. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable partial reconfiguration of both core and I/O simultaneously.

PLL Clock Sources

Cyclone V devices have up to 8 PLLs, each with nine outputs that you can use to reduce the number of oscillators required on your board, as well as reduce the clock pins used in the device by synthesizing multiple clock frequencies from a single reference clock source. You can use the PLLs for frequency synthesis, on-chip clock de-skew, jitter attenuation, dynamic phase-shift, zero delay buffer, counters reconfiguration, bandwidth reconfiguration, programmable output clock duty cycle, PLL cascading, and reference clock switch-over.

Cyclone V devices use a fractional PLL architecture in addition to the historical integer PLL. When you use a fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis. This eliminates the need for off-chip reference clock sources.

Cyclone V devices support the following features:

- Bandwidth and user-mode reconfiguration of PLLs
- Reference clock switchover
- Dynamic phase shift
- Direct, source synchronous, zero delay buffer, external feedback, and LVDS compensation

Clock Networks

The Cyclone V device clock network architecture is based on Altera's proven global, quadrant, and peripheral clock structure, which is supported by dual function GPIO clock input pins and PLLs. Cyclone V devices have 16 global clock networks capable of up to 625 MHz operation. The Quartus® II software identifies all unused sections of the clock network and powers them down, which reduces power consumption.

Enhanced Configuration and Configuration via Protocol

Cyclone V devices support the following configuration modes:

- Active Serial (AS) ×1 and ×4 mode (serial configuration device [EPCS])
- Passive Serial (PS) configuration ×1 through CPLD/external uC (3-chip)
- Fast Passive Parallel (FPP) configuration ×8 and ×16 data widths
- Configuration through JTAG
- Configuration via Protocol (CvP)
- Configuration via commodity parallel flash (PFL)

Cyclone V supports 3.3 V programming voltage for all configuration modes.

You can now configure Cyclone V devices through PCIe with CvP instead of an external flash or ROM. CvP offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. Cyclone V CvP meets the PCIe 100 ms power-up-to-active time requirement.

Table 10 lists the configuration modes that Cyclone V devices support.

Table 10. Cyclone V Device Configuration Modes (Part 1 of 2)

Mode	Compression	Encryption	Remote Update	Data Width	Maximum Clock Rate (MHz)	Maximum Data Rate (Mbps)
Active Serial	✓	✓	✓	1, 4	80	—
Passive Serial	✓	✓	—	1	125	125
Fast Passive Parallel	✓	✓	Parallel flash loader	8, 16	125, 125	—
CvP	—	✓	✓	1, 2, 4, 8	—	—

Table 10. Cyclone V Device Configuration Modes (Part 2 of 2)

Mode	Compression	Encryption	Remote Update	Data Width	Maximum Clock Rate (MHz)	Maximum Data Rate (Mbps)
Partial Reconfiguration	—	✓	✓	16	125	—
JTAG	—	—	—	1	33	33

Document Revision History

Table 11 lists the revision history for this advance information brief.

Table 11. Document Revision History

Date	Version	Changes
May 2011	1.2	Updated variable precision DSP information and PLL clock sources information.
March 2011	1.1	Changed CvPCIe to CvP.
January 2011	1.0	Initial release.