Pin Information for the Stratix® IV GT EP4S40G5 Device
Version 1.1
Note (1)

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
1A		TDI		TDI			J29			
1A		TMS		TMS			N27			
1A		TRST		TRST			A32			
1A		TCK		TCK			G30			
1A		TDO		TDO			F30			
1A	VREFB1AN0	IO			DIFFIO_TX_L1n	DIFFOUT_L1n	K29			
1A	VREFB1AN0	IO			DIFFIO_TX_L1p	DIFFOUT_L1p	L29			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	C34			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D34			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J30	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	K30	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	C31	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	D31	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	M28	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	N28	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	H32	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	J32	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	B32	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	C32	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	M31	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	N31	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	C33	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	D33	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	M30	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	N30	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	G31	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	H31	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	M29	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	N29	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	E31	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	F31	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	K31	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L31	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	E32	DQSn5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	F32	DQS5L	DQ3L/CQn3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	R28	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	T28	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	E34	DQSn6L	DQSn3L/DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	F34	DQS6L	DQS3L/CQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	R27	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	T27	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	J33	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	K32	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	F33	DQSn7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	G33	DQS7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	P29	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	R29	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	H34			
1C	VREFB1CN0	IO			DIFFIO_TX_L19n	DIFFOUT_L37n	L32	DQ12L	DQ12L	DQ12L
1C	VREFB1CN0	IO			DIFFIO_TX_L19p	DIFFOUT_L37p	M32	DQ12L	DQ12L	DQ12L
1C	VREFB1CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L39n	P32	DQ12L	DQ12L	DQ12L
1C	VREFB1CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L39p	P31	DQ12L	DQ12L	DQ12L

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
1C	VREFB1CN0	IO			DIFFIO_TX_L21p	DIFFOUT_L41p	T30	DQ13L	DQ12L	DQ12L
1C	VREFB1CN0	IO			DIFFIO_RX_L21n	DIFFOUT_L42n	N34	DQ13L	DQ12L	DQ12L
1C	VREFB1CN0	IO			DIFFIO_RX_L21p	DIFFOUT_L42p	N33	DQ13L	DQ12L	DQ12L
1C	VREFB1CN0	IO			DIFFIO_RX_L22n	DIFFOUT_L44n	M34	DQSn14L	DQ13L	DQSn12L/DQ12L
1C	VREFB1CN0	IO			DIFFIO_RX_L22p	DIFFOUT_L44p	M33	DQS14L	DQ13L/CQn13L	DQS12L/CQ12L
1C	VREFB1CN0	IO			DIFFIO_TX_L23n	DIFFOUT_L45n	V28	DQ14L	DQ13L	DQ12L
1C	VREFB1CN0	IO			DIFFIO_TX_L23p	DIFFOUT_L45p	W28	DQ14L	DQ13L	DQ12L
1C	VREFB1CN0	IO			DIFFIO_RX_L23p	DIFFOUT_L46p	L34	DQS15L	DQS13L/CQ13L	DQ12L
1C	VREFB1CN0	CLKUSR		CLKUSR			R31			
1C	VREFB1CN0	IO			DIFFIO_TX_L24p	DIFFOUT_L47p	R30	DQ15L	DQ13L	DQ12L
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L25n	DIFFOUT_L49n	W30	DQ16L	DQ14L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L25p	DIFFOUT_L49p	W29	DQ16L	DQ14L	
1C	VREFB1CN0	DATA2		DATA2			N35			
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L25p	DIFFOUT_L50p	P34	DQS16L	DQ14L/CQn14L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L26n	DIFFOUT_L51n	V27	DQ16L	DQ14L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L26p	DIFFOUT_L51p	W26	DQ16L	DQ14L	
1C	VREFB1CN0	DATA6		DATA6			R35			
1C	VREFB1CN0	DATA7		DATA7			R34			
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L27n	DIFFOUT_L53n	V30	DQ17L	DQ14L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L27p	DIFFOUT_L53p	V29	DQ17L	DQ14L	
1C	VREFB1CN0	DEV_OE		DEV_OE			U35			
1C	VREFB1CN0	DEV_CLRn		DEV_CLRn			V34			
1C	VREFB1CN0	CLK1n	CLK1n				J34			
1C	VREFB1CN0	CLK1p	CLK1p				K34			
2C	VREFB2CN0	CLK3p	CLK3p				AJ34			
2C	VREFB2CN0	CLK3n	CLK3n				AH34			
2C	VREFB2CN0	IO			DIFFIO_TX_L30p	DIFFOUT_L60p	AB30	DQ18L	DQ21L	
2C	VREFB2CN0	IO			DIFFIO_TX_L31p	DIFFOUT_L62p	AB27	DQ19L	DQ21L	
2C	VREFB2CN0	IO			DIFFIO_TX_L31n	DIFFOUT_L62n	AB28	DQ19L	DQ21L	
2C	VREFB2CN0	IO			DIFFIO_TX_L32p	DIFFOUT_L64p	AC28	DQ19L	DQ21L	
2C	VREFB2CN0	IO			DIFFIO_TX_L32n	DIFFOUT_L64n	AC29	DQ19L	DQ21L	
2C	VREFB2CN0	IO			DIFFIO_RX_L33p	DIFFOUT_L65p	AK34	DQ20L	DQ22L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_RX_L34p	DIFFOUT_L67p	AL34	DQS20L	DQS22L/CQ22L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_TX_L34p	DIFFOUT_L68p	AD28	DQ21L	DQ22L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_TX_L34n	DIFFOUT_L68n	AD29	DQ21L	DQ22L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_RX_L35p	DIFFOUT_L69p	AH32	DQS21L	DQ22L/CQn22L	DQS23L/CQ23L
2C	VREFB2CN0	IO			DIFFIO_RX_L35n	DIFFOUT_L69n	AH33	DQSn21L	DQ22L	DQSn23L/DQ23L
2C	VREFB2CN0	IO			DIFFIO_TX_L35p	DIFFOUT_L70p	AE28	DQ21L	DQ22L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_TX_L35n	DIFFOUT_L70n	AE29	DQ21L	DQ22L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_RX_L36p	DIFFOUT_L71p	AN34	DQ22L	DQ23L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_TX_L36p	DIFFOUT_L72p	AD30	DQ22L	DQ23L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_RX_L37p	DIFFOUT_L73p	AM34	DQS22L	DQS23L/CQ23L	DQ23L/CQn23L
2C	VREFB2CN0	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	AF29	DQ23L	DQ23L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	AG30	DQ23L	DQ23L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_RX_L38p	DIFFOUT_L75p	AJ32	DQS23L	DQ23L/CQn23L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AK33	DQSn23L	DQ23L	DQ23L
2C	VREFB2CN0	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	AE30	DQ23L	DQ23L	DQ23L
2A	VREFB2AN0	IO			DIFFIO_RX_L45p	DIFFOUT_L89p	AN32			
2A	VREFB2AN0	IO			DIFFIO_RX_L45n	DIFFOUT_L89n	AP33			
2A	VREFB2AN0	IO			DIFFIO_TX_L45p	DIFFOUT_L90p	AC26	DQ28L		
2A	VREFB2AN0	IO			DIFFIO_TX_L45n	DIFFOUT_L90n	AD26	DQ28L		
2A	VREFB2AN0	IO			DIFFIO_RX_L46p	DIFFOUT_L91p	AN33	DQS28L		

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
2A	VREFB2AN0	IO			DIFFIO_RX_L46n	DIFFOUT_L91n	AP34	DQSn28L		
2A	VREFB2AN0	IO			DIFFIO_TX_L46p	DIFFOUT_L92p	AD27	DQ28L		
2A	VREFB2AN0	IO			DIFFIO_TX_L46n	DIFFOUT_L92n	AE27	DQ28L		
2A	VREFB2AN0	IO			DIFFIO_RX_L47p	DIFFOUT_L93p	AT34	DQ29L	DQ32L	
2A	VREFB2AN0	IO			DIFFIO_RX_L47n	DIFFOUT_L93n	AR34	DQ29L	DQ32L	
2A	VREFB2AN0	IO			DIFFIO_TX_L47p	DIFFOUT_L94p	AJ31	DQ29L	DQ32L	
2A	VREFB2AN0	IO			DIFFIO_TX_L47n	DIFFOUT_L94n	AH30	DQ29L	DQ32L	
2A	VREFB2AN0	IO			DIFFIO_RX_L48p	DIFFOUT_L95p	AT33	DQS29L	DQS32L/CQ32L	
2A	VREFB2AN0	IO			DIFFIO_RX_L48n	DIFFOUT_L95n	AU33	DQSn29L	DQSn32L/DQ32L	
2A	VREFB2AN0	IO			DIFFIO_TX_L48p	DIFFOUT_L96p	AK32	DQ30L	DQ32L	
2A	VREFB2AN0	IO			DIFFIO_TX_L48n	DIFFOUT_L96n	AL32	DQ30L	DQ32L	
2A	VREFB2AN0	IO			DIFFIO_TX_L49p	DIFFOUT_L98p	AG29	DQ30L	DQ32L	
2A	VREFB2AN0	IO			DIFFIO_TX_L49n	DIFFOUT_L98n	AH29	DQ30L	DQ32L	
2A	VREFB2AN0	IO			DIFFIO_RX_L50p	DIFFOUT_L99p	AP32	DQ31L	DQ33L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_RX_L50n	DIFFOUT_L99n	AR32	DQ31L	DQ33L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L50p	DIFFOUT_L100p	AK31	DQ31L	DQ33L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L50n	DIFFOUT_L100n	AL31	DQ31L	DQ33L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_RX_L51p	DIFFOUT_L101p	AN30	DQS31L	DQS33L/CQ33L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_RX_L51n	DIFFOUT_L101n	AP30	DQSn31L	DQSn33L/DQ33L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L51p	DIFFOUT_L102p	AE26	DQ32L	DQ33L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L51n	DIFFOUT_L102n	AF26	DQ32L	DQ33L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_RX_L52p	DIFFOUT_L103p	AM31	DQS32L	DQ33L/CQn33L	DQS34L/CQ34L
2A	VREFB2AN0	IO			DIFFIO_RX_L52n	DIFFOUT_L103n	AN31	DQSn32L	DQ33L	DQSn34L/DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L52p	DIFFOUT_L104p	AK30	DQ32L	DQ33L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L52n	DIFFOUT_L104n	AL30	DQ32L	DQ33L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_RX_L53p	DIFFOUT_L105p	AT31	DQ33L	DQ34L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_RX_L53n	DIFFOUT_L105n	AU31	DQ33L	DQ34L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L53p	DIFFOUT_L106p	AG28	DQ33L	DQ34L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L53n	DIFFOUT_L106n	AH28	DQ33L	DQ34L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_RX_L54p	DIFFOUT_L107p	AR31	DQS33L	DQS34L/CQ34L	DQ34L/CQn34L
2A	VREFB2AN0	IO			DIFFIO_RX_L54n	DIFFOUT_L107n	AT30	DQSn33L	DQSn34L/DQ34L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L54p	DIFFOUT_L108p	AG27	DQ34L	DQ34L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L54n	DIFFOUT_L108n	AH27	DQ34L	DQ34L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_RX_L55p	DIFFOUT_L109p	AT32	DQS34L	DQ34L/CQn34L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_RX_L55n	DIFFOUT_L109n	AU32	DQSn34L	DQ34L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L55p	DIFFOUT_L110p	AL29	DQ34L	DQ34L	DQ34L
2A	VREFB2AN0	IO			DIFFIO_TX_L55n	DIFFOUT_L110n	AM29	DQ34L	DQ34L	DQ34L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L56p	DIFFOUT_L111p	AU34			
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L56n	DIFFOUT_L111n	AV34			
2A	VREFB2AN0	IO			DIFFIO_TX_L56p	DIFFOUT_L112p	AJ29			
2A	VREFB2AN0	IO			DIFFIO_TX_L56n	DIFFOUT_L112n	AK29			
		nCONFIG		nCONFIG			AW36			
		nSTATUS		nSTATUS			AW35			
		CONF_DONE		CONF_DONE			AV35			
		PORSEL		PORSEL			AP29			
		nCE		nCE			AN29			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AD25	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AE25	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AG25	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AF25	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AE24	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AK27	DQ1B	DQ1B	DQ1B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AK26	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AJ26	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AH26	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AL27	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AK25	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AJ25	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AW34	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AW33	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AW32	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AV32	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AV31	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AW31	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AW30	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AV29	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AW28	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AW27	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AW29	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AV28	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AN27	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AP27	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AN26	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AM26	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AP26	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AL25	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AR28	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AP28	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AT29	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AU29	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AU28	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AT28	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AG24			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AH24			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AU27			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AT27			
3B	VREFB3BN0	IO				DIFFOUT_B25n	AM25	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B25p	AN25	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AP24	DQSn9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AN24	DQS9B	DQ9B/CQn9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B27n	AP25	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B27p	AR25	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AU26	DQSn10B	DQSn9B/DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AT26	DQS10B	DQS9B/CQ9B	DQ9B/CQn9B
3B	VREFB3BN0	IO				DIFFOUT_B29n	AT25	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B29p	AU25	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	AW26	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	AV26	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B31n	AH22	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B31p	AE23	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	AG22	DQSn11B	DQ10B	DQSn9B/DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	AF22	DQS11B	DQ10B/CQn10B	DQS9B/CQ9B
3B	VREFB3BN0	IO				DIFFOUT_B33n	AE22	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B33p	AF23	DQ11B	DQ10B	DQ9B

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
3B	VREFB3BN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AL23	DQSn12B	DQSn10B/DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AK23	DQS12B	DQS10B/CQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B35n	AK24	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B35p	AJ22	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AJ23	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AH23	DQ12B	DQ10B	DQ9B
3C	VREFB3CN0	IO				DIFFOUT_B49n	AN23	DQ17B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B49p	AM23	DQ17B	DQ17B	
3C	VREFB3CN0	IO	RDN3C		DIFFIO_RX_B25n	DIFFOUT_B50n	AN22	DQSn17B	DQ17B	
3C	VREFB3CN0	IO	RUP3C		DIFFIO_RX_B25p	DIFFOUT_B50p	AM22	DQS17B	DQ17B/CQn17B	
3C	VREFB3CN0	IO				DIFFOUT_B51n	AL21	DQ17B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B51p	AL22	DQ17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B26n	DIFFOUT_B52n	AU24	DQSn18B	DQSn17B/DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B26p	DIFFOUT_B52p	AT24	DQS18B	DQS17B/CQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B53n	AR23	DQ18B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B53p	AP23	DQ18B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B54n	AU23	DQ18B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B54p	AT23	DQ18B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B55n	AG20	DQ19B		
3C	VREFB3CN0	IO				DIFFOUT_B55p	AD21	DQ19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B56n	AF20	DQSn19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B56p	AE20	DQS19B		
3C	VREFB3CN0	IO				DIFFOUT_B57n	AE21	DQ19B		
3C	VREFB3CN0	IO				DIFFOUT_B57p	AG21	DQ19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B58n	AW25			
3C	VREFB3CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B58p	AV25			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B59n	AJ20			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B59p	AH20			
3C	VREFB3CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B60n	AW23			
3C	VREFB3CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B60p	AV23			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B61n	AP21			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B61p	AN21			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B31n	DIFFOUT_B62n	AU22			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B31p	DIFFOUT_B62p	AT22			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B63n	AW22			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B63p	AV22			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B32n	DIFFOUT_B64n	AT21			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B32p	DIFFOUT_B64p	AR22			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B33p	DIFFOUT_B65p	AW20			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B33n	DIFFOUT_B65n	AW21			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B66p	AV19			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B66n	AW19			
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B34p	DIFFOUT_B67p	AR20			
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B34n	DIFFOUT_B67n	AT20			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B68p	AN20			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B68n	AP20			
4C	VREFB4CN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AU20			
4C	VREFB4CN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AV20			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B70p	AH18			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B70n	AH19			
4C	VREFB4CN0	IO			DIFFIO_RX_B36p	DIFFOUT_B71p	AT19			
4C	VREFB4CN0	IO			DIFFIO_RX_B36n	DIFFOUT_B71n	AU19			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
4C	VREFB4CN0	IO				DIFFOUT_B72p	AD19	DQ20B		
4C	VREFB4CN0	IO				DIFFOUT_B72n	AG19	DQ20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AE19	DQS20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AF19	DQSn20B		
4C	VREFB4CN0	IO				DIFFOUT_B74p	AG18	DQ20B		
4C	VREFB4CN0	IO				DIFFOUT_B74n	AE18	DQ20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AT18	DQ21B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AU18	DQ21B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B76p	AT17	DQ21B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B76n	AW18	DQ21B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AU17	DQS21B	DQS22B/CQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AV17	DQSn21B	DQSn22B/DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B78p	AN19	DQ22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B78n	AM19	DQ22B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AN18	DQS22B	DQ22B/CQn22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AP18	DQSn22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B80p	AR19	DQ22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B80n	AP19	DQ22B	DQ22B	
4B	VREFB4BN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AK17	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AL17	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B94p	AJ16	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B94n	AM17	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B48p	DIFFOUT_B95p	AK16	DQS27B	DQS29B/CQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B48n	DIFFOUT_B95n	AL16	DQSn27B	DQSn29B/DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B96p	AH17	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B96n	AE17	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B49p	DIFFOUT_B97p	AF17	DQS28B	DQ29B/CQn29B	DQS30B/CQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B49n	DIFFOUT_B97n	AG17	DQSn28B	DQ29B	DQSn30B/DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B98p	AH16	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B98n	AG16	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B50p	DIFFOUT_B99p	AP17	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B50n	DIFFOUT_B99n	AR17	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B100p	AN16	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B100n	AN17	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B51p	DIFFOUT_B101p	AP16	DQS29B	DQS30B/CQ30B	DQ30B/CQn30B
4B	VREFB4BN0	IO			DIFFIO_RX_B51n	DIFFOUT_B101n	AR16	DQSn29B	DQSn30B/DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B102p	AW16	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B102n	AT16	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B52p	DIFFOUT_B103p	AU16	DQS30B	DQ30B/CQn30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B52n	DIFFOUT_B103n	AV16	DQSn30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B104p	AU15	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B104n	AT15	DQ30B	DQ30B	DQ30B
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B109p	AN15			
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B109n	AP15			
4A	VREFB4AN0	IO				DIFFOUT_B110p	AE16			
4A	VREFB4AN0	IO				DIFFOUT_B110n	AF16			
4A	VREFB4AN0	IO			DIFFIO_RX_B56p	DIFFOUT_B111p	AV14	DQ33B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B56n	DIFFOUT_B111n	AW14	DQ33B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B112p	AT14	DQ33B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B112n	AU14	DQ33B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B57p	DIFFOUT_B113p	AV13	DQS33B	DQS36B/CQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B57n	DIFFOUT_B113n	AW13	DQSn33B	DQSn36B/DQ36B	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
4A	VREFB4AN0	IO				DIFFOUT_B114p	AW12	DQ34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B114n	AW11	DQ34B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B115p	AU11	DQS34B	DQ36B/CQn36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B115n	AV11	DQSn34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B116p	AT12	DQ34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B116n	AU12	DQ34B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B117p	AP14	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B117n	AR14	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118p	AP13	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118n	AN14	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60p	DIFFOUT_B119p	AR13	DQS35B	DQS37B/CQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60n	DIFFOUT_B119n	AT13	DQSn35B	DQSn37B/DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120p	AN13	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120n	AL15	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61p	DIFFOUT_B121p	AL13	DQS36B	DQ37B/CQn37B	DQS38B/CQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61n	DIFFOUT_B121n	AM13	DQSn36B	DQ37B	DQSn38B/DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122p	AL14	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122n	AM14	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B123p	AJ13	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B123n	AK13	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124p	AH13	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124n	AK14	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B125p	AH14	DQS37B	DQS38B/CQ38B	DQ38B/CQn38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B125n	AJ14	DQSn37B	DQSn38B/DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126p	AG14	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126n	AG15	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B64p	DIFFOUT_B127p	AE14	DQS38B	DQ38B/CQn38B	DQ38B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B64n	DIFFOUT_B127n	AF14	DQSn38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128p	AD15	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128n	AE15	DQ38B	DQ38B	DQ38B
		nIO_PULLUP		nIO_PULLUP			AM11			
		nCEO		nCEO			AT11			
		DCLK		DCLK			AR11			
		nCSO		nCSO			AP11			
		ASDO		ASDO			AN11			
5A	VREFB5AN0	IO			DIFFIO_TX_R1n	DIFFOUT_R1n	AM10			
5A	VREFB5AN0	IO			DIFFIO_TX_R1p	DIFFOUT_R1p	AL10			
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AW7			
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AV7			
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AP10	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AN10	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AW8	DQSn1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AV8	DQS1R	DQ1R/CQn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	AJ11	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	AH11	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AU10	DQSn2R	DQSn1R/DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AT10	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AH12	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	AG12	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AW10	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AV10	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	AG13	DQ3R	DQ2R	DQ1R

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	AF13	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AU9	DQSn3R	DQ2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AT9	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	AP9	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	AN9	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AU8	DQSn4R	DQSn2R/DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	AT8	DQS4R	DQS2R/CQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	AP7	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	AN7	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	AR8	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	AP8	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	AL9	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	AK9	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	AU7	DQSn5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	AT7	DQS5R	DQ3R/CQn3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	AM8	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	AL8	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	AU6	DQSn6R	DQSn3R/DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	AT6	DQS6R	DQS3R/CQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	AJ10	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	AH10	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	AW4	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	AV5	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	AE12	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	AE13	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	AD12	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	AD13	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	AW5			
5A	VREFB5AN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	AW6			
5C	VREFB5CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R37n	AH8	DQ12R	DQ12R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R37p	AH9	DQ12R	DQ12R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R38p	AP6	DQS12R	DQ12R/CQn12R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	AK7	DQ12R	DQ12R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	AK8	DQ12R	DQ12R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R40p	AM6	DQS13R	DQS12R/CQ12R	DQ12R/CQn12R
5C	VREFB5CN0	IO			DIFFIO_TX_R21n	DIFFOUT_R41n	AE10	DQ13R	DQ12R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_TX_R21p	DIFFOUT_R41p	AE11	DQ13R	DQ12R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_RX_R21p	DIFFOUT_R42p	AN6	DQ13R	DQ12R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_TX_R22n	DIFFOUT_R43n	AF10	DQ14R	DQ13R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_TX_R22p	DIFFOUT_R43p	AF11	DQ14R	DQ13R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_RX_R22p	DIFFOUT_R44p	AL6	DQS14R	DQ13R/CQn13R	DQS12R/CQ12R
5C	VREFB5CN0	IO			DIFFIO_TX_R23p	DIFFOUT_R45p	AG10	DQ14R	DQ13R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_RX_R23p	DIFFOUT_R46p	AK6	DQS15R	DQS13R/CQ13R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R47p	AD10	DQ15R	DQ13R	DQ12R
5C	VREFB5CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R51n	AB10	DQ16R	DQ14R	
5C	VREFB5CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R51p	AB11	DQ16R	DQ14R	
5C	VREFB5CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R53n	AB12	DQ17R	DQ14R	
5C	VREFB5CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R53p	AB13	DQ17R	DQ14R	
5C	VREFB5CN0	IO	PLL_R3_CLKOUT0n		DIFFIO_TX_R28n	DIFFOUT_R55n	AC10			
5C	VREFB5CN0	IO	PLL_R3_FB_CLKOUT0p		DIFFIO_TX_R28p	DIFFOUT_R55p	AC11			
5C	VREFB5CN0	CLK8n	CLK8n				AH6			
5C	VREFB5CN0	CLK8p	CLK8p				AJ6			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
6C	VREFB6CN0	CLK10p	CLK10p				P6			
6C	VREFB6CN0	CLK10n	CLK10n				N6			
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R29p	DIFFOUT_R58p	W12			
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R29n	DIFFOUT_R58n	W11			
6C	VREFB6CN0	IO			DIFFIO_TX_R30p	DIFFOUT_R60p	V12	DQ18R	DQ21R	
6C	VREFB6CN0	IO			DIFFIO_TX_R30n	DIFFOUT_R60n	V11	DQ18R	DQ21R	
6C	VREFB6CN0	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	U10	DQ19R	DQ21R	
6C	VREFB6CN0	IO			DIFFIO_TX_R32p	DIFFOUT_R64p	V10	DQ19R	DQ21R	
6C	VREFB6CN0	IO			DIFFIO_TX_R33p	DIFFOUT_R66p	N9	DQ20R	DQ22R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_TX_R33n	DIFFOUT_R66n	P8	DQ20R	DQ22R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_TX_R34p	DIFFOUT_R68p	T10	DQ21R	DQ22R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_TX_R34n	DIFFOUT_R68n	R10	DQ21R	DQ22R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_RX_R35p	DIFFOUT_R69p	M6	DQS21R	DQ22R/CQn22R	DQS23R/CQ23R
6C	VREFB6CN0	IO			DIFFIO_RX_R36p	DIFFOUT_R71p	N8	DQ22R	DQ23R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_RX_R36n	DIFFOUT_R71n	N7	DQ22R	DQ23R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_TX_R36p	DIFFOUT_R72p	M8	DQ22R	DQ23R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_TX_R36n	DIFFOUT_R72n	M7	DQ22R	DQ23R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	K6	DQS22R	DQS23R/CQ23R	DQ23R/CQn23R
6C	VREFB6CN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	L8	DQ23R	DQ23R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	L7	DQ23R	DQ23R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	J6	DQS23R	DQ23R/CQn23R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	K7	DQ23R	DQ23R	DQ23R
6C	VREFB6CN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	J7	DQ23R	DQ23R	DQ23R
6A	VREFB6AN0	IO			DIFFIO_RX_R45p	DIFFOUT_R89p	G8			
6A	VREFB6AN0	IO			DIFFIO_RX_R45n	DIFFOUT_R89n	F8			
6A	VREFB6AN0	IO			DIFFIO_TX_R45p	DIFFOUT_R90p	T13	DQ28R		
6A	VREFB6AN0	IO			DIFFIO_TX_R45n	DIFFOUT_R90n	T12	DQ28R		
6A	VREFB6AN0	IO			DIFFIO_RX_R46p	DIFFOUT_R91p	F7	DQS28R		
6A	VREFB6AN0	IO			DIFFIO_RX_R46n	DIFFOUT_R91n	E7	DQSn28R		
6A	VREFB6AN0	IO			DIFFIO_TX_R46p	DIFFOUT_R92p	H7	DQ28R		
6A	VREFB6AN0	IO			DIFFIO_TX_R46n	DIFFOUT_R92n	G7	DQ28R		
6A	VREFB6AN0	IO			DIFFIO_TX_R47p	DIFFOUT_R94p	R13	DQ29R	DQ32R	
6A	VREFB6AN0	IO			DIFFIO_TX_R47n	DIFFOUT_R94n	P13	DQ29R	DQ32R	
6A	VREFB6AN0	IO			DIFFIO_RX_R48p	DIFFOUT_R95p	G6	DQS29R	DQS32R/CQ32R	
6A	VREFB6AN0	IO			DIFFIO_RX_R48n	DIFFOUT_R95n	F6	DQSn29R	DQSn32R/DQ32R	
6A	VREFB6AN0	IO			DIFFIO_TX_R48p	DIFFOUT_R96p	R12	DQ30R	DQ32R	
6A	VREFB6AN0	IO			DIFFIO_TX_R48n	DIFFOUT_R96n	R11	DQ30R	DQ32R	
6A	VREFB6AN0	IO			DIFFIO_RX_R49p	DIFFOUT_R97p	G9	DQS30R	DQ32R/CQn32R	
6A	VREFB6AN0	IO			DIFFIO_RX_R49n	DIFFOUT_R97n	F9	DQSn30R	DQ32R	
6A	VREFB6AN0	IO			DIFFIO_TX_R49p	DIFFOUT_R98p	N11	DQ30R	DQ32R	
6A	VREFB6AN0	IO			DIFFIO_TX_R49n	DIFFOUT_R98n	N10	DQ30R	DQ32R	
6A	VREFB6AN0	IO			DIFFIO_RX_R50p	DIFFOUT_R99p	F10	DQ31R	DQ33R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_RX_R50n	DIFFOUT_R99n	E10	DQ31R	DQ33R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R50p	DIFFOUT_R100p	M10	DQ31R	DQ33R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R50n	DIFFOUT_R100n	L10	DQ31R	DQ33R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_RX_R51p	DIFFOUT_R101p	D7	DQS31R	DQS33R/CQ33R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_RX_R51n	DIFFOUT_R101n	C7	DQSn31R	DQSn33R/DQ33R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R51p	DIFFOUT_R102p	K9	DQ32R	DQ33R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R51n	DIFFOUT_R102n	J9	DQ32R	DQ33R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_RX_R52p	DIFFOUT_R103p	D8	DQS32R	DQ33R/CQn33R	DQS34R/CQ34R
6A	VREFB6AN0	IO			DIFFIO_RX_R52n	DIFFOUT_R103n	C8	DQSn32R	DQ33R	DQSn34R/DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R52p	DIFFOUT_R104p	K8	DQ32R	DQ33R	DQ34R

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
6A	VREFB6AN0	IO			DIFFIO_TX_R52n	DIFFOUT_R104n	J8	DQ32R	DQ33R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_RX_R53p	DIFFOUT_R105p	D9	DQ33R	DQ34R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_RX_R53n	DIFFOUT_R105n	C9	DQ33R	DQ34R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R53p	DIFFOUT_R106p	M11	DQ33R	DQ34R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R53n	DIFFOUT_R106n	L11	DQ33R	DQ34R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R54p	DIFFOUT_R108p	N12	DQ34R	DQ34R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R54n	DIFFOUT_R108n	M12	DQ34R	DQ34R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_RX_R55p	DIFFOUT_R109p	D10	DQS34R	DQ34R/CQn34R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_RX_R55n	DIFFOUT_R109n	C10	DQSn34R	DQ34R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R55p	DIFFOUT_R110p	K10	DQ34R	DQ34R	DQ34R
6A	VREFB6AN0	IO			DIFFIO_TX_R55n	DIFFOUT_R110n	J10	DQ34R	DQ34R	DQ34R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R56p	DIFFOUT_R111p	D6			
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R56n	DIFFOUT_R111n	C6			
6A	VREFB6AN0	IO			DIFFIO_TX_R56p	DIFFOUT_R112p	H10			
6A	VREFB6AN0	IO			DIFFIO_TX_R56n	DIFFOUT_R112n	G10			
		MSEL2		MSEL2			A8			
		MSEL1		MSEL1			H11			
		MSEL0		MSEL0			J11			
7A	VREFB7AN0	IO				DIFFOUT_T1n	M13	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	N13	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	N14	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	P14	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	N15	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	R14	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	K13	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	L13	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	K12	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	M14	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	K14	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	L14	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	J13	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	J12	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	G13	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	H13	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	G14	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	H14	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	E13	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	F13	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	D13	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	F12	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	E14	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	F14	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	C11	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	A10	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	A11	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	B11	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	B10	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	D11	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	C14	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	D14	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	C13	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	C12	DQ6T	DQ3T	

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	A13	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	B13	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	J15			
7A	VREFB7AN0	IO				DIFFOUT_T19p	K15			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	A14			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	B14			
7B	VREFB7BN0	IO				DIFFOUT_T25n	G15	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T25p	E16	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	F16	DQSn9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	G16	DQS9T	DQ9T/CQn9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T27n	G17	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T27p	F15	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	C15	DQSn10T	DQSn9T/DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	D15	DQS10T	DQS9T/CQ9T	DQ9T/CQn9T
7B	VREFB7BN0	IO				DIFFOUT_T29n	A16	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T29p	D16	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	B16	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	C16	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T31n	P16	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T31p	P17	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	M16	DQSn11T	DQ10T	DQSn9T/DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	N16	DQS11T	DQ10T/CQn10T	DQS9T/CQ9T
7B	VREFB7BN0	IO				DIFFOUT_T33n	N17	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T33p	M17	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	J16	DQSn12T	DQSn10T/DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	K16	DQS12T	DQS10T/CQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T35n	K17	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T35p	L16	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	H17	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	J17	DQ12T	DQ10T	DQ9T
7C	VREFB7CN0	IO				DIFFOUT_T49n	C17	DQ17T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T49p	F17	DQ17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T25n	DIFFOUT_T50n	D17	DQSn17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T25p	DIFFOUT_T50p	E17	DQS17T	DQ17T/CQn17T	
7C	VREFB7CN0	IO				DIFFOUT_T51n	C18	DQ17T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T51p	D18	DQ17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T26n	DIFFOUT_T52n	F18	DQSn18T	DQSn17T/DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T26p	DIFFOUT_T52p	G18	DQS18T	DQS17T/CQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T53n	G20	DQ18T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T53p	F20	DQ18T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T54n	F19	DQ18T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T54p	G19	DQ18T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T55n	R18	DQ19T		
7C	VREFB7CN0	IO				DIFFOUT_T55p	J18	DQ19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T56n	A17	DQSn19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T56p	B17	DQS19T		
7C	VREFB7CN0	IO				DIFFOUT_T57n	H19	DQ19T		
7C	VREFB7CN0	IO				DIFFOUT_T57p	P18	DQ19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T29n	DIFFOUT_T58n	A18			
7C	VREFB7CN0	IO			DIFFIO_RX_T29p	DIFFOUT_T58p	B19			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T59n	M19			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T59p	L19			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
7C	VREFB7CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T60n	C19			
7C	VREFB7CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T60p	D19			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T61n	N19			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T61p	P19			
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T31n	DIFFOUT_T62n	C20			
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T31p	DIFFOUT_T62p	D20			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T63n	A19			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T63p	B20			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T32n	DIFFOUT_T64n	A20			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T32p	DIFFOUT_T64p	A21			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T33p	DIFFOUT_T65p	B22			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T33n	DIFFOUT_T65n	A22			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T66p	B23			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T66n	A23			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T34p	DIFFOUT_T67p	G21			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T34n	DIFFOUT_T67n	F21			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T68p	M20			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T68n	L20			
8C	VREFB8CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	D21			
8C	VREFB8CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	C22			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T70p	N20			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T70n	P20			
8C	VREFB8CN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	A25			
8C	VREFB8CN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	A24			
8C	VREFB8CN0	IO				DIFFOUT_T72p	M21	DQ20T		
8C	VREFB8CN0	IO				DIFFOUT_T72n	R20	DQ20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	D24	DQS20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	C24	DQSn20T		
8C	VREFB8CN0	IO				DIFFOUT_T74p	N21	DQ20T		
8C	VREFB8CN0	IO				DIFFOUT_T74n	M22	DQ20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	J22	DQ21T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	H22	DQ21T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T76p	G22	DQ21T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T76n	K22	DQ21T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	J23	DQS21T	DQS22T/CQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	H23	DQSn21T	DQSn22T/DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T78p	E22	DQ22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T78n	D22	DQ22T	DQ22T	
8C	VREFB8CN0	IO	RUP8C		DIFFIO_RX_T40p	DIFFOUT_T79p	E23	DQS22T	DQ22T/CQn22T	
8C	VREFB8CN0	IO	RDN8C		DIFFIO_RX_T40n	DIFFOUT_T79n	D23	DQSn22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T80p	G23	DQ22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T80n	F23	DQ22T	DQ22T	
8B	VREFB8BN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	K24	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	J24	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T94p	M24	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T94n	J25	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T48p	DIFFOUT_T95p	L23	DQS27T	DQS29T/CQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T48n	DIFFOUT_T95n	K23	DQSn27T	DQSn29T/DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T96p	N22	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T96n	M23	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T49p	DIFFOUT_T97p	P23	DQS28T	DQ29T/CQn29T	DQS30T/CQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T49n	DIFFOUT_T97n	N23	DQSn28T	DQ29T	DQSn30T/DQ30T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
8B	VREFB8BN0	IO				DIFFOUT_T98p	R22	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T98n	P22	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T50p	DIFFOUT_T99p	G24	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T50n	DIFFOUT_T99n	F24	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T100p	G25	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T100n	D25	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T51p	DIFFOUT_T101p	F25	DQS29T	DQS30T/CQ30T	DQ30T/CQn30T
8B	VREFB8BN0	IO			DIFFIO_RX_T51n	DIFFOUT_T101n	E25	DQSn29T	DQSn30T/DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T102p	C25	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T102n	B25	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T52p	DIFFOUT_T103p	C26	DQS30T	DQ30T/CQn30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T52n	DIFFOUT_T103n	B26	DQSn30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T104p	A26	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T104n	D26	DQ30T	DQ30T	DQ30T
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T109p	G26			
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T109n	F26			
8A	VREFB8AN0	IO				DIFFOUT_T110p	P24			
8A	VREFB8AN0	IO				DIFFOUT_T110n	R24			
8A	VREFB8AN0	IO			DIFFIO_RX_T56p	DIFFOUT_T111p	A28	DQ33T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T56n	DIFFOUT_T111n	A27	DQ33T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T112p	C27	DQ33T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T112n	D27	DQ33T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T57p	DIFFOUT_T113p	C28	DQS33T	DQS36T/CQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T57n	DIFFOUT_T113n	B28	DQSn33T	DQSn36T/DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T114p	B31	DQ34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T114n	A31	DQ34T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T58p	DIFFOUT_T115p	B29	DQS34T	DQ36T/CQn36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T58n	DIFFOUT_T115n	A29	DQSn34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T116p	C29	DQ34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T116n	C30	DQ34T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T117p	F28	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T117n	E28	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118p	D28	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118n	F27	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60p	DIFFOUT_T119p	E29	DQS35T	DQS37T/CQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60n	DIFFOUT_T119n	D29	DQSn35T	DQSn37T/DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120p	G27	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120n	H26	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T121p	H28	DQS36T	DQ37T/CQn37T	DQS38T/CQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T121n	G28	DQSn36T	DQ37T	DQSn38T/DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122p	J26	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122n	G29	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62p	DIFFOUT_T123p	L26	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62n	DIFFOUT_T123n	K26	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124p	L25	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124n	K28	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T125p	K27	DQS37T	DQS38T/CQ38T	DQ38T/CQn38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T125n	J27	DQSn37T	DQSn38T/DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126p	M25	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126n	N25	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T64p	DIFFOUT_T127p	P26	DQS38T	DQ38T/CQn38T	DQ38T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T64n	DIFFOUT_T127n	N26	DQSn38T	DQ38T	DQ38T

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
8A	VREFB8AN0	IO				DIFFOUT_T128p	P25	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128n	M27	DQ38T	DQ38T	DQ38T
QL3		GXB_TX_L11p					B36			
QL3		GXB_TX_L11n					B37			
QL3		GXB_RX_L11p					C38			
QL3		GXB_RX_L11n					C39			
QL3		GXB_TX_L10p					D36			
QL3		GXB_TX_L10n					D37			
QL3		GXB_RX_L10p					E38			
QL3		GXB_RX_L10n					E39			
QL3		GXB_CMUTX_L5p					F36			
QL3		GXB_CMUTX_L5n					F37			
QL3		REFCLK_L5p, GXB_CMURX_L5p					G38			
QL3		REFCLK_L5n, GXB_CMURX_L5n					G39			
QL3		GXB_CMUTX_L4p					H36			
QL3		GXB_CMUTX_L4n					H37			
QL3		REFCLK_L4p, GXB_CMURX_L4p					J38			
QL3		REFCLK_L4n, GXB_CMURX_L4n					J39			
QL3		GXB_TX_L9p					K36			
QL3		GXB_TX_L9n					K37			
QL3		GXB_RX_L9p					L38			
QL3		GXB_RX_L9n					L39			
QL3		GXB_TX_L8p					M36			
QL3		GXB_TX_L8n					M37			
QL3		GXB_RX_L8p					N38			
QL3		GXB_RX_L8n					N39			
QL2		GXB_TX_L7p					P36			
QL2		GXB_TX_L7n					P37			
QL2		GXB_RX_L7p					R38			
QL2		GXB_RX_L7n					R39			
QL2		GXB_TX_L6p					T36			
QL2		GXB_TX_L6n					T37			
QL2		GXB_RX_L6p					U38			
QL2		GXB_RX_L6n					U39			
QL2		GXB_CMUTX_L3p					V36			
QL2		GXB_CMUTX_L3n					V37			
QL2		REFCLK_L3p, GXB_CMURX_L3p					W38			
QL2		REFCLK_L3n, GXB_CMURX_L3n					W39			
QL2		GXB_CMUTX_L2p					Y36			
QL2		GXB_CMUTX_L2n					Y37			
QL2		REFCLK_L2p, GXB_CMURX_L2p					AA38			
QL2		REFCLK_L2n, GXB_CMURX_L2n					AA39			
QL2		GXB_TX_L5p					AB36			
QL2		GXB_TX_L5n					AB37			
QL2		GXB_RX_L5p					AC38			
QL2		GXB_RX_L5n					AC39			
QL2		GXB_TX_L4p					AD36			
QL2		GXB_TX_L4n					AD37			
QL2		GXB_RX_L4p					AE38			
QL2		GXB_RX_L4n					AE39			
QL1		GXB_TX_L3p					AF36			
QL1		GXB_TX_L3n					AF37			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
QL1		GXB_RX_L3p					AG38			
QL1		GXB_RX_L3n					AG39			
QL1		GXB_TX_L2p					AH36			
QL1		GXB_TX_L2n					AH37			
QL1		GXB_RX_L2p					AJ38			
QL1		GXB_RX_L2n					AJ39			
QL1		GXB_CMUTX_L1p					AK36			
QL1		GXB_CMUTX_L1n					AK37			
QL1		REFCLK_L1p, GXB_CMURX_L1p					AL38			
QL1		REFCLK_L1n, GXB_CMURX_L1n					AL39			
QL1		GXB_CMUTX_L0p					AM36			
QL1		GXB_CMUTX_L0n					AM37			
QL1		REFCLK_L0p, GXB_CMURX_L0p					AN38			
QL1		REFCLK_L0n, GXB_CMURX_L0n					AN39			
QL1		GXB_TX_L1p					AP36			
QL1		GXB_TX_L1n					AP37			
QL1		GXB_RX_L1p					AR38			
QL1		GXB_RX_L1n					AR39			
QL1		GXB_TX_L0p					AT36			
QL1		GXB_TX_L0n					AT37			
QL1		GXB_RX_L0p					AU38			
QL1		GXB_RX_L0n					AU39			
QR1		GXB_RX_R0n					AU1			
QR1		GXB_RX_R0p					AU2			
QR1		GXB_TX_R0n					AT3			
QR1		GXB_TX_R0p					AT4			
QR1		GXB_RX_R1n					AR1			
QR1		GXB_RX_R1p					AR2			
QR1		GXB_TX_R1n					AP3			
QR1		GXB_TX_R1p					AP4			
QR1		REFCLK_R0n, GXB_CMURX_R0n					AN1			
QR1		REFCLK_R0p, GXB_CMURX_R0p					AN2			
QR1		GXB_CMUTX_R0n					AM3			
QR1		GXB_CMUTX_R0p					AM4			
QR1		REFCLK_R1n, GXB_CMURX_R1n					AL1			
QR1		REFCLK_R1p, GXB_CMURX_R1p					AL2			
QR1		GXB_CMUTX_R1n					AK3			
QR1		GXB_CMUTX_R1p					AK4			
QR1		GXB_RX_R2n					AJ1			
QR1		GXB_RX_R2p					AJ2			
QR1		GXB_TX_R2n					AH3			
QR1		GXB_TX_R2p					AH4			
QR1		GXB_RX_R3n					AG1			
QR1		GXB_RX_R3p					AG2			
QR1		GXB_TX_R3n					AF3			
QR1		GXB_TX_R3p					AF4			
QR2		GXB_RX_R4n					AE1			
QR2		GXB_RX_R4p					AE2			
QR2		GXB_TX_R4n					AD3			
QR2		GXB_TX_R4p					AD4			
QR2		GXB_RX_R5n					AC1			
QR2		GXB_RX_R5p					AC2			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
QR2		GXB_TX_R5n					AB3			
QR2		GXB_TX_R5p					AB4			
QR2		REFCLK_R2n, GXB_CMURX_R2n					AA1			
QR2		REFCLK_R2p, GXB_CMURX_R2p					AA2			
QR2		GXB_CMUTX_R2n					Y3			
QR2		GXB_CMUTX_R2p					Y4			
QR2		REFCLK_R3n, GXB_CMURX_R3n					W1			
QR2		REFCLK_R3p, GXB_CMURX_R3p					W2			
QR2		GXB_CMUTX_R3n					V3			
QR2		GXB_CMUTX_R3p					V4			
QR2		GXB_RX_R6n					U1			
QR2		GXB_RX_R6p					U2			
QR2		GXB_TX_R6n					T3			
QR2		GXB_TX_R6p					T4			
QR2		GXB_RX_R7n					R1			
QR2		GXB_RX_R7p					R2			
QR2		GXB_TX_R7n					P3			
QR2		GXB_TX_R7p					P4			
QR3		GXB_RX_R8n					N1			
QR3		GXB_RX_R8p					N2			
QR3		GXB_TX_R8n					M3			
QR3		GXB_TX_R8p					M4			
QR3		GXB_RX_R9n					L1			
QR3		GXB_RX_R9p					L2			
QR3		GXB_TX_R9n					K3			
QR3		GXB_TX_R9p					K4			
QR3		REFCLK_R4n, GXB_CMURX_R4n					J1			
QR3		REFCLK_R4p, GXB_CMURX_R4p					J2			
QR3		GXB_CMUTX_R4n					H3			
QR3		GXB_CMUTX_R4p					H4			
QR3		REFCLK_R5n, GXB_CMURX_R5n					G1			
QR3		REFCLK_R5p, GXB_CMURX_R5p					G2			
QR3		GXB_CMUTX_R5n					F3			
QR3		GXB_CMUTX_R5p					F4			
QR3		GXB_RX_R10n					E1			
QR3		GXB_RX_R10p					E2			
QR3		GXB_TX_R10n					D3			
QR3		GXB_TX_R10p					D4			
QR3		GXB_RX_R11n					C1			
QR3		GXB_RX_R11p					C2			
QR3		GXB_TX_R11n					B3			
QR3		GXB_TX_R11p					B4			
		GND					F35			
		GND					G35			
		GND					H35			
		GND					J35			
		GND					AB31			
		GND					AC32			
		GND					AC31			
		GND					T31			
		GND					R33			
		GND					R32			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		GND					AL11			
		GND					W6			
		GND					W5			
		GND					W8			
		GND					R6			
		GND					R5			
		GND					V9			
		GND					R7			
		GND					V6			
		GND					U5			
		GND					N5			
		GND					J5			
		GND					R9			
		GND					R8			
		GND					K5			
		GND					G5			
		GND					F5			
		GND					D5			
		GND					C5			
		GND					Y21			
		GND					AV6			
		GND					AV9			
		GND					AV12			
		GND					AV15			
		GND					AV18			
		GND					AV21			
		GND					AV24			
		GND					AV27			
		GND					AV30			
		GND					AV33			
		GND					AR6			
		GND					AR9			
		GND					AR12			
		GND					AR15			
		GND					AR18			
		GND					AR21			
		GND					AR24			
		GND					AR27			
		GND					AR30			
		GND					AR33			
		GND					AM7			
		GND					AM9			
		GND					AM12			
		GND					AM15			
		GND					AM18			
		GND					AM21			
		GND					AM24			
		GND					AM27			
		GND					AM30			
		GND					AM33			
		GND					AJ7			
		GND					AJ9			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		GND					AJ12			
		GND					AJ15			
		GND					AJ18			
		GND					AJ21			
		GND					AJ24			
		GND					AJ27			
		GND					AJ30			
		GND					AJ33			
		GND					AF9			
		GND					AF12			
		GND					AF15			
		GND					AF18			
		GND					AF21			
		GND					AF24			
		GND					AF27			
		GND					AF30			
		GND					AD23			
		GND					AC7			
		GND					AC9			
		GND					AC12			
		GND					AC14			
		GND					AC16			
		GND					AC18			
		GND					AC20			
		GND					AC22			
		GND					AC24			
		GND					AC27			
		GND					AC30			
		GND					AC33			
		GND					AB15			
		GND					AB17			
		GND					AB19			
		GND					AB21			
		GND					AB23			
		GND					AB25			
		GND					AA14			
		GND					AA16			
		GND					AA18			
		GND					AA22			
		GND					AA24			
		GND					Y12			
		GND					Y15			
		GND					Y17			
		GND					Y19			
		GND					Y23			
		GND					Y25			
		GND					Y27			
		GND					Y30			
		GND					W10			
		GND					W14			
		GND					W16			
		GND					W18			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		GND					W20			
		GND					W22			
		GND					W24			
		GND					V15			
		GND					V17			
		GND					V19			
		GND					V21			
		GND					V23			
		GND					V25			
		GND					U9			
		GND					U12			
		GND					U14			
		GND					U16			
		GND					U18			
		GND					U20			
		GND					U22			
		GND					U24			
		GND					U26			
		GND					U28			
		GND					U30			
		GND					T15			
		GND					T17			
		GND					T19			
		GND					T21			
		GND					T23			
		GND					T25			
		GND					P7			
		GND					P9			
		GND					P12			
		GND					P15			
		GND					P21			
		GND					P27			
		GND					P30			
		GND					P33			
		GND					N18			
		GND					N24			
		GND					L6			
		GND					L9			
		GND					L12			
		GND					L15			
		GND					L18			
		GND					L21			
		GND					L24			
		GND					L27			
		GND					L30			
		GND					L33			
		GND					H6			
		GND					H9			
		GND					H12			
		GND					H15			
		GND					H18			
		GND					H21			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		GND					H24			
		GND					H27			
		GND					H30			
		GND					H33			
		GND					E6			
		GND					E9			
		GND					E12			
		GND					E15			
		GND					E18			
		GND					E21			
		GND					E24			
		GND					E27			
		GND					E30			
		GND					E33			
		GND					B9			
		GND					B12			
		GND					B15			
		GND					B18			
		GND					B21			
		GND					B24			
		GND					B27			
		GND					B30			
		GND					A38			
		GND					A37			
		GND					A36			
		GND					A35			
		GND					A33			
		GND					B39			
		GND					B38			
		GND					B35			
		GND					B34			
		GND					B33			
		GND					C37			
		GND					C36			
		GND					D39			
		GND					D38			
		GND					E37			
		GND					E36			
		GND					F39			
		GND					F38			
		GND					G37			
		GND					G36			
		GND					H39			
		GND					H38			
		GND					J37			
		GND					J36			
		GND					K39			
		GND					K38			
		GND					L37			
		GND					L36			
		GND					M39			
		GND					M38			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		GND					N37			
		GND					N36			
		GND					P39			
		GND					P38			
		GND					R37			
		GND					R36			
		GND					T39			
		GND					T38			
		GND					T34			
		GND					T32			
		GND					U37			
		GND					AW37			
		GND					AV37			
		GND					AV38			
		GND					AV39			
		GND					AU36			
		GND					AU37			
		GND					AT38			
		GND					AT39			
		GND					AR36			
		GND					AR37			
		GND					AP38			
		GND					AP39			
		GND					AN36			
		GND					AN37			
		GND					AM38			
		GND					AM39			
		GND					AL36			
		GND					AL37			
		GND					AK38			
		GND					AK39			
		GND					AJ36			
		GND					AJ37			
		GND					AH38			
		GND					AH39			
		GND					AG36			
		GND					AG37			
		GND					AF33			
		GND					AF38			
		GND					AF39			
		GND					AE36			
		GND					AE37			
		GND					AD32			
		GND					AD34			
		GND					AD38			
		GND					AD39			
		GND					AC36			
		GND					AC37			
		GND					AB33			
		GND					AB38			
		GND					AB39			
		GND					AA36			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		GND					AA37			
		GND					Y32			
		GND					Y34			
		GND					Y38			
		GND					Y39			
		GND					W36			
		GND					W37			
		GND					V33			
		GND					V38			
		GND					V39			
		GND					U36			
		GND					AR35			
		GND					AF34			
		GND					AG34			
		GND					AJ35			
		GND					AH35			
		GND					AK35			
		GND					AG31			
		GND					AG32			
		GND					AL35			
		GND					AN35			
		GND					AD31			
		GND					AM35			
		GND					AE31			
		GND					AP35			
		GND					AA35			
		GND					AB34			
		GND					AC34			
		GND					A7			
		GND					A5			
		GND					A4			
		GND					A3			
		GND					A2			
		GND					B7			
		GND					B6			
		GND					B5			
		GND					B2			
		GND					B1			
		GND					C4			
		GND					C3			
		GND					D2			
		GND					D1			
		GND					E4			
		GND					E3			
		GND					F2			
		GND					F1			
		GND					G4			
		GND					G3			
		GND					H2			
		GND					H1			
		GND					J4			
		GND					J3			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		GND					K2			
		GND					K1			
		GND					L4			
		GND					L3			
		GND					M2			
		GND					M1			
		GND					N4			
		GND					N3			
		GND					P2			
		GND					P1			
		GND					R4			
		GND					R3			
		GND					T8			
		GND					T6			
		GND					T2			
		GND					T1			
		GND					U4			
		GND					U3			
		GND					V7			
		GND					V2			
		GND					V1			
		GND					W4			
		GND					W3			
		GND					Y8			
		GND					Y6			
		GND					Y2			
		GND					Y1			
		GND					AA4			
		GND					AA3			
		GND					AB7			
		GND					AB2			
		GND					AB1			
		GND					AC4			
		GND					AC3			
		GND					AD8			
		GND					AD6			
		GND					AD2			
		GND					AD1			
		GND					AE4			
		GND					AE3			
		GND					AF7			
		GND					AF2			
		GND					AF1			
		GND					AG4			
		GND					AG3			
		GND					AH2			
		GND					AH1			
		GND					AJ4			
		GND					AJ3			
		GND					AW3			
		GND					AV1			
		GND					AV2			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		GND					AV3			
		GND					AU3			
		GND					AU4			
		GND					AT1			
		GND					AT2			
		GND					AR3			
		GND					AR4			
		GND					AP1			
		GND					AP2			
		GND					AN3			
		GND					AN4			
		GND					AM1			
		GND					AM2			
		GND					AL3			
		GND					AL4			
		GND					AK1			
		GND					AK2			
		GND					AC6			
		GND					AB6			
		GND					AA5			
		GND					AT5			
		GND					AR5			
		GND					AP5			
		GND					AM5			
		GND					AL5			
		GND					AG9			
		GND					AK5			
		GND					AD9			
		GND					AJ5			
		GND					AG7			
		GND					AG8			
		GND					AC8			
		GND					AB9			
		GND					AH5			
		GND					AG6			
		GND					AF6			
		GND					W7			
		GND					T9			
		GND					AN5			
		VCC					Y20			
		VCC					AC15			
		VCC					AC17			
		VCC					AC25			
		VCC					AB14			
		VCC					AB16			
		VCC					AB18			
		VCC					AB20			
		VCC					AB22			
		VCC					AB24			
		VCC					AA15			
		VCC					AA19			
		VCC					AA21			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		VCC					AA25			
		VCC					Y14			
		VCC					Y16			
		VCC					Y18			
		VCC					Y22			
		VCC					Y24			
		VCC					W15			
		VCC					W19			
		VCC					W21			
		VCC					W25			
		VCC					V14			
		VCC					V16			
		VCC					V18			
		VCC					V20			
		VCC					V22			
		VCC					V24			
		VCC					V26			
		VCC					U15			
		VCC					U19			
		VCC					U21			
		VCC					U25			
		VCC					T14			
		VCC					T16			
		VCC					T24			
		VCC					T26			
		VCC					T18			
		VCC					AC19			
		VCC					AC21			
		VCC					AC23			
		VCC					AA17			
		VCC					AA23			
		VCC					W17			
		VCC					W23			
		VCC					U17			
		VCC					U23			
		VCC					T20			
		VCC					T22			
		VCC					AF32			
		VCC					AE32			
		VCC					AB32			
		VCC					AA32			
		VCC					V32			
		VCC					U32			
		VCC					AF8			
		VCC					AE8			
		VCC					AB8			
		VCC					AA8			
		VCC					V8			
		VCC					U8			
		VCCPT					AA27			
		VCCPT					AA26			
		VCCPT					AM20			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		VCCPT					Y13			
		VCCPT					AA12			
		VCCPT					H20			
		DNU					AA20			
		VCCPGM					AK28			
		VCCPGM					AK12			
		TEMPDIODEn					E11			
		TEMPDIODEp					A9			
		VCC_CLKIN3C					AK21			
		VCC_CLKIN4C					AK18			
		VCC_CLKIN7C					K18			
		VCC_CLKIN8C					K21			
		VCCBAT					K11			
		VCCA_PLL_B1					AL20			
		VCCA_PLL_B2					AL19			
		VCCA_PLL_L2					Y29			
		VCCA_PLL_L3					AA29			
		VCCA_PLL_R2					Y10			
		VCCA_PLL_R3					AA10			
		VCCA_PLL_T1					J20			
		VCCA_PLL_T2					J19			
		VCCD_PLL_B1					AK20			
		VCCD_PLL_B2					AK19			
		VCCD_PLL_L2					Y28			
		VCCD_PLL_L3					AA28			
		VCCD_PLL_R2					Y11			
		VCCD_PLL_R3					AA11			
		VCCD_PLL_T1					K20			
		VCCD_PLL_T2					K19			
		VCCIO1A					J31			
		VCCIO1A					G32			
		VCCIO1A					G34			
		VCCIO1A					E35			
		VCCIO1A					D32			
		VCCIO1C					AA30			
		VCCIO1C					T29			
		VCCIO1C					N32			
		VCCIO1C					K33			
		VCCIO2A					AT35			
		VCCIO2A					AP31			
		VCCIO2A					AM32			
		VCCIO2A					AJ28			
		VCCIO2A					AG26			
		VCCIO2C					AL33			
		VCCIO2C					AH31			
		VCCIO2C					AG33			
		VCCIO2C					AF31			
		VCCIO3A					AU30			
		VCCIO3A					AR29			
		VCCIO3A					AL26			
		VCCIO3A					AH25			
		VCCIO3B					AR26			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		VCCIO3B					AG23			
		VCCIO3C					AW24			
		VCCIO3C					AK22			
		VCCIO3C					AH21			
		VCCIO4A					AU13			
		VCCIO4A					AP12			
		VCCIO4A					AK15			
		VCCIO4A					AH15			
		VCCIO4B					AW15			
		VCCIO4B					AJ17			
		VCCIO4C					AW17			
		VCCIO4C					AU21			
		VCCIO4C					AJ19			
		VCCIO5A					AW9			
		VCCIO5A					AR7			
		VCCIO5A					AR10			
		VCCIO5A					AN8			
		VCCIO5A					AK10			
		VCCIO5C					AL7			
		VCCIO5C					AJ8			
		VCCIO5C					AH7			
		VCCIO5C					AE9			
		VCCIO6A					M9			
		VCCIO6A					H8			
		VCCIO6A					E5			
		VCCIO6A					E8			
		VCCIO6A					B8			
		VCCIO6C					V13			
		VCCIO6C					T11			
		VCCIO6C					P10			
		VCCIO6C					H5			
		VCCIO7A					M15			
		VCCIO7A					J14			
		VCCIO7A					D12			
		VCCIO7A					A12			
		VCCIO7B					L17			
		VCCIO7B					A15			
		VCCIO7C					M18			
		VCCIO7C					E19			
		VCCIO7C					C21			
		VCCIO8A					M26			
		VCCIO8A					J28			
		VCCIO8A					D30			
		VCCIO8A					A30			
		VCCIO8B					K25			
		VCCIO8B					E26			
		VCCIO8C					L22			
		VCCIO8C					F22			
		VCCIO8C					C23			
		VCCPD1A					U27			
		VCCPD1C					W27			
		VCCPD2A					AB26			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		VCCPD2C					Y26			
		VCCPD3A					AD24			
		VCCPD3B					AD22			
		VCCPD3C					AD20			
		VCCPD4A					AD14			
		VCCPD4B					AD16			
		VCCPD4C					AD18			
		VCCPD5A					AC13			
		VCCPD5C					AA13			
		VCCPD6A					U13			
		VCCPD6C					W13			
		VCCPD7A					R15			
		VCCPD7B					R17			
		VCCPD7C					R19			
		VCCPD8A					R25			
		VCCPD8B					R23			
		VCCPD8C					R21			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				P28			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				U29			
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				AF28			
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				AB29			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AN28			
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AL24			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AP22			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AN12			
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AM16			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AL18			
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				AG11			
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				AD11			
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				P11			
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				U11			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G12			
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				H16			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				E20			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				F29			
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				H25			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				J21			
		NC					L28			
		NC					AM28			
		NC					AK11			
		NC					F11			
		NC					AV36			
		NC					AU35			
		NC					AU5			
		NC					AV4			
		NC					AD17			
		NC					R16			
		NC					R26			
		NC					C35			
		NC					D35			
		NC					L35			
		NC					V31			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		NC					U31			
		NC					W33			
		NC					W32			
		NC					W35			
		NC					W34			
		VCCAUX					H29			
		VCCAUX					AL28			
		VCCAUX					AL12			
		VCCAUX					G11			
		VCCA_L					M35			
		VCCA_L					AF35			
		VCCA_L					AG35			
		VCCA_L					K35			
		VCCA_R					M5			
		VCCA_R					AF5			
		VCCA_R					L5			
		VCCA_R					AG5			
		VCCH_GXBL0					AE34			
		VCCH_GXBL1					AA34			
		VCCH_GXBL2					U34			
		VCCH_GXBR0					AE6			
		VCCH_GXBR1					AA6			
		VCCH_GXBR2					U6			
		VCCL_GXBL0					AD33			
		VCCL_GXBL0					AE33			
		VCCL_GXBL1					Y33			
		VCCL_GXBL1					AA33			
		VCCL_GXBL2					T33			
		VCCL_GXBL2					U33			
		VCCL_GXBR0					AD7			
		VCCL_GXBR0					AE7			
		VCCL_GXBR1					Y7			
		VCCL_GXBR1					AA7			
		VCCL_GXBR2					T7			
		VCCL_GXBR2					U7			
		VCCR_R					T5			
		VCCR_R					Y5			
		VCCR_R					AD5			
		VCCR_R					AE5			
		VCCR_L					T35			
		VCCR_L					Y35			
		VCCR_L					AD35			
		VCCR_L					AE35			
		VCCT_R					P5			
		VCCT_R					V5			
		VCCT_R					AB5			
		VCCT_R					AC5			
		VCCT_L					P35			
		VCCT_L					V35			
		VCCT_L					AB35			
		VCCT_L					AC35			
		VCCHIP_R					W9			

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	H1517	DQS for X4 for H1517	DQS for X8/X9 for H1517	DQS for X16/ X18 for H1517
		VCCHIP_R					Y9			
		VCCHIP_R					AA9			
		VCCHIP_L					W31			
		VCCHIP_L					Y31			
		VCCHIP_L					AA31			
		RREF_L0					AW38			
		RREF_L1					A34			
		RREF_R0					AW2			
		RREF_R1					A6			

Note:
(1) If the p pin or n pin is not available, the particular differential pair is not supported.

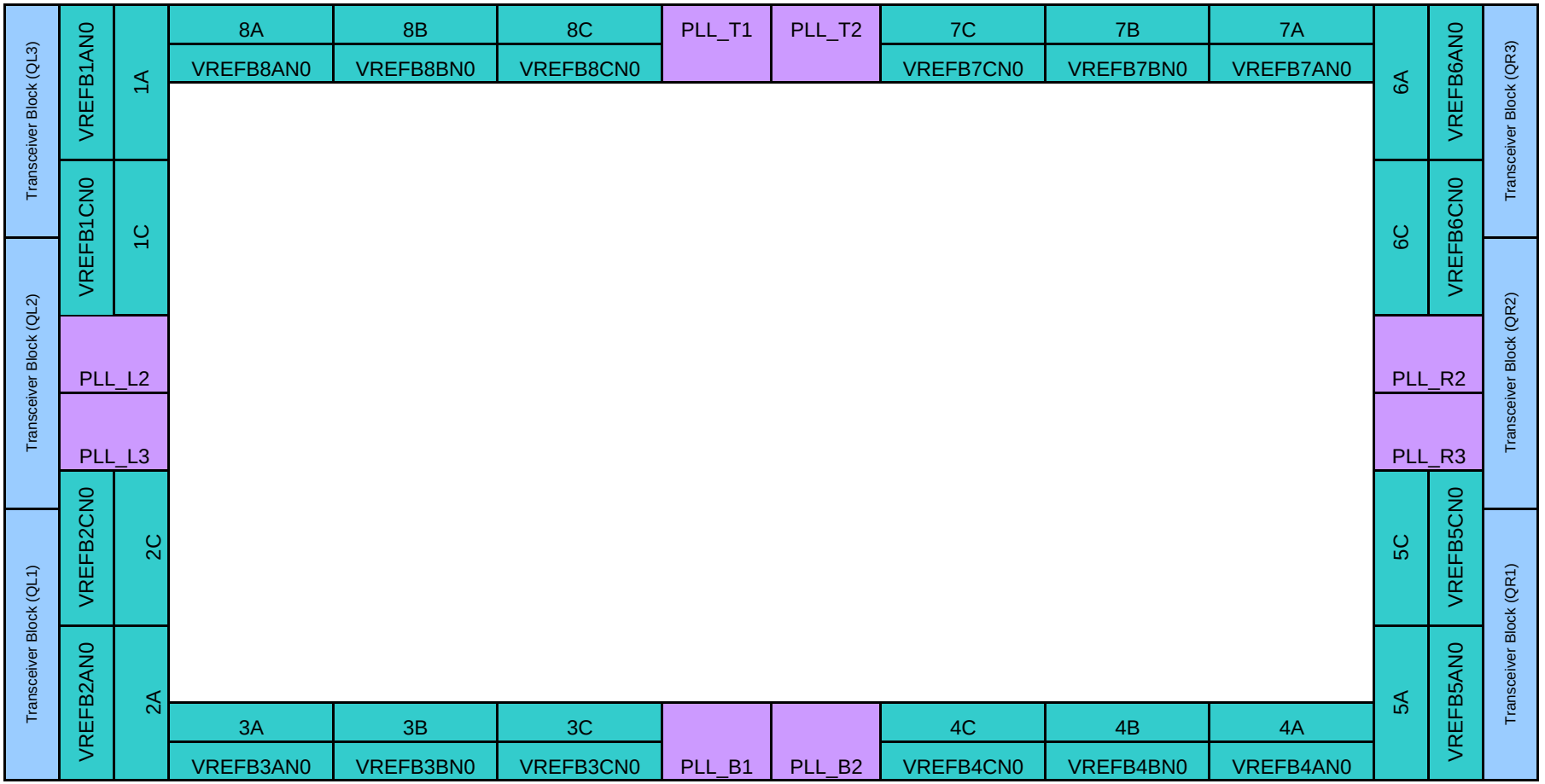
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
	Clock and PLL Pins	
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[4:7,9, 11:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L4,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L4 and R4 respectively.
PLL_[L4,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L4 and R4 respectively.
PLL_[L1, L2, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[0:7], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.
MSEL[0:2]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
TCK	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.
	Optional/Dual-Purpose Configuration Pins	
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn (Note 6)	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.
DEV_OE (Note 6)	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.
DATA0 (Note 6)	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[1:7] (Note 6)	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR (Note 6)	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
Differential I/O Pins		
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[##][T,B], DQS[##][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[##][T,B], DQSn[##][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[##][T,B], DQ[##][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[##][T,B], CQ[##][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[##][T,B], CQn[##][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
Reference Pins		
RUP[1:8]A, (Note 7) RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, (Note 7) RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCC	Power	VCC supplies power to the core and periphery.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in data sheet, even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in data sheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,C], VCCIO[2,3,4,5,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTL 3.3 V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,C], VCCPD[2,3,4,5,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
VREF[1:8][A,C]N0, VREF[2,3,4,5,7,8]BN0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.
		Transceiver (I/O Banks) Pins
VCCHIP_[L,R]	Power	PCIe Hard IP digital power supply, specific to the left (L) side or right (R) side of the device.
VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.
VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.
VCCL_GXB[L,R][0:3]	Power	Analog power, block level clock distribution.
VCCH_GXB[L,R][0:3]	Power	Analog power, block level TX buffers, specific to left (L) side and right (R) side.
VCCA_[L,R]	Power	Analog power, TX driver, RX receiver, CDR, specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]p (Note 3)	Input	High speed positive differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_RX_[L,R][0:15]n (Note 3)	Input	High speed negative differential receiver channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]p (Note 3)	Output	High speed positive differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
GXB_TX_[L,R][0:15]n (Note 3)	Output	High speed negative differential transmitter channels. Specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]p, GXB_CMURX_[L,R][0:7]p (Note 3 and 4)	Input	High speed differential reference clock positive, or CMU receiver channels, specific to the left (L) side or right (R) side of the device.
REFCLK_[L,R][0:7]n, GXB_CMURX_[L,R][0:7]n (Note 3 and 4)	Input	High speed differential reference clock complement, or CMU complementary receiver channel, specific to the left (L) side or right (R) side of the device.
GXB_CMUTX_[L,R][0:7]p, (Note 4) GXB_CMUTX_[L,R][0:7]n	Output	CMU transmitter channels, specific to the left (L) side or right (R) side of the device.
RREF_[L,R][0:1]	Input	Reference resistor for transceiver, specific to the left (L) side or right (R) side of the device.

Notes:

1. This pin definition is prepared based on the EP4S100G5.
2. Some of the pull-up /pull-down resisitors mentioned in the table above may not be required, depending on the exact device configuration scheme.
   The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.
   Refer to the Configuring Stratix IV GX Devices chapter in the Stratix IV GX Device Handbook for more information.
3. Transceiver signals GXB_RX[15..0] and GXB_TX[15..0] are device specific.
4. Dual purpose CMU Receiver channels. Can be used either as reference clock or CMU receiver channels in devices with 5th and 6th channels.
5. Refer to pin connections guidelines and data sheet for the recommended operating voltage.
6. Although some configuration pins may indicate that they serve as dual purpose (I/O and configuration) pins, this functionality is device dependent.
   Refer to the pin list to determine if the regular I/O function is available for the specific dual-purpose configuration pin.
7. The regular I/O function is not available for some of these reference pins. The availability of the regular I/O function on these reference pins is device dependent.
   Refer to the pin list to determine if the regular I/O function is available for the specific reference pin.



Note:

1. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	9/18/2009	Initial release.
1.1	12/3/2009	Added bank number for JTAG pins.
		Added Note (6) and Note (7) in Pin Definitions.
		Grouped nCSO, ASDO, and DCLK into dedicated configuration/JTAG pins in Pin Definitions.