Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF0B2	IO	DIFFIO_RX38p		C1	C1		F31			HIGH
B2	VREF0B2	IO	DIFFIO_RX38n		D2	D2		F32			HIGH
B2	VREF0B2	IO	DIFFIO_TX38p		E3	E3		G28			HIGH
B2	VREF0B2	IO	DIFFIO_TX38n		E4	E4		G27			HIGH
B2	VREF0B2	IO	DIFFIO_RX37p		E1	E1		G29			HIGH
B2	VREF0B2	IO	DIFFIO_RX37n		E2	E2		G30			HIGH
B2	VREF0B2	IO	DIFFIO_TX37p		F3	F3	F24	H28			HIGH
B2	VREF0B2	IO	DIFFIO_TX37n		F4	F4	F23	H27			HIGH
B2	VREF0B2	IO	DIFFIO_RX36p		F1	F1	C27	H30			HIGH
B2	VREF0B2	IO	DIFFIO_RX36n		F2	F2	C28	H29			HIGH
B2	VREF0B2	IO	DIFFIO_TX36p		G5	G5	G23	J27			HIGH
B2	VREF0B2	IO	DIFFIO_TX36n		G6	G6	G24	J28			HIGH
B2	VREF0B2	IO	DIFFIO_RX35p		G1	G1	D27	G31			HIGH
B2	VREF0B2	IO	DIFFIO_RX35n		G2	G2	D28	G32			HIGH
B2	VREF0B2	IO	DIFFIO_TX35p		G3	G3	H24	H25			HIGH
B2	VREF0B2	IO	DIFFIO_TX35n		G4	G4	H23	H26			HIGH
B2	VREF0B2	IO	DIFFIO_RX34p		H1	H1	E27	H31			HIGH
B2	VREF0B2	IO	DIFFIO_RX34n		H2	H2	E28	H32			HIGH
B2	VREF0B2	IO	DIFFIO_TX34p		H3	H3	H22	J25			HIGH
B2	VREF0B2	IO	DIFFIO_TX34n		H4	H4	H21	J26			HIGH
B2	VREF0B2	VREF0B2			H8	H8	E24	F27			
B2	VREF0B2	IO	DIFFIO_RX33p				F25	J29			HIGH
B2	VREF0B2	IO	DIFFIO_RX33n				F26	J30			HIGH
B2	VREF0B2	IO	DIFFIO_TX33p		H6	H6	J24	K28			HIGH
B2	VREF0B2	IO	DIFFIO_TX33n		H5	H5	J23	K27			HIGH
B2	VREF0B2	IO	DIFFIO_RX32p				F27	K30			HIGH
B2	VREF0B2	IO	DIFFIO_RX32n				F28	K29			HIGH
B2	VREF0B2	IO	DIFFIO_TX32p		J7	J7	K23	K26			HIGH
B2	VREF0B2	IO	DIFFIO_TX32n		H7	H7	K24	K25			HIGH
B2	VREF0B2	IO	DIFFIO_RX31p		J4	J4	G26	J32			HIGH
B2	VREF0B2	IO	DIFFIO_RX31n		J3	J3	G25	J31			HIGH
B2	VREF0B2	IO	DIFFIO_TX31p				J21	L27			HIGH
B2	VREF0B2	IO	DIFFIO_TX31n				J22	L26			HIGH
B2	VREF0B2	IO	DIFFIO_RX30p		J2	J2	G27	K31			HIGH
B2	VREF0B2	IO	DIFFIO_RX30n		J1	J1	G28	L32			HIGH
B2	VREF0B2	IO	DIFFIO_TX30p		J6	J6	K21	M26			HIGH
B2	VREF0B2	IO	DIFFIO_TX30n		J5	J5	K22	M27			HIGH
B2	VREF0B2	IO	DIFFIO_RX29p/RUP2		K4	K4	H26	M28			HIGH
B2	VREF0B2	IO	DIFFIO_RX29n/RDN2		K3	K3	H25	M29			HIGH
B2	VREF0B2	IO	DIFFIO_TX29p				L22	M24			HIGH
B2	VREF0B2	IO	DIFFIO_TX29n				L21	M25			HIGH
B2	VREF1B2	IO	DIFFIO_RX28p				H27	L30			HIGH
B2	VREF1B2	IO	DIFFIO_RX28n				H28	L31			HIGH
B2	VREF1B2	IO	DIFFIO_TX28p				L23	N24			HIGH
B2	VREF1B2	IO	DIFFIO_TX28n				L24	N23			HIGH
B2	VREF1B2	IO	DIFFIO_RX27p		K2	K2	J25	M31			HIGH
B2	VREF1B2	IO	DIFFIO_RX27n		K1	K1	J26	M30			HIGH
B2	VREF1B2	IO	DIFFIO_TX27p		K9	K9	L20	N27			HIGH
B2	VREF1B2	IO	DIFFIO_TX27n		J8	J8	L19	N28			HIGH
B2	VREF1B2	IO	DIFFIO_RX26p		K6	K6	J27	N29			HIGH
B2	VREF1B2	IO	DIFFIO_RX26n		K5	K5	J28	N30			HIGH
B2	VREF1B2	IO	DIFFIO_TX26p		K8	K8	M22	P23			HIGH
B2	VREF1B2	IO	DIFFIO_TX26n		K7	K7	M21	P24			HIGH
B2	VREF1B2	IO	DIFFIO_RX25p		L3	L3	K26	N31			HIGH
B2	VREF1B2	IO	DIFFIO_RX25n		L2	L2	K25	N32			HIGH
B2	VREF1B2	IO	DIFFIO_TX25p		L5	L5	M24	N25			HIGH
B2	VREF1B2	IO	DIFFIO_TX25n		L4	L4	M23	N26			HIGH
B2	VREF1B2	IO	DIFFIO_RX24p				K27	P29			HIGH
B2	VREF1B2	IO	DIFFIO_RX24n				K28	P30			HIGH
B2	VREF1B2	IO	DIFFIO_TX24p		L7	L7	M20	P28			HIGH
B2	VREF1B2	IO	DIFFIO_TX24n		L6	L6	M19	P27			HIGH
B2	VREF1B2	VREF1B2			L8	L8	K20	L25			
B2	VREF1B2	IO	DIFFIO_RX23p		M6	M6	L25	P31			HIGH
B2	VREF1B2	IO	DIFFIO_RX23n		M7	M7	L26	P32			HIGH
B2	VREF1B2	IO	DIFFIO_TX23p				N26	R28			HIGH
B2	VREF1B2	IO	DIFFIO_TX23n				N25	R27			HIGH
B2	VREF1B2	IO	DIFFIO_RX22p		M4	M4	L27	R32			HIGH
B2	VREF1B2	IO	DIFFIO_RX22n		M5	M5	L28	R31			HIGH
B2	VREF1B2	IO	DIFFIO_TX22p				N24	P25			HIGH
B2	VREF1B2	IO	DIFFIO_TX22n				N23	P26			HIGH
B2	VREF1B2	IO	DIFFIO_RX21p		N6	N6	M25	R30			HIGH
B2	VREF1B2	IO	DIFFIO_RX21n		N7	N7	M26	R29			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B2	VREF1B2	IO	DIFFIO_TX21p		M8	M8	N22	R23			HIGH
B2	VREF1B2	IO	DIFFIO_TX21n		M9	M9	N21	R24			HIGH
B2	VREF1B2	IO	DIFFIO_RX20p				M27	T32			HIGH
B2	VREF1B2	IO	DIFFIO_RX20n				N28	T31			HIGH
B2	VREF1B2	IO	DIFFIO_TX20p		P8	P8	N20	R25			HIGH
B2	VREF1B2	IO	DIFFIO_TX20n		N8	N8	N19	R26			HIGH
B2	VREF1B2	CLK0n			N2	N2	N27	T30			
B2	VREF1B2	CLK0p			N3	N3	P27	T29			
B2	VREF1B2	IO	CLK1n				P26	T28			
B2	VREF1B2	CLK1p			M1	M1	P25	T27			
		VCCA_PLL1			M3	M3	P23	T25			
		GND									
		GNDA_PLL1			N5	N5	P24	T26			
		VCCG_PLL1			M2	M2	P21	R22			
		GNDG_PLL1			N4	N4	P22	T22			
		VCCA_PLL2			P5	P5	R23	U25			
		GND									
		GNDA_PLL2			P3	P3	R24	U26			
		VCCG_PLL2			P4	P4	R21	U24			
		GNDG_PLL2			P2	P2	R22	T24			
B1	VREF0B1	CLK2p			R1	R1	R27	U31			
B1	VREF0B1	CLK2n			R2	R2	T27	U32			
B1	VREF0B1	CLK3p			R3	R3	R25	U29			
B1	VREF0B1	IO	CLK3n				R26	U30			
B1	VREF0B1	IO	DIFFIO_RX19p				T28	U28			HIGH
B1	VREF0B1	IO	DIFFIO_RX19n				U27	U27			HIGH
B1	VREF0B1	IO	DIFFIO_TX19p		P6	P6	T21	V26			HIGH
B1	VREF0B1	IO	DIFFIO_TX19n		P7	P7	T22	V25			HIGH
B1	VREF0B1	IO	DIFFIO_RX18p		R6	R6	U26	V32			HIGH
B1	VREF0B1	IO	DIFFIO_RX18n		R7	R7	U25	V31			HIGH
B1	VREF0B1	IO	DIFFIO_TX18p		R8	R8	T19	V28			HIGH
B1	VREF0B1	IO	DIFFIO_TX18n		R9	R9	T20	V27			HIGH
B1	VREF0B1	IO	DIFFIO_RX17p		R4	R4	V27	V30			HIGH
B1	VREF0B1	IO	DIFFIO_RX17n		R5	R5	V28	V29			HIGH
B1	VREF0B1	IO	DIFFIO_TX17p				T23	W25			HIGH
B1	VREF0B1	IO	DIFFIO_TX17n				T24	W26			HIGH
B1	VREF0B1	VREF0B1			T8	T8	R19	V21			
B1	VREF0B1	IO	DIFFIO_RX16p		T3	T3	V26	W32			HIGH
B1	VREF0B1	IO	DIFFIO_RX16n		T2	T2	V25	W31			HIGH
B1	VREF0B1	IO	DIFFIO_TX16p				T26	W27			HIGH
B1	VREF0B1	IO	DIFFIO_TX16n				T25	W28			HIGH
B1	VREF0B1	IO	DIFFIO_RX15p				W28	W30			HIGH
B1	VREF0B1	IO	DIFFIO_RX15n				W27	W29			HIGH
B1	VREF0B1	IO	DIFFIO_TX15p		T7	T7	U19	V24			HIGH
B1	VREF0B1	IO	DIFFIO_TX15n		T6	T6	U20	V23			HIGH
B1	VREF0B1	IO	DIFFIO_RX14p		T5	T5	W26	Y32			HIGH
B1	VREF0B1	IO	DIFFIO_RX14n		T4	T4	W25	Y31			HIGH
B1	VREF0B1	IO	DIFFIO_TX14p		U6	U6	U24	Y26			HIGH
B1	VREF0B1	IO	DIFFIO_TX14n		U5	U5	U23	Y25			HIGH
B1	VREF1B1	IO	DIFFIO_RX13p		U2	U2	Y28	Y30			HIGH
B1	VREF1B1	IO	DIFFIO_RX13n		U1	U1	Y27	Y29			HIGH
B1	VREF1B1	IO	DIFFIO_TX13p		U8	U8	U21	Y28			HIGH
B1	VREF1B1	IO	DIFFIO_TX13n		U7	U7	U22	Y27			HIGH
B1	VREF1B1	IO	DIFFIO_RX12p		U4	U4	Y26	AA31			HIGH
B1	VREF1B1	IO	DIFFIO_RX12n		U3	U3	Y25	AA30			HIGH
B1	VREF1B1	IO	DIFFIO_TX12p		U9	U9	V19	W23			HIGH
B1	VREF1B1	IO	DIFFIO_TX12n		V8	V8	V20	W24			HIGH
B1	VREF1B1	IO	DIFFIO_RX11p				AA28	AB31			HIGH
B1	VREF1B1	IO	DIFFIO_RX11n				AA27	AB30			HIGH
B1	VREF1B1	IO	DIFFIO_TX11p				V24	Y23			HIGH
B1	VREF1B1	IO	DIFFIO_TX11n				V23	Y24			HIGH
B1	VREF1B1	IO	DIFFIO_RX10p/RUP1		V6	V6	AA25	AA28			HIGH
B1	VREF1B1	IO	DIFFIO_RX10n/RDN1		V5	V5	AA26	AA29			HIGH
B1	VREF1B1	IO	DIFFIO_TX10p				V22	AA25			HIGH
B1	VREF1B1	IO	DIFFIO_TX10n				V21	AA24			HIGH
B1	VREF1B1	VREF1B1			V7	V7	W20	AA23			
B1	VREF1B1	IO	DIFFIO_RX9p				AB28	AB32			HIGH
B1	VREF1B1	IO	DIFFIO_RX9n				AB27	AC31			HIGH
B1	VREF1B1	IO	DIFFIO_TX9p				W23	AA27			HIGH
B1	VREF1B1	IO	DIFFIO_TX9n				W24	AA26			HIGH
B1	VREF1B1	IO	DIFFIO_RX8p		V1	V1	AB26	AD32			HIGH
B1	VREF1B1	IO	DIFFIO_RX8n		V2	V2	AB25	AD31			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B1	VREF1B1	IO	DIFFIO_TX8p		W5	W5	W21	AB27			HIGH
B1	VREF1B1	IO	DIFFIO_TX8n		W6	W6	W22	AB26			HIGH
B1	VREF1B1	IO	DIFFIO_RX7p		V3	V3	AC28	AC29			HIGH
B1	VREF1B1	IO	DIFFIO_RX7n		V4	V4	AC27	AC30			HIGH
B1	VREF1B1	IO	DIFFIO_TX7p		W7	W7	Y21	AC25			HIGH
B1	VREF1B1	IO	DIFFIO_TX7n		W8	W8	Y22	AC26			HIGH
B1	VREF2B1	IO	DIFFIO_RX6p		W1	W1	AD28	AD30			HIGH
B1	VREF2B1	IO	DIFFIO_RX6n		W2	W2	AD27	AD29			HIGH
B1	VREF2B1	IO	DIFFIO_TX6p				Y24	AC27			HIGH
B1	VREF2B1	IO	DIFFIO_TX6n				Y23	AC28			HIGH
B1	VREF2B1	IO	DIFFIO_RX5p				AE28	AE32			HIGH
B1	VREF2B1	IO	DIFFIO_RX5n				AE27	AE31			HIGH
B1	VREF2B1	IO	DIFFIO_TX5p		Y3	Y3	AA23	AD28			HIGH
B1	VREF2B1	IO	DIFFIO_TX5n		Y4	Y4	AA24	AD27			HIGH
B1	VREF2B1	IO	DIFFIO_RX4p		W3	W3	AF28	AE30			HIGH
B1	VREF2B1	IO	DIFFIO_RX4n		W4	W4	AF27	AE29			HIGH
B1	VREF2B1	IO	DIFFIO_TX4p		Y6	Y6	AA21	AD26			HIGH
B1	VREF2B1	IO	DIFFIO_TX4n		Y5	Y5	AA22	AD25			HIGH
B1	VREF2B1	IO	DIFFIO_RX3p		Y2	Y2		AF32			HIGH
B1	VREF2B1	IO	DIFFIO_RX3n		Y1	Y1		AF31			HIGH
B1	VREF2B1	IO	DIFFIO_TX3p		AA6	AA6	AB23	AE28			HIGH
B1	VREF2B1	IO	DIFFIO_TX3n		AA5	AA5	AB24	AE27			HIGH
B1	VREF2B1	VREF2B1			Y7	Y7	AE26	AB25			
B1	VREF2B1	IO	DIFFIO_RX2p		AA2	AA2		AF30			HIGH
B1	VREF2B1	IO	DIFFIO_RX2n		AA1	AA1		AF29			HIGH
B1	VREF2B1	IO	DIFFIO_TX2p		AA4	AA4		AE25			HIGH
B1	VREF2B1	IO	DIFFIO_TX2n		AA3	AA3		AE26			HIGH
B1	VREF2B1	IO	DIFFIO_RX1p		AB2	AB2		AG31			HIGH
B1	VREF2B1	IO	DIFFIO_RX1n		AB1	AB1		AG32			HIGH
B1	VREF2B1	IO	DIFFIO_TX1p		AB4	AB4		AF27			HIGH
B1	VREF2B1	IO	DIFFIO_TX1n		AB3	AB3		AF28			HIGH
B1	VREF2B1	IO	DIFFIO_RX0p		AC2	AC2		AG30			HIGH
B1	VREF2B1	IO	DIFFIO_RX0n		AD1	AD1		AG29			HIGH
B1	VREF2B1	IO	DIFFIO_TX0p		AC4	AC4		AF26			HIGH
B1	VREF2B1	IO	DIFFIO_TX0n		AC3	AC3		AF25			HIGH
B8	VREF0B8	IO					AC24	AB24			
B8	VREF0B8	IO	DQ9B7		AD5	AD5	AG26	AH28	DQ3B15	DQ1B31	
B8	VREF0B8	IO			AC5	AC5	AC23	AC24			
B8	VREF0B8	IO	DQ9B6		AD2	AD2	AH26	AK30	DQ3B14	DQ1B30	
B8	VREF0B8	IO	DQ9B5		AE2	AE2	AG25	AJ28	DQ3B13	DQ1B29	
B8	VREF0B8	IO	DQ9B4		AD3	AD3	AH25	AJ29	DQ3B12	DQ1B28	
B8	VREF0B8	IO					AB22	AC23			
B8	VREF0B8	IO	DQ9B3		AE4	AE4	AF25	AK29	DQ3B11	DQ1B27	
B8	VREF0B8	IO						AD24			
B8	VREF0B8	IO	DQS9B		AD4	AD4	AF24	AK28			
B8	VREF0B8	IO	DQ9B2		AE3	AE3	AG24	AL30	DQ3B10	DQ1B26	
B8	VREF0B8	IO					AE25	AD23			
B8	VREF0B8	IO	DQ9B1		AB5	AB5	AE24	AL29	DQ3B9	DQ1B25	
B8	VREF0B8	IO						AE24			
B8	VREF0B8	IO	DQ9B0		AF3	AF3	AH24	AM29	DQ3B8	DQ1B24	
B8	VREF0B8	IO			AB6	AB6	AD24	AE23			
B8	VREF0B8	IO			AC6	AC6		AF24			
B8	VREF0B8	IO	DQ8B7		AC7	AC7	AG23	AH26	DQ3B7	DQ1B23	
B8	VREF0B8	VREF0B8			AE5	AE5	AD22	AH27			
B8	VREF0B8	IO	DQ8B6		AD6	AD6	AD23	AJ27	DQ3B6	DQ1B22	
B8	VREF0B8	IO	DQ8B5		AE7	AE7	AF23	AL28	DQ3B5	DQ1B21	
B8	VREF0B8	IO			AF5	AF5	AB21	AC22			
B8	VREF0B8	IO	DQ8B4		AB7	AB7	AH23	AK27	DQ3B4	DQ1B20	
B8	VREF0B8	IO	DQ8B3		AD7	AD7	AE22	AJ26	DQ3B3	DQ1B19	
B8	VREF0B8	IO						AG24			
B8	VREF0B8	IO	DQS8B		AE6	AE6	AE23	AL27	DQS3B		
B8	VREF0B8	IO	DQ8B2		AA7	AA7	AF22	AM27	DQ3B2	DQ1B18	
B8	VREF0B8	IO					AB20	AB22			
B8	VREF0B8	IO	DQ8B1		AF7	AF7	AH22	AM28	DQ3B1	DQ1B17	
B8	VREF0B8	IO	DQ8B0		AF6	AF6	AG22	AK26	DQ3B0	DQ1B16	
B8	VREF0B8	IO						AF23			
B8	VREF1B8	IO					Y20	AA21			
B8	VREF1B8	IO	DQ7B7		AC8	AC8	AD21	AH24	DQ2B15	DQ1B15	
B8	VREF1B8	IO						AB21			
B8	VREF1B8	IO	DQ7B6		AB8	AB8	AE21	AJ24	DQ2B14	DQ1B14	
B8	VREF1B8	IO	DQ7B5		AD8	AD8	AG21	AJ25	DQ2B13	DQ1B13	
B8	VREF1B8	IO					AC22	AD22			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B8	VREF1B8	IO	DQ7B4		AE8	AE8	AF21	AK25	DQ2B12	DQ1B12	
B8	VREF1B8	IO	DQ7B3		AF8	AF8	AE20	AL25	DQ2B11	DQ1B11	
B8	VREF1B8	IO						AC21			
B8	VREF1B8	IO	DQS7B		Y9	Y9	AG20	AL26		DQS1B	
B8	VREF1B8	IO	DQ7B2		Y8	Y8	AF20	AK24	DQ2B10	DQ1B10	
B8	VREF1B8	IO					AC20	AG23			
B8	VREF1B8	IO	DQ7B1		W9	W9	AH21	AM25	DQ2B9	DQ1B9	
B8	VREF1B8	IO						AD21			
B8	VREF1B8	IO	DQ7B0		AA8	AA8	AH20	AM26	DQ2B8	DQ1B8	
B8	VREF1B8	IO	DQ6B7		AC9	AC9	AE19	AJ23	DQ2B7	DQ1B7	
B8	VREF1B8	IO	FCLK3		AD9	AD9	AC21	AE21			
B8	VREF1B8	IO	FCLK2		AB9	AB9	AC19	AF21			
B8	VREF1B8	VREF1B8			AE9	AE9	AD20	AH25			
B8	VREF1B8	IO	DQ6B6		AF9	AF9	AD19	AL24	DQ2B6	DQ1B6	
B8	VREF1B8	IO	DQ6B5		AD10	AD10	AF19	AH22	DQ2B5	DQ1B5	
B8	VREF1B8	IO						AF22			
B8	VREF1B8	IO	DQ6B4		AE10	AE10	AG19	AM24	DQ2B4	DQ1B4	
B8	VREF1B8	IO		PGM2	AA9	AA9	AB19	AA20			
B8	VREF1B8	IO	DQ6B3		AC10	AC10	AH19	AK23	DQ2B3	DQ1B3	
B8	VREF1B8	IO						AB20			
B8	VREF1B8	IO	DQS6B		Y10	Y10	AF18	AJ22	DQS2B		
B8	VREF1B8	IO	DQ6B2		AA10	AA10	AD18	AL23	DQ2B2	DQ1B2	
B8	VREF1B8	IO		CRC_ERROR	W10	W10	AA20	AF20			
B8	VREF1B8	IO	DQ6B1		AB10	AB10	AE18	AK22	DQ2B1	DQ1B1	
B8	VREF1B8	IO	DQ6B0		AF10	AF10	AG18	AL22	DQ2B0	DQ1B0	
B8	VREF1B8	IO	RDN8		AB11	AB11	Y19	AC20			
B8	VREF1B8	IO	RUP8		AE11	AE11	W19	AH19			
B8	VREF1B8	IO	DQ5B7				AF17	AM22			
B8	VREF1B8	IO						AG22			
B8	VREF1B8	IO	DQ5B6				AG17	AJ21			
B8	VREF1B8	IO	DQ5B5				AE17	AK21			
B8	VREF2B8	IO						AB19			
B8	VREF2B8	IO	DQ5B4				AD17	AL21			
B8	VREF2B8	IO		RDYnBSY	AC11	AC11	AA19	AA19			
B8	VREF2B8	IO	DQ5B3				AG16	AH20			
B8	VREF2B8	IO					AB18	AD20			
B8	VREF2B8	IO	DQS5B				AH16	AJ20			
B8	VREF2B8	IO	DQ5B2				AD16	AK20			
B8	VREF2B8	IO		nCS	Y11	Y11	Y18	AC19			
B8	VREF2B8	IO	DQ5B1				AF16	AL20			
B8	VREF2B8	IO	DQ5B0				AE16	AM20			
B8	VREF2B8	IO			AD11	AD11		AG21			
B8	VREF2B8	IO						AG20			
B8	VREF2B8	IO					V18	AE20			
B8	VREF2B8	IO					W18	AD19			
B8	VREF2B8	IO		CS	AA11	AA11	AA18	AG19			
B8	VREF2B8	IO						AJ18			
B8	VREF2B8	IO						AH18			
B8	VREF2B8	IO						AK18			
B8	VREF2B8	VREF2B8			W11	W11	AH18	AH23			
B8	VREF2B8	IO	CLK5n		AD12	AD12	Y17	AJ19			
B8	VREF2B8	CLK5p			AC12	AC12	AA17	AK19			
B8	VREF2B8	IO	CLK4n		AF12	AF12	AB17	AL19			
B8	VREF2B8	CLK4p			AE12	AE12	AC17	AM19			
B8	VREF2B8	PLL_ENA		PLL_ENA	W12	W12	AC18	AF19			
B8	VREF2B8	MSEL0		MSEL0	Y12	Y12	AC16	AG18			
B8	VREF2B8	MSEL1		MSEL1	Y13	Y13	W17	AE18			
B8	VREF2B8	MSEL2		MSEL2	W13	W13	AB15	AE19			
B12	VREF2B8	IO	PLL6_OUT3n				Y16	AM18			
B12	VREF2B8	IO	PLL6_OUT3p				W16	AL18			
B12	VREF2B8	IO	PLL6_OUT2n				AG15	AK17			
B12	VREF2B8	IO	PLL6_OUT2p				AF15	AJ17			
B11	VREF2B8	IO	PLL6_FBn		AB12	AB12	AA15	AM17			
B11	VREF2B8	IO	PLL6_FBp		AA12	AA12	AA14	AL17			
B11	VREF2B8	IO	PLL6_OUT1n		AB14	AB14	W15	AK16			
B11	VREF2B8	IO	PLL6_OUT1p		AA14	AA14	W14	AJ16			
B11	VREF2B8	IO	PLL6_OUT0n		AB13	AB13	AE15	AM16			
B11	VREF2B8	IO	PLL6_OUT0p		AA13	AA13	AD15	AL16			
B12		VCC_PLL6_OUTB					AB16	AB17			
B11		VCC_PLL6_OUTA					AC14	AE17			
B11		VCC_PLL6_OUTA			AE13	AE13					
		VCCA_PLL6			AD14	AD14	AG14	AG17			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND									
		GNDA_PLL6			AC14	AC14	AF14	AH17			
		VCCG_PLL6			AD13	AD13	AA13	AD16			
		GNDG_PLL6			AE14	AE14	AB14	AB16			
B7	VREF0B7	CLK7p			AE15	AE15	W13	AM15			
B7	VREF0B7	IO	CLK7n				Y13	AL15			
B7	VREF0B7	CLK6p			AF15	AF15	AD14	AK15			
B7	VREF0B7	IO	CLK6n				AE14	AJ15			
B7	VREF0B7	nCE		nCE	Y14	Y14	AB13	AF18			
B7	VREF0B7	nCEO		nCEO	W14	W14	AC13	AH15			
B7	VREF0B7	IO						AA18			
B7	VREF0B7	IO						AB15			
B7	VREF0B7	IO		PGM0	W15	W15	W12	AD18			
B7	VREF0B7	nIO_PULLUP		nIO_PULLUP	AA15	AA15	Y12	AF15			
B7	VREF0B7	VCCSEL		VCCSEL	Y15	Y15	AA12	AJ14			
B7	VREF0B7	PORSEL		PORSEL	W16	W16	AC12	AG15			
B7	VREF0B7	IO						AA15			
B7	VREF0B7	IO						AD15			
B7	VREF0B7	IO						AC15			
B7	VREF0B7	IO						AK14			
B7	VREF0B7	IO						AC18			
B7	VREF0B7	IO						AL14			
B7	VREF0B7	VREF0B7			AB15	AB15	AD11	AH12			
B7	VREF0B7	IO		INIT_DONE	AC15	AC15	W11	AE15			
B7	VREF0B7	IO					V11	AB14			
B7	VREF0B7	IO	DQ4B7				AD13	AL13			
B7	VREF0B7	IO	DQ4B6				AE13	AM13			
B7	VREF0B7	IO		nRS	Y16	Y16	AC11	AB18			
B7	VREF0B7	IO	DQ4B5				AF13	AH13			
B7	VREF0B7	IO					Y11	AA14			
B7	VREF0B7	IO	DQ4B4				AD12	AJ13			
B7	VREF0B7	IO	DQ4B3				AG13	AK13			
B7	VREF0B7	IO		RUnLU	AD15	AD15	W10	AF14			
B7	VREF0B7	IO	DQS4B				AH13	AJ12			
B7	VREF0B7	IO			AA16	AA16	AB12	AE14			
B7	VREF1B7	IO	DQ4B2				AE12	AK12			
B7	VREF1B7	IO	DQ4B1				AF12	AL12			
B7	VREF1B7	IO		PGM1	AC16	AC16	AA11	AG14			
B7	VREF1B7	IO	DQ4B0				AG12	AM11			
B7	VREF1B7	IO	RDN7		AB16	AB16	AC10	AC14			
B7	VREF1B7	IO	RUP7		AD16	AD16	AB11	AF13			
B7	VREF1B7	IO	DQ3B7		W17	W17	AG11	AL10	DQ1B15	DQ0B31	
B7	VREF1B7	IO						AD14			
B7	VREF1B7	IO	DQ3B6		AE16	AE16	AH11	AK11	DQ1B14	DQ0B30	
B7	VREF1B7	IO	DQ3B5		Y17	Y17	AE11	AL11	DQ1B13	DQ0B29	
B7	VREF1B7	IO	DEV_CLRn		AF17	AF17	AC9	AH14			
B7	VREF1B7	IO	DQ3B4		AA17	AA17	AF11	AK10	DQ1B12	DQ0B28	
B7	VREF1B7	IO	DQ3B3		Y18	Y18	AE10	AM9	DQ1B11	DQ0B27	
B7	VREF1B7	IO						AB13			
B7	VREF1B7	IO	DQS3B		AE17	AE17	AG10	AJ11	DQS1B		
B7	VREF1B7	IO					Y10	AG13			
B7	VREF1B7	IO	DQ3B2		W18	W18	AH10	AL9	DQ1B10	DQ0B26	
B7	VREF1B7	IO	DQ3B1		AB17	AB17	AF10	AJ10	DQ1B9	DQ0B25	
B7	VREF1B7	VREF1B7			AB18	AB18	AD9	AH10			
B7	VREF1B7	IO	DQ3B0		AA18	AA18	AD10	AH11	DQ1B8	DQ0B24	
B7	VREF1B7	IO			Y19	Y19		AC13			
B7	VREF1B7	IO					AA10	AE13			
B7	VREF1B7	IO	DQ2B7		AF18	AF18	AG9	AL8	DQ1B7	DQ0B23	
B7	VREF1B7	IO	FCLK5		AC17	AC17	AC8	AM14			
B7	VREF1B7	IO	FCLK4		AD17	AD17	AB10	AF12			
B7	VREF1B7	IO	DQ2B6		AE18	AE18	AF9	AJ9	DQ1B6	DQ0B22	
B7	VREF1B7	IO	DQ2B5		AF19	AF19	AE9	AK9	DQ1B5	DQ0B21	
B7	VREF1B7	IO					AB9	AD13			
B7	VREF1B7	IO	DQ2B4		Y20	Y20	AH8	AM8	DQ1B4	DQ0B20	
B7	VREF1B7	IO	DQ2B3		AA19	AA19	AH9	AH9	DQ1B3	DQ0B19	
B7	VREF1B7	IO			AD18	AD18		AG12			
B7	VREF2B7	IO	DQS2B		AB19	AB19	AE8	AK8		DQS0B	
B7	VREF2B7	IO	DQ2B2		AD19	AD19	AD8	AM7	DQ1B2	DQ0B18	
B7	VREF2B7	IO			AC18	AC18	AA9	AE12			
B7	VREF2B7	IO	DQ2B1		AC19	AC19	AF8	AJ8	DQ1B1	DQ0B17	
B7	VREF2B7	IO	DQ2B0		AE19	AE19	AG8	AL7	DQ1B0	DQ0B16	
B7	VREF2B7	IO						AC12			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B7	VREF2B7	IO			AF20	AF20	AB8	AA12			
B7	VREF2B7	IO	DQ1B7		AE20	AE20	AF6	AL6	DQ0B15	DQ0B15	
B7	VREF2B7	IO	DQ1B6		AA20	AA20	AG7	AM6	DQ0B14	DQ0B14	
B7	VREF2B7	IO					AC7	AD12			
B7	VREF2B7	IO	DQ1B5		AB20	AB20	AH7	AJ7	DQ0B13	DQ0B13	
B7	VREF2B7	IO	DQ1B4		AF21	AF21	AF7	AM5	DQ0B12	DQ0B12	
B7	VREF2B7	IO						AB11			
B7	VREF2B7	IO	DQ1B3		AC20	AC20	AD6	AK7	DQ0B11	DQ0B11	
B7	VREF2B7	IO	DQS1B		AA21	AA21	AE7	AH7	DQS0B		
B7	VREF2B7	IO			AB21	AB21	AD5	AE11			
B7	VREF2B7	IO	DQ1B2		AE21	AE21	AH6	AL5	DQ0B10	DQ0B10	
B7	VREF2B7	IO	DQ1B1		AD20	AD20	AG6	AK6	DQ0B9	DQ0B9	
B7	VREF2B7	VREF2B7			AD21	AD21	AD7	AH8			
B7	VREF2B7	IO	DQ1B0		AC21	AC21	AE6	AJ6	DQ0B8	DQ0B8	
B7	VREF2B7	IO					Y9	AF10			
B7	VREF2B7	IO						AG10			
B7	VREF2B7	IO	DQ0B7		AE25	AE25	AF5	AL3	DQ0B7	DQ0B7	
B7	VREF2B7	IO					AE4	AG11			
B7	VREF2B7	IO	DQ0B6		AF22	AF22	AH5	AL4	DQ0B6	DQ0B6	
B7	VREF2B7	IO					AC6	AD9			
B7	VREF2B7	IO	DQ0B5		AF24	AF24	AF4	AM4	DQ0B5	DQ0B5	
B7	VREF2B7	IO	DQ0B4		AE22	AE22	AG4	AJ4	DQ0B4	DQ0B4	
B7	VREF2B7	IO			AD23	AD23		AG9			
B7	VREF2B7	IO	DQ0B3		AB22	AB22	AG5	AJ5	DQ0B3	DQ0B3	
B7	VREF2B7	IO	DQS0B		AE23	AE23	AH3	AK5			
B7	VREF2B7	IO			AD24	AD24	AC5	AC9			
B7	VREF2B7	IO	DQ0B2		AC23	AC23	AG3	AH5	DQ0B2	DQ0B2	
B7	VREF2B7	IO	DQ0B1		AC22	AC22	AE5	AK3	DQ0B1	DQ0B1	
B7	VREF2B7	IO			AD22	AD22	AB7	AE9			
B7	VREF2B7	IO	DQ0B0		AE24	AE24	AH4	AK4	DQ0B0	DQ0B0	
B7	VREF2B7	IO						AF9			
B6	VREF0B6	IO	DIFFIO_TX77n		AD25	AD25		AF8			HIGH
B6	VREF0B6	IO	DIFFIO_TX77p		AC24	AC24		AF7			HIGH
B6	VREF0B6	IO	DIFFIO_RX77n		AD26	AD26		AG4			HIGH
B6	VREF0B6	IO	DIFFIO_RX77p		AC25	AC25		AG3			HIGH
B6	VREF0B6	IO	DIFFIO_TX76n		AB24	AB24		AF5			HIGH
B6	VREF0B6	IO	DIFFIO_TX76p		AB23	AB23		AF6			HIGH
B6	VREF0B6	IO	DIFFIO_RX76n		AB26	AB26		AG1			HIGH
B6	VREF0B6	IO	DIFFIO_RX76p		AB25	AB25		AG2			HIGH
B6	VREF0B6	IO	DIFFIO_TX75n		AA24	AA24		AE7			HIGH
B6	VREF0B6	IO	DIFFIO_TX75p		AA23	AA23		AE8			HIGH
B6	VREF0B6	IO	DIFFIO_RX75n		AA26	AA26		AF4			HIGH
B6	VREF0B6	IO	DIFFIO_RX75p		AA25	AA25		AF3			HIGH
B6	VREF0B6	VREF0B6			Y21	Y21	AE3	AG6			
B6	VREF0B6	IO	DIFFIO_TX74n		AA22	AA22	AB5	AD6			HIGH
B6	VREF0B6	IO	DIFFIO_TX74p		Y22	Y22	AB6	AD5			HIGH
B6	VREF0B6	IO	DIFFIO_RX74n		Y26	Y26		AF2			HIGH
B6	VREF0B6	IO	DIFFIO_RX74p		Y25	Y25		AF1			HIGH
B6	VREF0B6	IO	DIFFIO_TX73n		Y24	Y24	AA7	AE6			HIGH
B6	VREF0B6	IO	DIFFIO_TX73p		Y23	Y23	AA8	AE5			HIGH
B6	VREF0B6	IO	DIFFIO_RX73n		W23	W23	AF2	AE4			HIGH
B6	VREF0B6	IO	DIFFIO_RX73p		W24	W24	AF1	AE3			HIGH
B6	VREF0B6	IO	DIFFIO_TX72n		W21	W21	AA5	AD8			HIGH
B6	VREF0B6	IO	DIFFIO_TX72p		W22	W22	AA6	AD7			HIGH
B6	VREF0B6	IO	DIFFIO_RX72n				AE2	AE2			HIGH
B6	VREF0B6	IO	DIFFIO_RX72p				AE1	AE1			HIGH
B6	VREF0B6	IO	DIFFIO_TX71n				Y6	AC5			HIGH
B6	VREF0B6	IO	DIFFIO_TX71p				Y5	AC6			HIGH
B6	VREF0B6	IO	DIFFIO_RX71n		W25	W25	AD2	AC3			HIGH
B6	VREF0B6	IO	DIFFIO_RX71p		W26	W26	AD1	AC4			HIGH
B6	VREF1B6	IO	DIFFIO_TX70n		W19	W19	Y7	AC7			HIGH
B6	VREF1B6	IO	DIFFIO_TX70p		W20	W20	Y8	AC8			HIGH
B6	VREF1B6	IO	DIFFIO_RX70n		V23	V23	AC2	AD3			HIGH
B6	VREF1B6	IO	DIFFIO_RX70p		V24	V24	AC1	AD4			HIGH
B6	VREF1B6	IO	DIFFIO_TX69n		V21	V21	W7	AB7			HIGH
B6	VREF1B6	IO	DIFFIO_TX69p		V22	V22	W8	AB6			HIGH
B6	VREF1B6	IO	DIFFIO_RX69n		V25	V25	AB4	AD2			HIGH
B6	VREF1B6	IO	DIFFIO_RX69p		V26	V26	AB3	AD1			HIGH
B6	VREF1B6	IO	DIFFIO_TX68n				W5	AA6			HIGH
B6	VREF1B6	IO	DIFFIO_TX68p				W6	AA7			HIGH
B6	VREF1B6	IO	DIFFIO_RX68n				AB2	AC2			HIGH
B6	VREF1B6	IO	DIFFIO_RX68p				AB1	AB1			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B6	VREF1B6	VREF1B6			V20	V20	W9	AB8			
B6	VREF1B6	IO	DIFFIO_TX67n				V8	AA9			HIGH
B6	VREF1B6	IO	DIFFIO_TX67p				V7	AA8			HIGH
B6	VREF1B6	IO	DIFFIO_RX67n/RDN6		U24	U24	AA3	AA4			HIGH
B6	VREF1B6	IO	DIFFIO_RX67p/RUP6		U23	U23	AA4	AA5			HIGH
B6	VREF1B6	IO	DIFFIO_TX66n				V6	Y5			HIGH
B6	VREF1B6	IO	DIFFIO_TX66p				V5	Y6			HIGH
B6	VREF1B6	IO	DIFFIO_RX66n				AA2	AB3			HIGH
B6	VREF1B6	IO	DIFFIO_RX66p				AA1	AB2			HIGH
B6	VREF1B6	IO	DIFFIO_TX65n		V19	V19	V9	Y7			HIGH
B6	VREF1B6	IO	DIFFIO_TX65p		U20	U20	V10	Y8			HIGH
B6	VREF1B6	IO	DIFFIO_RX65n		U26	U26	Y4	AA3			HIGH
B6	VREF1B6	IO	DIFFIO_RX65p		U25	U25	Y3	AA2			HIGH
B6	VREF1B6	IO	DIFFIO_TX64n		U19	U19	U7	W5			HIGH
B6	VREF1B6	IO	DIFFIO_TX64p		U18	U18	U8	W6			HIGH
B6	VREF1B6	IO	DIFFIO_RX64n		U22	U22	Y2	Y4			HIGH
B6	VREF1B6	IO	DIFFIO_RX64p		U21	U21	Y1	Y3			HIGH
B6	VREF2B6	IO	DIFFIO_TX63n		T21	T21	U6	Y10			HIGH
B6	VREF2B6	IO	DIFFIO_TX63p		T20	T20	U5	Y9			HIGH
B6	VREF2B6	IO	DIFFIO_RX63n		T25	T25	W4	Y2			HIGH
B6	VREF2B6	IO	DIFFIO_RX63p		T24	T24	W3	Y1			HIGH
B6	VREF2B6	IO	DIFFIO_TX62n		T19	T19	U9	W10			HIGH
B6	VREF2B6	IO	DIFFIO_TX62p		R19	R19	U10	W9			HIGH
B6	VREF2B6	IO	DIFFIO_RX62n				W2	W4			HIGH
B6	VREF2B6	IO	DIFFIO_RX62p				W1	W3			HIGH
B6	VREF2B6	IO	DIFFIO_TX61n				T6	V9			HIGH
B6	VREF2B6	IO	DIFFIO_TX61p				T5	V10			HIGH
B6	VREF2B6	IO	DIFFIO_RX61n		T23	T23	V4	W2			HIGH
B6	VREF2B6	IO	DIFFIO_RX61p		T22	T22	V3	W1			HIGH
B6	VREF2B6	VREF2B6			R18	R18	R10	AA10			
B6	VREF2B6	IO	DIFFIO_TX60n				T10	V5			HIGH
B6	VREF2B6	IO	DIFFIO_TX60p				T9	V6			HIGH
B6	VREF2B6	IO	DIFFIO_RX60n		R22	R22	V1	V4			HIGH
B6	VREF2B6	IO	DIFFIO_RX60p		R23	R23	V2	V3			HIGH
B6	VREF2B6	IO	DIFFIO_TX59n		P20	P20	T7	V8			HIGH
B6	VREF2B6	IO	DIFFIO_TX59p		P21	P21	T8	V7			HIGH
B6	VREF2B6	IO	DIFFIO_RX59n		R20	R20	U4	V2			HIGH
B6	VREF2B6	IO	DIFFIO_RX59p		R21	R21	U3	V1			HIGH
B6	VREF2B6	IO	DIFFIO_TX58n		P19	P19	T4	W8			HIGH
B6	VREF2B6	IO	DIFFIO_TX58p		N19	N19	T3	W7			HIGH
B6	VREF2B6	IO	DIFFIO_RX58n				U2	U5			HIGH
B6	VREF2B6	IO	DIFFIO_RX58p				T1	U6			HIGH
B6	VREF2B6	IO	CLK8n				R3	U3			
B6	VREF2B6	CLK8p			P24	P24	R4	U4			
B6	VREF2B6	CLK9n			P25	P25	T2	U1			
B6	VREF2B6	CLK9p			R26	R26	R2	U2			
		GNDG_PLL3			R25	R25	R7	U11			
		VCCG_PLL3			P23	P23	R8	V11			
		GNDA_PLL3			R24	R24	R5	U7			
		GND									
		VCCA_PLL3			P22	P22	R6	U8			
		GNDG_PLL4			N22	N22	P7	U9			
		VCCG_PLL4			N24	N24	P8	T9			
		GNDA_PLL4			N23	N23	P5	T7			
		GND									
		VCCA_PLL4			N25	N25	P6	T8			
B5	VREF0B5	CLK10p			M26	M26	P4	T6			
B5	VREF0B5	IO	CLK10n				P3	T5			
B5	VREF0B5	CLK11p			M24	M24	P2	T4			
B5	VREF0B5	CLK11n			M25	M25	N2	T3			
B5	VREF0B5	IO	DIFFIO_TX57n		N20	N20	N10	R7			HIGH
B5	VREF0B5	IO	DIFFIO_TX57p		N21	N21	N9	R8			HIGH
B5	VREF0B5	IO	DIFFIO_RX57n				M2	T2			HIGH
B5	VREF0B5	IO	DIFFIO_RX57p				N1	T1			HIGH
B5	VREF0B5	IO	DIFFIO_TX56n		M18	M18	N5	P7			HIGH
B5	VREF0B5	IO	DIFFIO_TX56p		M19	M19	N6	P8			HIGH
B5	VREF0B5	IO	DIFFIO_RX56n		M20	M20	M3	R1			HIGH
B5	VREF0B5	IO	DIFFIO_RX56p		M21	M21	M4	R2			HIGH
B5	VREF0B5	IO	DIFFIO_TX55n				N7	R5			HIGH
B5	VREF0B5	IO	DIFFIO_TX55p				N8	R6			HIGH
B5	VREF0B5	IO	DIFFIO_RX55n		M22	M22	L1	R3			HIGH
B5	VREF0B5	IO	DIFFIO_RX55p		M23	M23	L2	R4			HIGH

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B5	VREF0B5	IO	DIFFIO_TX54n				N4	R10			HIGH
B5	VREF0B5	IO	DIFFIO_TX54p				N3	R9			HIGH
B5	VREF0B5	IO	DIFFIO_RX54n		L22	L22	L3	P1			HIGH
B5	VREF0B5	IO	DIFFIO_RX54p		L23	L23	L4	P2			HIGH
B5	VREF0B5	VREF0B5			L19	L19	P10	R12			
B5	VREF0B5	IO	DIFFIO_TX53n		L21	L21	M10	P6			HIGH
B5	VREF0B5	IO	DIFFIO_TX53p		L20	L20	M9	P5			HIGH
B5	VREF0B5	IO	DIFFIO_RX53n				K1	P3			HIGH
B5	VREF0B5	IO	DIFFIO_RX53p				K2	P4			HIGH
B5	VREF0B5	IO	DIFFIO_TX52n		K20	K20	M6	N7			HIGH
B5	VREF0B5	IO	DIFFIO_TX52p		K19	K19	M5	N8			HIGH
B5	VREF0B5	IO	DIFFIO_RX52n		L25	L25	K4	N1			HIGH
B5	VREF0B5	IO	DIFFIO_RX52p		L24	L24	K3	N2			HIGH
B5	VREF0B5	IO	DIFFIO_TX51n		K22	K22	M8	P9			HIGH
B5	VREF0B5	IO	DIFFIO_TX51p		K21	K21	M7	P10			HIGH
B5	VREF0B5	IO	DIFFIO_RX51n		K24	K24	J1	N3			HIGH
B5	VREF0B5	IO	DIFFIO_RX51p		K23	K23	J2	N4			HIGH
B5	VREF0B5	IO	DIFFIO_TX50n		J20	J20	L10	N5			HIGH
B5	VREF0B5	IO	DIFFIO_TX50p		J19	J19	L9	N6			HIGH
B5	VREF0B5	IO	DIFFIO_RX50n		K26	K26	J3	M2			HIGH
B5	VREF0B5	IO	DIFFIO_RX50p		K25	K25	J4	M3			HIGH
B5	VREF0B5	IO	DIFFIO_TX49n				L5	N10			HIGH
B5	VREF0B5	IO	DIFFIO_TX49p				L6	N9			HIGH
B5	VREF0B5	IO	DIFFIO_RX49n				H1	L2			HIGH
B5	VREF0B5	IO	DIFFIO_RX49p				H2	L3			HIGH
B5	VREF1B5	IO	DIFFIO_TX48n				L8	M8			HIGH
B5	VREF1B5	IO	DIFFIO_TX48p				L7	M9			HIGH
B5	VREF1B5	IO	DIFFIO_RX48n/RDN5		J22	J22	H3	M4			HIGH
B5	VREF1B5	IO	DIFFIO_RX48p/RUP5		J21	J21	H4	M5			HIGH
B5	VREF1B5	IO	DIFFIO_TX47n		H20	H20	K7	M6			HIGH
B5	VREF1B5	IO	DIFFIO_TX47p		H19	H19	K8	M7			HIGH
B5	VREF1B5	IO	DIFFIO_RX47n		J26	J26	G1	L1			HIGH
B5	VREF1B5	IO	DIFFIO_RX47p		J25	J25	G2	K2			HIGH
B5	VREF1B5	IO	DIFFIO_TX46n				J7	L6			HIGH
B5	VREF1B5	IO	DIFFIO_TX46p				J8	L7			HIGH
B5	VREF1B5	IO	DIFFIO_RX46n		J24	J24	G4	J2			HIGH
B5	VREF1B5	IO	DIFFIO_RX46p		J23	J23	G3	J1			HIGH
B5	VREF1B5	IO	DIFFIO_TX45n		H22	H22	K5	K5			HIGH
B5	VREF1B5	IO	DIFFIO_TX45p		H21	H21	K6	K6			HIGH
B5	VREF1B5	IO	DIFFIO_RX45n				F1	K4			HIGH
B5	VREF1B5	IO	DIFFIO_RX45p				F2	K3			HIGH
B5	VREF1B5	IO	DIFFIO_TX44n		H24	H24	J6	K8			HIGH
B5	VREF1B5	IO	DIFFIO_TX44p		H23	H23	J5	K7			HIGH
B5	VREF1B5	IO	DIFFIO_RX44n				F3	J3			HIGH
B5	VREF1B5	IO	DIFFIO_RX44p				F4	J4			HIGH
B5	VREF1B5	VREF1B5			J18	J18	K9	L8			
B5	VREF1B5	IO	DIFFIO_TX43n		G21	G21	H8	J5			HIGH
B5	VREF1B5	IO	DIFFIO_TX43p		G22	G22	H7	J6			HIGH
B5	VREF1B5	IO	DIFFIO_RX43n		H25	H25	E1	H1			HIGH
B5	VREF1B5	IO	DIFFIO_RX43p		H26	H26	E2	H2			HIGH
B5	VREF1B5	IO	DIFFIO_TX42n		G23	G23	H6	J7			HIGH
B5	VREF1B5	IO	DIFFIO_TX42p		G24	G24	H5	J8			HIGH
B5	VREF1B5	IO	DIFFIO_RX42n		G25	G25	D1	G1			HIGH
B5	VREF1B5	IO	DIFFIO_RX42p		G26	G26	D2	G2			HIGH
B5	VREF1B5	IO	DIFFIO_TX41n		F23	F23	G5	H5			HIGH
B5	VREF1B5	IO	DIFFIO_TX41p		F24	F24	G6	H6			HIGH
B5	VREF1B5	IO	DIFFIO_RX41n		F25	F25	C1	H3			HIGH
B5	VREF1B5	IO	DIFFIO_RX41p		F26	F26	C2	H4			HIGH
B5	VREF1B5	IO	DIFFIO_TX40n		E23	E23	F6	H8			HIGH
B5	VREF1B5	IO	DIFFIO_TX40p		E24	E24	F5	H7			HIGH
B5	VREF1B5	IO	DIFFIO_RX40n		E25	E25		F1			HIGH
B5	VREF1B5	IO	DIFFIO_RX40p		E26	E26		F2			HIGH
B5	VREF1B5	IO	DIFFIO_TX39n		D24	D24		G6			HIGH
B5	VREF1B5	IO	DIFFIO_TX39p		C25	C25		G5			HIGH
B5	VREF1B5	IO	DIFFIO_RX39n		D25	D25		G3			HIGH
B5	VREF1B5	IO	DIFFIO_RX39p		C26	C26		G4			HIGH
B4	VREF0B4	IO						F7			
B4	VREF0B4	IO	DQ0T0		B24	B24	A4	D5	DQ0T0	DQ0T0	
B4	VREF0B4	IO			B25	B25	G7	K9			
B4	VREF0B4	IO	DQ0T1		D23	D23	A3	C3	DQ0T1	DQ0T1	
B4	VREF0B4	IO	DQ0T2		D22	D22	B3	E5	DQ0T2	DQ0T2	
B4	VREF0B4	IO	DQS0T		C24	C24	D5	C5			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF0B4	IO			B23	B23	F7	F8			
B4	VREF0B4	IO	DQ0T3		E22	E22	B5	C4	DQ0T3	DQ0T3	
B4	VREF0B4	IO			C23	C23		J9			
B4	VREF0B4	IO	DQ0T4		B22	B22	B4	D4	DQ0T4	DQ0T4	
B4	VREF0B4	IO	DQ0T5		A24	A24	C4	A4	DQ0T5	DQ0T5	
B4	VREF0B4	IO					G8	M10			
B4	VREF0B4	IO	DQ0T6		A22	A22	A5	B4	DQ0T6	DQ0T6	
B4	VREF0B4	IO					F8	G9			
B4	VREF0B4	IO	DQ0T7		C22	C22	C5	B3	DQ0T7	DQ0T7	
B4	VREF0B4	IO						H9			
B4	VREF0B4	IO					J9	L9			
B4	VREF0B4	IO	DQ1T0		C20	C20	E6	D6	DQ0T8	DQ0T8	
B4	VREF0B4	VREF0B4			F22	F22	E7	E6			
B4	VREF0B4	IO	DQ1T1		D21	D21	A6	C6	DQ0T9	DQ0T9	
B4	VREF0B4	IO	DQ1T2		D20	D20	B7	B5	DQ0T10	DQ0T10	
B4	VREF0B4	IO			B21	B21		K11			
B4	VREF0B4	IO	DQS1T		A21	A21	B6	E7	DQS0T		
B4	VREF0B4	IO					H9	L11			
B4	VREF0B4	IO	DQ1T3		C21	C21	D6	C7	DQ0T11	DQ0T11	
B4	VREF0B4	IO	DQ1T4		B20	B20	A7	A5	DQ0T12	DQ0T12	
B4	VREF0B4	IO						J11			
B4	VREF0B4	IO	DQ1T5		E21	E21	D7	D7	DQ0T13	DQ0T13	
B4	VREF0B4	IO					G9	F9			
B4	VREF0B4	IO	DQ1T6		A20	A20	C6	A6	DQ0T14	DQ0T14	
B4	VREF0B4	IO	DQ1T7		F21	F21	C7	B6	DQ0T15	DQ0T15	
B4	VREF0B4	IO			C19	C19	F9	G10			
B4	VREF0B4	IO						F10			
B4	VREF0B4	IO	DQ2T0		D19	D19	D8	B7	DQ1T0	DQ0T16	
B4	VREF0B4	IO	DQ2T1		E20	E20	C8	D8	DQ1T1	DQ0T17	
B4	VREF0B4	IO			B19	B19	H10	L12			
B4	VREF0B4	IO	DQ2T2		E19	E19	E8	B8	DQ1T2	DQ0T18	
B4	VREF1B4	IO	DQS2T		A19	A19	C9	A7		DQS0T	
B4	VREF1B4	IO						H11			
B4	VREF1B4	IO	DQ2T3		C18	C18	D9	E9	DQ1T3	DQ0T19	
B4	VREF1B4	IO	DQ2T4		B18	B18	B9	A8	DQ1T4	DQ0T20	
B4	VREF1B4	IO	DQ2T5		D18	D18	B8	C9	DQ1T5	DQ0T21	
B4	VREF1B4	IO	DQ2T6		F20	F20	A8	C8	DQ1T6	DQ0T22	
B4	VREF1B4	IO	FCLK6		G19	G19	G10	G12			
B4	VREF1B4	IO	FCLK7		E18	E18	F10	A14			
B4	VREF1B4	IO	DQ2T7		G20	G20	A9	D9	DQ1T7	DQ0T23	
B4	VREF1B4	IO						J12			
B4	VREF1B4	IO			A18	A18	J10	K12			
B4	VREF1B4	IO	DQ3T0		F19	F19	E10	E11	DQ1T8	DQ0T24	
B4	VREF1B4	VREF1B4			F18	F18	E9	E8			
B4	VREF1B4	IO	DQ3T1		C17	C17	A10	B9	DQ1T9	DQ0T25	
B4	VREF1B4	IO					F11	H12			
B4	VREF1B4	IO	DQ3T2		G18	G18	C10	D10	DQ1T10	DQ0T26	
B4	VREF1B4	IO					K10	K13			
B4	VREF1B4	IO	DQS3T		B17	B17	D10	D11	DQS1T		
B4	VREF1B4	IO	DQ3T3		E17	E17	B10	C10	DQ1T11	DQ0T27	
B4	VREF1B4	IO						F12			
B4	VREF1B4	IO	DQ3T4		F17	F17	A11	A9	DQ1T12	DQ0T28	
B4	VREF1B4	IO	DQ3T5		D17	D17	C11	B11	DQ1T13	DQ0T29	
B4	VREF1B4	IO	DEV_OE		G17	G17	J11	L13			
B4	VREF1B4	IO	DQ3T6		A17	A17	D11	C11	DQ1T14	DQ0T30	
B4	VREF1B4	IO	DQ3T7		H18	H18	B11	B10	DQ1T15	DQ0T31	
B4	VREF1B4	IO	RUP4		D16	D16	H11	G13			
B4	VREF1B4	IO	RDN4		C16	C16	G11	J13			
B4	VREF1B4	IO	DQ4T0				B12	A11			
B4	VREF1B4	IO		nWS	E16	E16	K11	D14			
B4	VREF1B4	IO	DQ4T1				C12	B12			
B4	VREF1B4	IO	DQ4T2				D12	C12			
B4	VREF2B4	IO			B16	B16	G12	F13			
B4	VREF2B4	IO	DQS4T				A13	D12			
B4	VREF2B4	IO		DATA0	F16	F16	H12	E14			
B4	VREF2B4	IO	DQ4T3				B13	C13			
B4	VREF2B4	IO	DQ4T4				E12	D13			
B4	VREF2B4	IO					L11	L14			
B4	VREF2B4	IO	DQ4T5				C13	E13			
B4	VREF2B4	IO		DATA1	C15	C15	F12	F14			
B4	VREF2B4	IO	DQ4T6				D13	A13			
B4	VREF2B4	IO	DQ4T7				E13	B13			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B4	VREF2B4	IO					M11	H13			
B4	VREF2B4	IO		DATA2	H16	H16	J12	F15			
B4	VREF2B4	VREF2B4			G16	G16	E11	E10			
B4	VREF2B4	IO						C14			
B4	VREF2B4	IO						B14			
B4	VREF2B4	IO						H14			
B4	VREF2B4	IO						J15			
B4	VREF2B4	IO						J14			
B4	VREF2B4	IO						K14			
B4	VREF2B4	TMS		TMS	E15	E15	F13	E15			
B4	VREF2B4	TRST		TRST	D15	D15	L12	G15			
B4	VREF2B4	TCK		TCK	G15	G15	K12	G14			
B4	VREF2B4	IO		DATA3	F15	F15	M12	C16			
B4	VREF2B4	IO						K15			
B4	VREF2B4	IO						L15			
B4	VREF2B4	TDI		TDI	H15	H15	G13	D16			
B4	VREF2B4	TDO		TDO	G14	G14	H13	F16			
B4	VREF2B4	IO	CLK12n				J13	A15			
B4	VREF2B4	CLK12p			B15	B15	K13	B15			
B4	VREF2B4	IO	CLK13n				L13	C15			
B4	VREF2B4	CLK13p			A15	A15	M13	D15			
		TEMPDIODEp			H14	H14	B14	E18			
		TEMPDIODEn			G13	G13	C14	F18			
		VCCA_PLL5			D14	D14	F14	G17			
		GND									
		GNDA_PLL5			B14	B14	G14	F17			
		VCCG_PLL5			C14	C14	D14	J16			
		GNDG_PLL5			B13	B13	E14	L16			
B9		VCC_PLL5_OUTA			D13	D13	F15	H17			
B10		VCC_PLL5_OUTB					G16	L17			
B9	VREF0B3	IO	PLL5_OUT0p		F13	F13	E15	B16			
B9	VREF0B3	IO	PLL5_OUT0n		E13	E13	D15	A16			
B9	VREF0B3	IO	PLL5_OUT1p		F14	F14	K14	B17			
B9	VREF0B3	IO	PLL5_OUT1n		E14	E14	K15	A17			
B9	VREF0B3	IO	PLL5_FBp		F12	F12	H14	D17			
B9	VREF0B3	IO	PLL5_FBn		E12	E12	H15	C17			
B10	VREF0B3	IO	PLL5_OUT2p				C15	B18			
B10	VREF0B3	IO	PLL5_OUT2n				B15	A18			
B10	VREF0B3	IO	PLL5_OUT3p				K16	D18			
B10	VREF0B3	IO	PLL5_OUT3n				J16	C18			
B3	VREF0B3	nSTATUS		nSTATUS	H13	H13	M16	G16			
B3	VREF0B3	nCONFIG		nCONFIG	H12	H12	L16	J18			
B3	VREF0B3	DCLK		DCLK	G12	G12	F16	E19			
B3	VREF0B3	CONF_DONE		CONF_DONE	H11	H11	G17	G18			
B3	VREF0B3	CLK14p			B12	B12	K17	A19			
B3	VREF0B3	IO	CLK14n		A12	A12	J17	B19			
B3	VREF0B3	CLK15p			D12	D12	M17	C19			
B3	VREF0B3	IO	CLK15n		C12	C12	L17	D19			
B3	VREF0B3	VREF0B3			F11	F11	E18	E21			
B3	VREF0B3	IO						K18			
B3	VREF0B3	IO						F19			
B3	VREF0B3	IO		DATA4	E11	E11	H17	G19			
B3	VREF0B3	IO					L18	F20			
B3	VREF0B3	IO					M18	L18			
B3	VREF0B3	IO						K20			
B3	VREF0B3	IO						H19			
B3	VREF0B3	IO			B11	B11	F17	G20			
B3	VREF0B3	IO	DQ5T0				D16	A20			
B3	VREF0B3	IO	DQ5T1				C16	B20			
B3	VREF0B3	IO		DATA5	G11	G11	K18	J19			
B3	VREF0B3	IO	DQ5T2				E16	C20			
B3	VREF0B3	IO	DQS5T				A16	D20			
B3	VREF0B3	IO						H20			
B3	VREF0B3	IO	DQ5T3				B16	E20			
B3	VREF0B3	IO		DATA6	H10	H10	H18	K19			
B3	VREF0B3	IO	DQ5T4				E17	B21			
B3	VREF0B3	IO	DQ5T5				D17	C21			
B3	VREF1B3	IO					F18	G21			
B3	VREF1B3	IO	DQ5T6				B17	D21			
B3	VREF1B3	IO						F23			
B3	VREF1B3	IO	DQ5T7				C17	A22			
B3	VREF1B3	IO	RUP3		C11	C11	J18	F21			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
B3	VREF1B3	IO	RDN3		D11	D11	K19	L19			
B3	VREF1B3	IO	DQ6T0		A10	A10	A18	B22	DQ2T0	DQ1T0	
B3	VREF1B3	IO	DQ6T1		E10	E10	C18	C22	DQ2T1	DQ1T1	
B3	VREF1B3	IO		DATA7	G10	G10	G18	J20			
B3	VREF1B3	IO	DQ6T2		F10	F10	D18	B23	DQ2T2	DQ1T2	
B3	VREF1B3	IO	DQS6T		G9	G9	B18	D22	DQS2T		
B3	VREF1B3	IO						L20			
B3	VREF1B3	IO	DQ6T3		F9	F9	A19	C23	DQ2T3	DQ1T3	
B3	VREF1B3	IO		CLKUSR	D10	D10	J19	H21			
B3	VREF1B3	IO	DQ6T4		C10	C10	B19	A24	DQ2T4	DQ1T4	
B3	VREF1B3	IO						J21			
B3	VREF1B3	IO	DQ6T5		B10	B10	C19	E22	DQ2T5	DQ1T5	
B3	VREF1B3	IO	DQ6T6		A9	A9	E19	B24	DQ2T6	DQ1T6	
B3	VREF1B3	VREF1B3			D9	D9	E20	E23			
B3	VREF1B3	IO	FCLK0		E9	E9	F19	F22			
B3	VREF1B3	IO	FCLK1		B9	B9	G19	G22			
B3	VREF1B3	IO	DQ6T7		C9	C9	D19	D23	DQ2T7	DQ1T7	
B3	VREF1B3	IO			G7	G7	H19	K21			
B3	VREF1B3	IO						L21			
B3	VREF1B3	IO	DQ7T0		A8	A8	B20	D24	DQ2T8	DQ1T8	
		GND			F8	F8	G20	H24			
B3	VREF1B3	IO	DQ7T1		A7	A7	A20	A25	DQ2T9	DQ1T9	
B3	VREF1B3	IO	DQ7T2		B8	B8	C20	C24	DQ2T10	DQ1T10	
B3	VREF1B3	IO						H22			
B3	VREF1B3	IO	DQS7T		E8	E8	D20	B26		DQS1T	
B3	VREF1B3	IO	DQ7T3		F7	F7	A21	B25	DQ2T11	DQ1T11	
B3	VREF1B3	IO					J20	K22			
B3	VREF1B3	IO	DQ7T4		B7	B7	B21	C25	DQ2T12	DQ1T12	
B3	VREF1B3	IO	DQ7T5		C8	C8	C21	D25	DQ2T13	DQ1T13	
B3	VREF1B3	IO						J22			
B3	VREF1B3	IO	DQ7T6		D8	D8	D21	A26	DQ2T14	DQ1T14	
B3	VREF1B3	IO	DQ7T7		E7	E7	E21	E24	DQ2T15	DQ1T15	
B3	VREF1B3	IO					H20	L22			
B3	VREF2B3	IO						G23			
B3	VREF2B3	IO	DQ8T0		B6	B6	B22	C26	DQ3T0	DQ1T16	
B3	VREF2B3	IO	DQ8T1		A6	A6	A22	A28	DQ3T1	DQ1T17	
B3	VREF2B3	IO						H23			
B3	VREF2B3	IO	DQ8T2		F6	F6	C22	A27	DQ3T2	DQ1T18	
B3	VREF2B3	IO	DQS8T		F5	F5	D23	B27	DQS3T		
B3	VREF2B3	IO						F24			
B3	VREF2B3	IO	DQ8T3		D6	D6	D22	D26	DQ3T3	DQ1T19	
B3	VREF2B3	IO	DQ8T4		E6	E6	A23	C27	DQ3T4	DQ1T20	
B3	VREF2B3	IO						J24			
B3	VREF2B3	IO	DQ8T5		A5	A5	C23	B28	DQ3T5	DQ1T21	
B3	VREF2B3	IO	DQ8T6		E5	E5	E23	D27	DQ3T6	DQ1T22	
B3	VREF2B3	VREF2B3			D7	D7	E22	E25			
B3	VREF2B3	IO	DQ8T7		C7	C7	B23	E26	DQ3T7	DQ1T23	
B3	VREF2B3	IO			C6	C6	F20	G24			
B3	VREF2B3	IO			B5	B5		J23			
B3	VREF2B3	IO	DQ9T0		C3	C3	A24	A29	DQ3T8	DQ1T24	
B3	VREF2B3	IO						K23			
B3	VREF2B3	IO	DQ9T1		A3	A3	C25	B29	DQ3T9	DQ1T25	
B3	VREF2B3	IO					F21	F25			
B3	VREF2B3	IO	DQ9T2		D5	D5	A25	B30	DQ3T10	DQ1T26	
B3	VREF2B3	IO	DQS9T		B4	B4	C24	C28			
B3	VREF2B3	IO					G21	F26			
B3	VREF2B3	IO	DQ9T3		C2	C2	D24	C29	DQ3T11	DQ1T27	
B3	VREF2B3	IO					G22	L23			
B3	VREF2B3	IO	DQ9T4		B3	B3	B24	D29	DQ3T12	DQ1T28	
B3	VREF2B3	IO	DQ9T5		D4	D4	B25	D28	DQ3T13	DQ1T29	
B3	VREF2B3	IO	DQ9T6		C4	C4	A26	C30	DQ3T14	DQ1T30	
B3	VREF2B3	IO			C5	C5	F22	K24			
B3	VREF2B3	IO	DQ9T7		D3	D3	B26	E28	DQ3T15	DQ1T31	
B3	VREF2B3	IO						L24			
		VCCIO2			D1	D1	B28	C31			
		VCCIO2			L1	L1	M28	C32			
		VCCIO2			L9	L9	P20	M32			
		VCCIO2						T23			
		VCCIO1			T1	T1	R20	AA32			
		VCCIO1			AC1	AC1	U28	AK31			
		VCCIO1			T9	T9	AG28	AK32			
		VCCIO1						U23			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		VCCIO8			AF4	AF4	Y15	AC17			
		VCCIO8			AF11	AF11	AH17	AM21			
		VCCIO8			V11	V11	AH27	AM30			
		VCCIO8			V12	V12					
		VCCIO7			V15	V15	Y14	AC16			
		VCCIO7			V16	V16	AH2	AM12			
		VCCIO7			AF16	AF16	AH12	AM3			
		VCCIO7			AF23	AF23					
		VCCIO6			T18	T18	R9	AA1			
		VCCIO6			AC26	AC26	U1	AK1			
		VCCIO6			T26	T26	AG1	AK2			
		VCCIO6						U10			
		VCCIO5			L26	L26	B1	C1			
		VCCIO5			L18	L18	M1	C2			
		VCCIO5			D26	D26	P9	M1			
		VCCIO5						T10			
		VCCIO4			A23	A23	A2	A12			
		VCCIO4			A16	A16	A12	A3			
		VCCIO4			J15	J15	J14	K16			
		VCCIO4			J16	J16					
		VCCIO3			A4	A4	A17	A21			
		VCCIO3			A11	A11	A27	A30			
		VCCIO3			J11	J11	J15	K17			
		VCCIO3			J12	J12					
		VCCINT			K11	K11	M14	M12			
		VCCINT			M15	M15	N11	M14			
		VCCINT			P17	P17	N13	M19			
		VCCINT			U10	U10	N15	M21			
		VCCINT			K13	K13	N17	N13			
		VCCINT			M17	M17	P12	N15			
		VCCINT			R10	R10	P14	N18			
		VCCINT			U12	U12	P16	N20			
		VCCINT			K15	K15	R13	P12			
		VCCINT			N10	N10	R15	P14			
		VCCINT			R12	R12	R17	P16			
		VCCINT			U14	U14	T12	P17			
		VCCINT			K17	K17	T14	P19			
		VCCINT			N12	N12	T16	P21			
		VCCINT			R14	R14	T18	R13			
		VCCINT			U16	U16	U11	R15			
		VCCINT			L10	L10	U13	R18			
		VCCINT			N14	N14	U15	R20			
		VCCINT			R16	R16	U17	T14			
		VCCINT			L12	L12	V12	T16			
		VCCINT			N16	N16	V16	T17			
		VCCINT			T11	T11		T19			
		VCCINT			L14	L14		U14			
		VCCINT			P11	P11		U16			
		VCCINT			T13	T13		U17			
		VCCINT			L16	L16		U19			
		VCCINT			P13	P13		V13			
		VCCINT			T15	T15		V15			
		VCCINT			M11	M11		V18			
		VCCINT			P15	P15		V20			
		VCCINT			T17	T17		W14			
		VCCINT			M13	M13		W16			
		VCCINT						W17			
		VCCINT						W19			
		VCCINT						Y13			
		VCCINT						Y15			
		VCCINT						Y18			
		VCCINT						Y20			
		GND			A13	A13	C3	AA16			
		GND			B1	B1	C26	AA17			
		GND			J17	J17	L14	AC1			
		GND			L17	L17	L15	AC32			
		GND			N17	N17	M15	AL1			
		GND			P26	P26	N12	AL2			
		GND			U11	U11	N14	AL31			
		GND			V18	V18	N16	AL32			
		GND			A14	A14	N18	AM10			
		GND			B2	B2	P1	AM2			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		GND			K10	K10	P11	AM23			
		GND			M10	M10	P13	AM31			
		GND			N18	N18	P15	B1			
		GND			R11	R11	P17	B2			
		GND			U13	U13	P18	B31			
		GND			A2	A2	P28	B32			
		GND			AF25	AF25	R1	K1			
		GND			J14	J14	R11	K32			
		GND			L15	L15	R12	M13			
		GND			N15	N15	R14	M15			
		GND			P18	P18	R16	M16			
		GND			T16	T16	R18	M17			
		GND			V17	V17	AA16	AD17			
		GND			A25	A25	AC15	AF17			
		GND			B26	B26	G15	J17			
		GND			K12	K12	H16	H18			
		GND			M12	M12	R28	M18			
		GND			N26	N26	T11	M20			
		GND			R13	R13	T13	N12			
		GND			U15	U15	T15	N14			
		GND			AE1	AE1	T17	N16			
		GND			G8	G8	U12	N17			
		GND			K14	K14	U14	N19			
		GND			M14	M14	U16	N21			
		GND			P1	P1	U18	P13			
		GND			R15	R15	V13	P15			
		GND			U17	U17	V14	P18			
		GND			AE26	AE26	V15	P20			
		GND			H9	H9	V17	R14			
		GND			K16	K16	AF3	R16			
		GND			M16	M16	AF26	R17			
		GND			P9	P9	AG2	R19			
		GND			R17	R17	AG27	T12			
		GND			V9	V9	AH14	T13			
		GND			AF2	AF2	AH15	T15			
		GND			H17	H17		T18			
		GND			K18	K18		T20			
		GND			N1	N1		T21			
		GND			P10	P10		U12			
		GND			T10	T10		U13			
		GND			V10	V10		U15			
		GND			AF13	AF13		U18			
		GND			J9	J9		U20			
		GND			L11	L11		U21			
		GND			N9	N9		V14			
		GND			P12	P12		V16			
		GND			T12	T12		V17			
		GND			V13	V13		V19			
		GND			AF14	AF14		W13			
		GND			J10	J10		W15			
		GND			L13	L13		W18			
		GND			N11	N11		W20			
		GND			P14	P14		Y14			
		GND			T14	T14		Y16			
		GND			V14	V14		Y17			
		GND			J13	J13		Y19			
		GND			N13	N13					
		GND			P16	P16					
		GND			C13	C13					
		GND			AC13	AC13					
		GND					A14	A10			
		GND					A15	A2			
		GND					B2	A23			
		GND					B27	A31			
		NC					P19	AA11			
		NC					E5	AB23			
		NC					E26	AE16			
		NC					E25	AG25			
		NC					D26	AH16			
		NC					D25	AJ3			
		NC					AC26	D32			
		NC					AC25	E30			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC					AD26	F30			
		NC					AD25	K10			
		NC					AC3	N22			
		NC					AD3	W11			
		NC					AC4	AB5			
		NC					AD4	AC11			
		NC					E3	AG5			
		NC					E4	AH1			
		NC					D3	AH31			
		NC					D4	D1			
		NC						E4			
		NC						F4			
		NC						G25			
		NC						L28			
		NC						R21			
		NC						Y11			
		NC						AA22			
		NC						AB29			
		NC						AF11			
		NC						AG27			
		NC						AH29			
		NC						AJ31			
		NC						E2			
		NC						E32			
		NC						G8			
		NC						L5			
		NC						P22			
		NC						W21			
		NC						AB10			
		NC						AD11			
		NC						AG8			
		NC						AH3			
		NC						AJ1			
		NC						D3			
		NC						E16			
		NC						F6			
		NC						H10			
		NC						M11			
		NC						U22			
		NC						Y21			
		NC						AA13			
		NC						AB28			
		NC						AE22			
		NC						AG26			
		NC						AH21			
		NC						AJ30			
		NC						E1			
		NC						E31			
		NC						G7			
		NC						L4			
		NC						P11			
		NC						W12			
		NC						AB9			
		NC						AD10			
		NC						AG7			
		NC						AH2			
		NC						AH32			
		NC						D2			
		NC						E12			
		NC						F5			
		NC						G26			
		NC						L29			
		NC						T11			
		NC						Y12			
		NC						AB4			
		NC						AC10			
		NC						AF16			
		NC						AG28			
		NC						AH30			
		NC						AJ32			
		NC						E3			
		NC						F3			

Bank Number	VREF Bank	Pin Name/Function	Optional Function(s)	Configuration Function	B672	F672	F780	F1020	DQS for x16	DQS for x32	DIFFIO Speed (1)
		NC						G11			
		NC						L10			
		NC						R11			
		NC						W22			
		NC						AB12			
		NC						AE10			
		NC						AG16			
		NC						AH4			
		NC						AJ2			
		NC						D30			
		NC						E17			
		NC						F11			
		NC						H15			
		NC						M22			
		NC						V12			
		NC						Y22			
		NC						AH6			
		NC						D31			
		NC						E27			
		NC						F28			
		NC						H16			
		NC						M23			
		NC						V22			
		NC						E29			
		NC						F29			
		NC						J10			
		NC						N11			

Note to Pin-List:

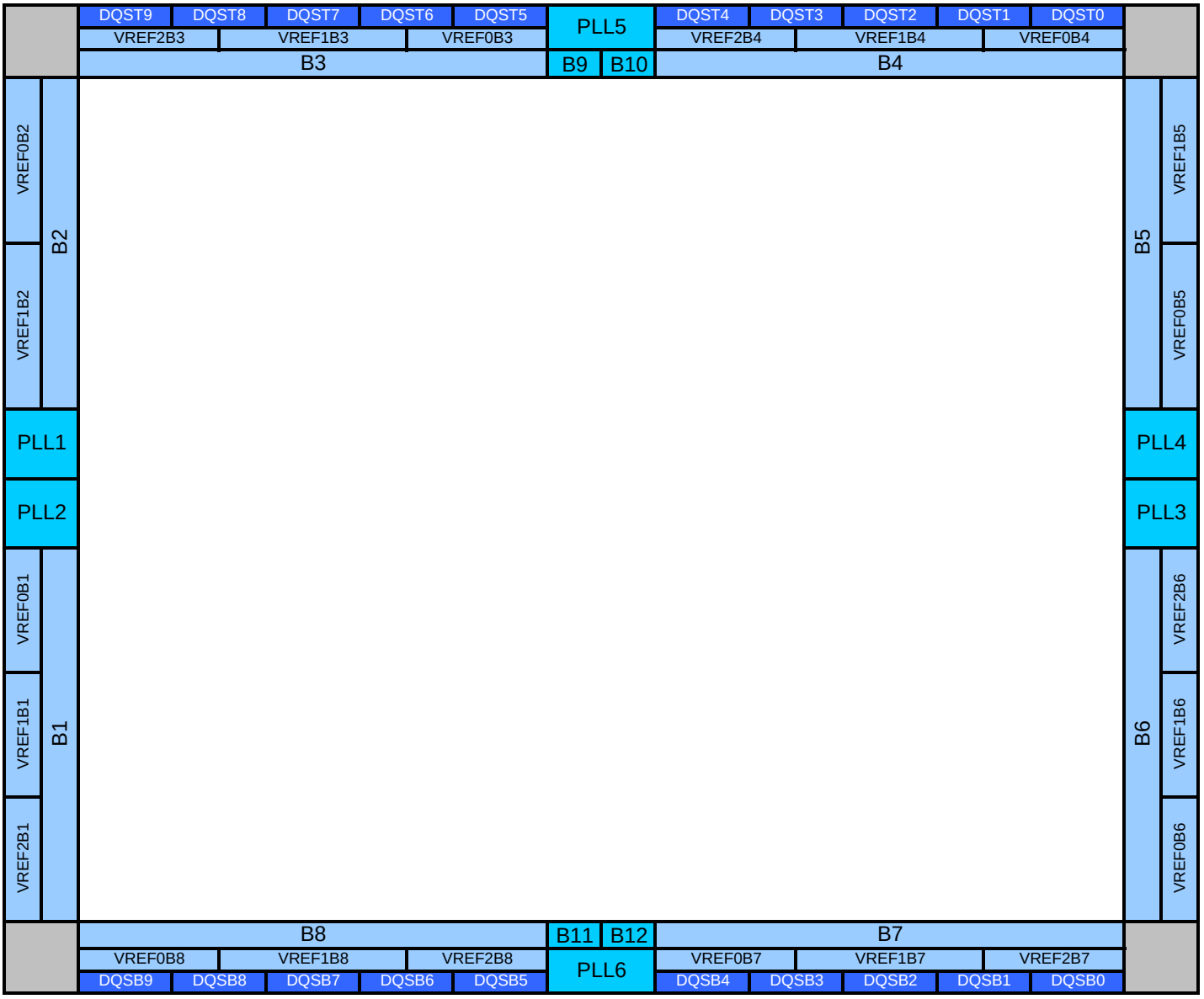
1) The wire bond and flip-chip packages will have different data rates for the high speed differential I/O channels. The following table shows the data rates as supported for each package.

Package	Package Type	High Speed Differential I/O Channel		Units
		High	Low	
B672	wire bond	462	N/A	Mbps
F672	wire bond	462	N/A	Mbps
F780	flip chip	840	N/A	Mbps
F1020	flip chip	840	N/A	Mbps

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
		Supply and Reference Pins
VREF[1..4]B[1..8]	Input	Input reference voltage for bank 1. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If VREF pins are not used, designers should connect them to either VCC or Gnd.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5-V, 1.8-V, 2.5-V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, 3.3-V PCML, HyperTransport™ technology, differential HSTL, GTL, GTL+, HSTL, SSTL, CTT, and 3.3-V AGP I/O standards.
VCC_PLL5_OUTA	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 9.
VCC_PLL5_OUTB	Power	External clock output buffer power for PLL5 clock outputs PLL5_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 10.
VCC_PLL6_OUTA	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[1..0]. The designer must connect this pin to the VCCIO of bank 11.
VCC_PLL6_OUTB	Power	External clock output buffer power for PLL6 clock outputs PLL6_OUT[3..2]. The designer must connect this pin to the VCCIO of bank 12.
VCCA_PLL[1..12]	Power	Analog power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDA_PLL[1..12]	Ground	Analog ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
VCCG_PLL[1..12]	Power	Guard ring power for PLLs[1..12]. The designer must connect this pin to 1.5 V, even if the PLL is not used.
GNDG_PLL[1..12]	Ground	Guard ring ground for PLLs[1..12]. The designer can connect this pin to the GND plane on the board.
NC	No Connect	Do not drive signals into these pins.
		Dedicated & Configuration/JTAG Pins
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin; it is not available as a user I/O pin.
nCONFIG	Input	Dedicated configuration control input. A low transition resets the target device; a low-to-high transition begins configuration. All I/O pins tri-state when nCONFIG is driven low.
DCLK	Input	Clock input used to clock configuration data from an external source into the Stratix device. This is a dedicated pin used for configuration.
nIO_PULLUP	Input	IF nIO_PULLUP is driven high during configuration, the weak pull-ups on all user I/O pins are disabled. If driven low, the weak pull-ups are enabled during configuration. nIO_PULLUP can be pulled up to either 1.5, 1.8, 2.5, or 3.3 V.
PORSEL	Input	Dedicated input pin used to select POR delay times of 2 ms or 100 ms during powerup. When PORSEL is connected to ground, the POR time is 100 ms. When PORSEL is connected to 3.3 V, the POR time is 2 ms.
VCCSEL	Input	VCCSEL is used to select which input buffer is used on all configuration pins. VCCSEL will control whether the 3.3-/2.5-V input buffer or the 1.8-/1.5-V input buffer is used. A "0" means 3.3/2.5 V and a "1" means 1.8-/1.5 V. At powerup, VCCSEL accepts 3.3V and 2.5V TTL Levels. VCCSEL affects the following pins: TDI, TMS, TCK, TRST, MSEL0, MSEL1, MSEL2, nCONFIG, nCE, DCLK, CONF_DONE, nSTATUS, and PLL_ENA.
nCE	Input	Active-low chip enables. Dedicated chip enable input used to detect which device is active in a chain of devices. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin.
TMS	Input	This is a dedicated JTAG input pin.
TDI	Input	This is a dedicated JTAG input pin.
TCK	Input	This is a dedicated JTAG input pin.
TDO	Output	This is a dedicated JTAG input pin.
TRST	Input	This is a dedicated JTAG input pin. Active low input, used to asynchronously reset the JTAG boundary scan circuit.
MSEL[2..0]	Input	Dedicated mode select control pins that set the configuration mode for the device.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix device. If the temperature sensing diode is not used then connect this pin to GND.

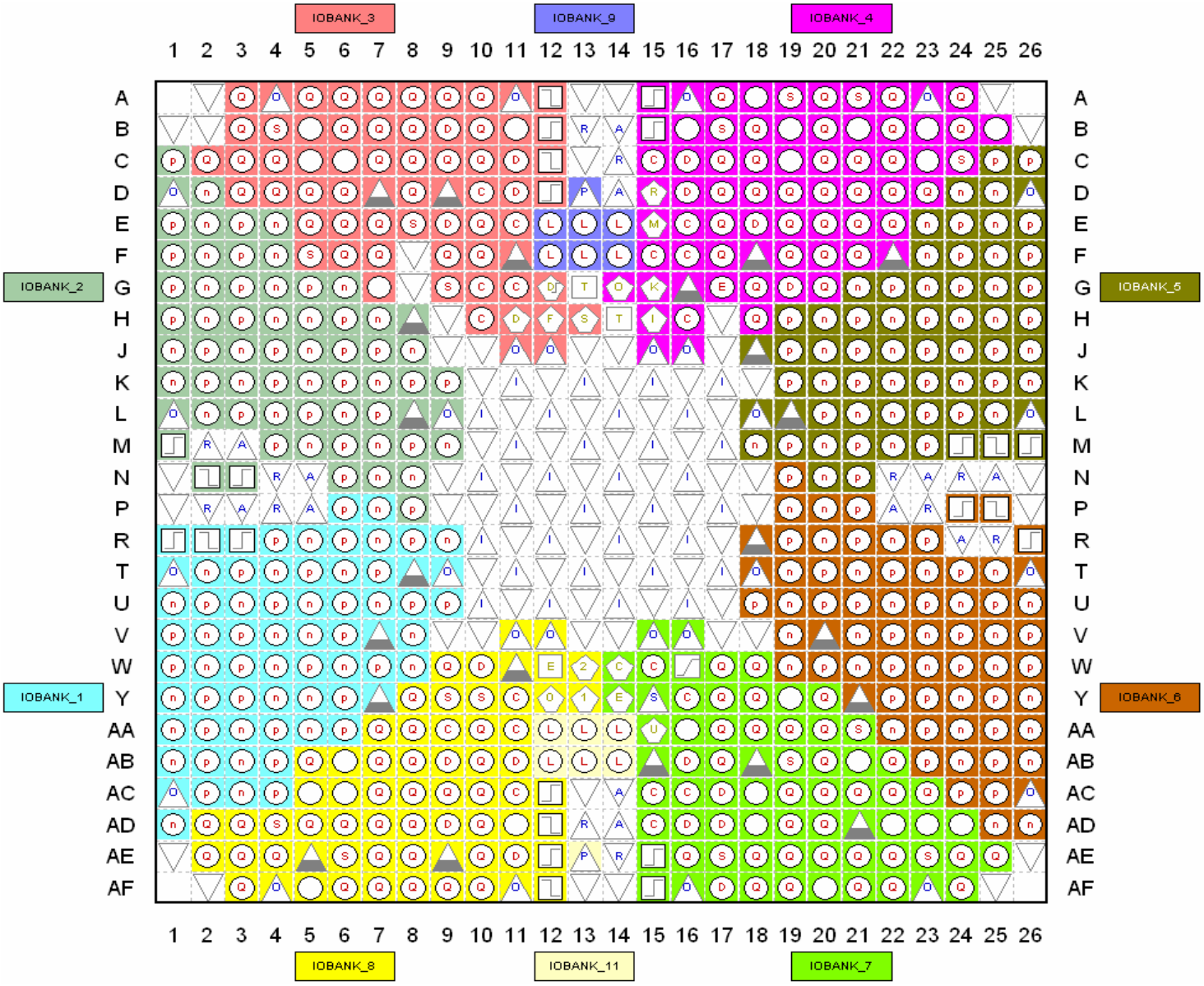
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Clock and PLL Pins	
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you must drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
FCLK[7..0]	Bidirectional	Optional fast regional clock pins. FCLK pins can also be used as type input, output, or as bidirectional pins.
CLK[15..0]p	Input	Dedicated global clock inputs 0 to 15.
CLK[15..0]n	I/O, Input	Optional negative terminal input for differential global clock input.
PLL6_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 6. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL6).
PLL6_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL5_OUT[3..0]p	I/O, Output	Optional external clock outputs [3..0] from enhanced PLL 5. These pins can be differential (four output pin pairs) or single ended (eight clock outputs from PLL5).
PLL5_OUT[3..0]n	I/O, Output	Optional negative terminal for external clock outputs [3..0] from PLL 5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
	Optional/Dual-Purpose Pins	
DATA0	I/O, Input	Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete.
DIFFIO_RX[0..77]p/n	I/O, RX channel	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[0..77]p/n	I/O, TX channel	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
PLL5_FBp	I/O, Input	External feedback input pin for PLL5. This pin can be used as a user I/O pin if external feedback mode is not used.
PLL5_FBn	I/O, Input	Negative terminal input for external feedback input PLL5_FBp
PLL6_FBp	I/O, Input	External feedback input pin for PLL6
PLL6_FBn	I/O, Input	Negative terminal input for external feedback input PLL6_FBp
INIT_DONE	I/O, Output	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
DATA[7..1]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. This pin can be used as a user I/O pin after configuration.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as defined in the users design.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. This pin can be used as a user I/O pin after configuration.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration
nCS,CS	I/O, Input	These are chip-select inputs that enable the Stratix device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
PGM[2..0]	I/O, Output	These output pins control one of eight pages in the EPC16 configuration device when using remote update or local update configuration modes. When not using remote update or local update configuration modes, these pins are user I/O pins.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
RUP[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{UP} must be connected to the designated RUP pin on that I/O bank. If not required, these pins are regular I/O pins.
RDN[8..1]	I/O, Input	Reference pins for banks 8 to 1. The external precision resistors R_{DN} must be connected to the designated RDN pin on that I/O bank. If not required, these pins are regular I/O pins.
RUnLU	I/O, Input	Input control pin to select remote update or local update modes. If MSEL2 = 1, this is a input control pin to select remote update (RUnLU =1) or local update (RUnLU =0) modes. If MSEL2=0, the RUnLU pin is a user I/O pin.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.



Notes:
1.This is a top view of the silicon die. The die is mounted up-side down in flip-chip packages and right-side up in wire-bond packages.
2.This is a pictoral representation only to get an idea of placement on the device. Refer to the pin-list and the Quartus II for exact locations.

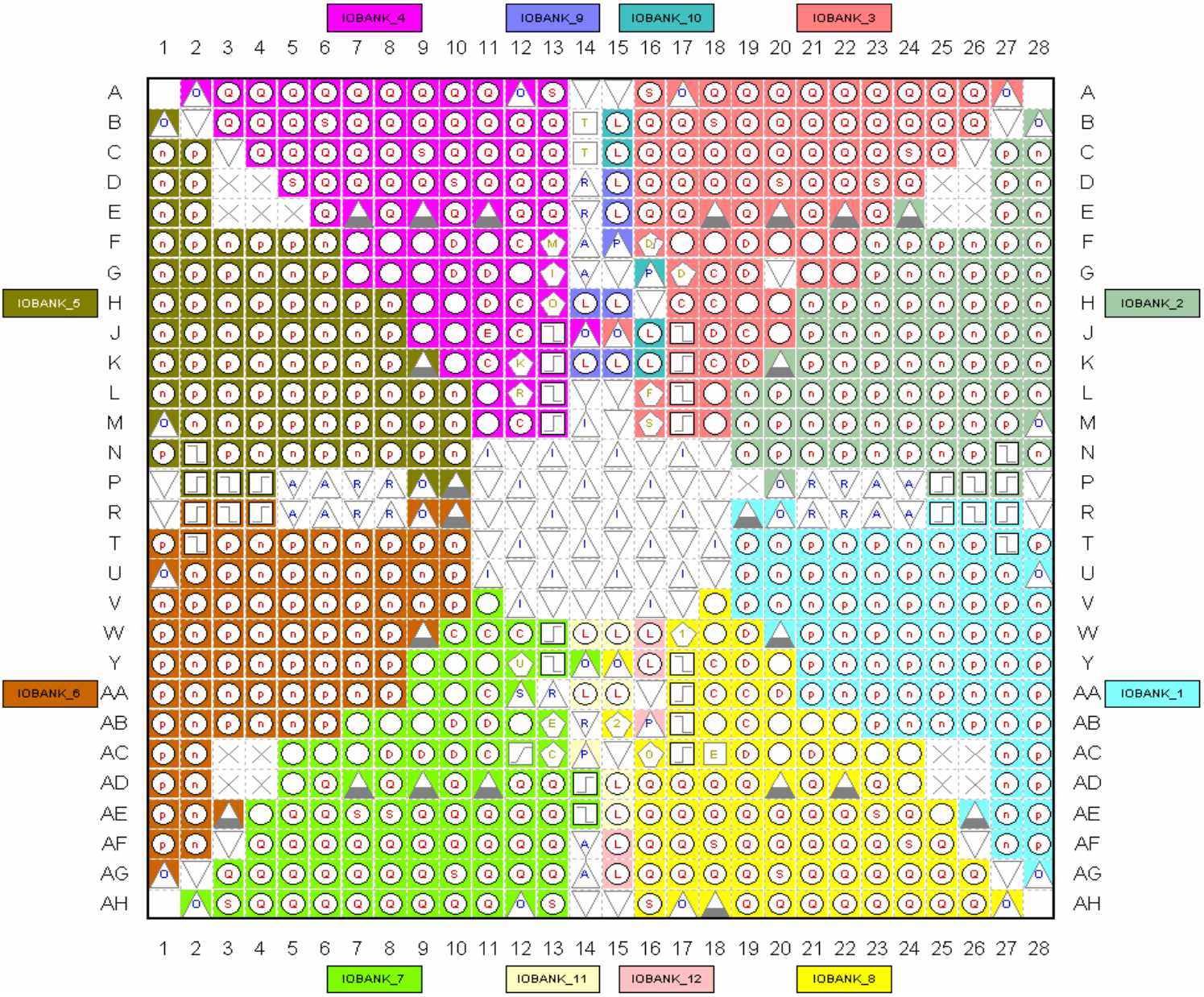
STRATIX EP1S25 B672/F672 Device Package Diagram



USER I/O PINS	DEDICATED PINS		POWER / GROUND PINS
USER IOs	CLK_p	nCEO	VCCA_PLL
DUAL PURPOSE PINS	CLK_n	nCE	VCCINT
OTHER CONFIGURATION	PORSEL	nCONFIG	VCCIO
DEV_OE	PLL_ENA	TDI	VCC_PLL_OUT
DIFF_n	TEMPDIODE	TCK	VCCG_PLL
DIFF_p	MSEL0	TMS	VCCSEL
DQ	MSEL1	TDO	VREF
DQS	MSEL2	TRST	GND
OTHER PLL	CONF_DONE	nSTATUS	GNDA_PLL
OTHER DUAL-PURPOSE	DCLK	nIO_PULLUP	GNDG_PLL
NO CONNECT			

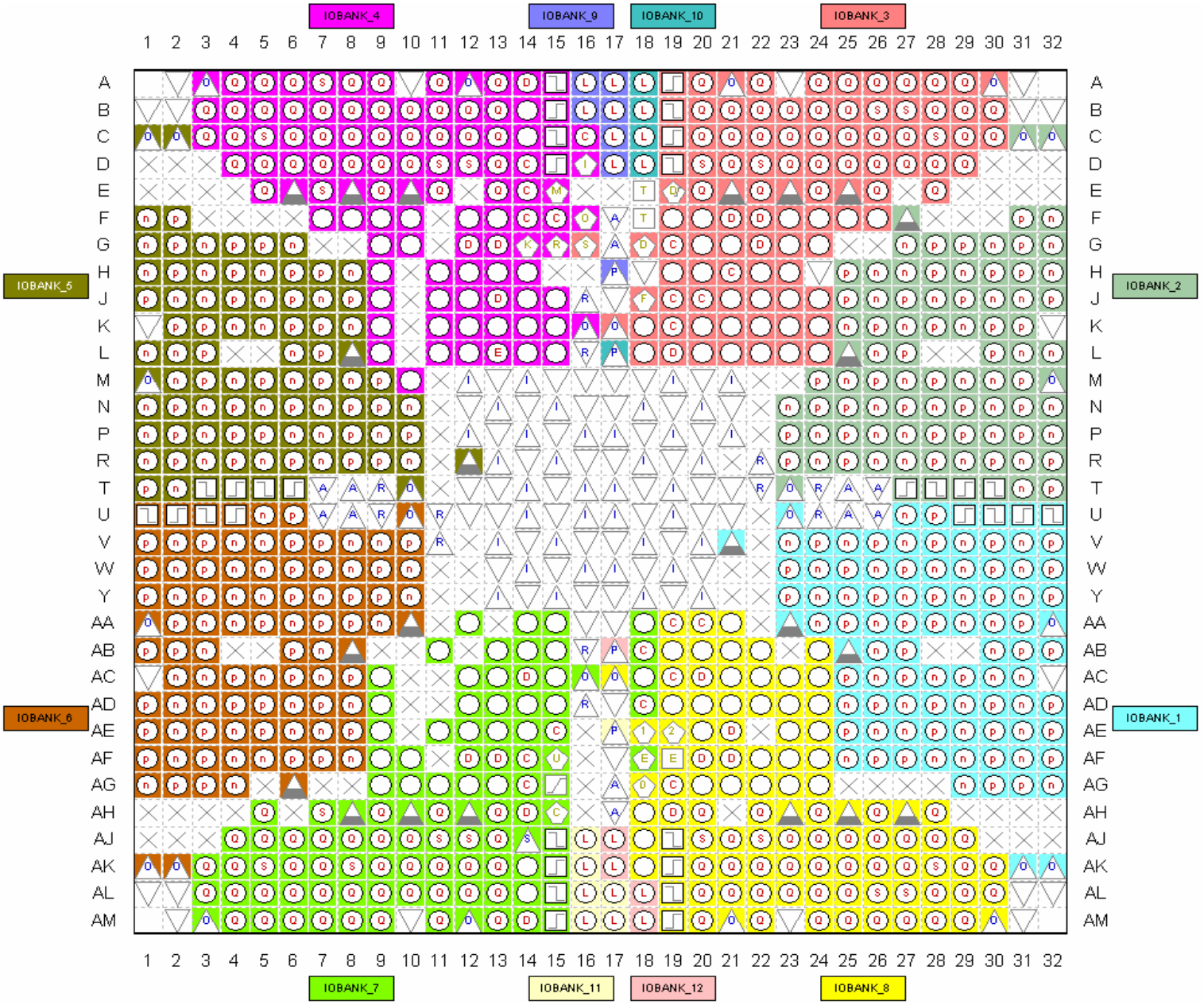
× NO CONNECT			

STRATIX EP1S25 F780 Device Package Diagram



USER I/O PINS	DEDICATED PINS		POWER / GROUND PINS
USER IOs	CLK_p	nCEO	VCCA_PLL
DUAL PURPOSE PINS	CLK_n	nCE	VCCINT
OTHER CONFIGURATION	PORSEL	nCONFIG	VCCIO
DEV_OE	PLL_ENA	TDI	VCC_PLL_OUT
DIFF_n	TEMPDIODE	TCK	VCCG_PLL
DIFF_p	MSEL0	TMS	VCCSEL
DQ	MSEL1	TDO	VREF
DQS	MSEL2	TRST	GND
OTHER PLL	CONF_DONE	nSTATUS	GNDA_PLL
OTHER DUAL-PURPOSE	DCLK	nIO_PULLUP	GNDG_PLL
NO CONNECT			

STRATIX EP1S25 F1020 Device Package Diagram



USER I/O PINS	DEDICATED PINS		POWER / GROUND PINS
USER IOs	CLK_p	nCEO	VCCA_PLL
DUAL PURPOSE PINS	CLK_n	nCE	VCCINT
OTHER CONFIGURATION	PORSEL	nCONFIG	VCCIO
DEV_OE	PLL_ENA	TDI	VCC_PLL_OUT
DIFF_n	TEMPDIODE	TCK	VCCG_PLL
DIFF_p	MSEL0	TMS	VCCSEL
DQ	MSEL1	TDO	VREF
DQS	MSEL2	TRST	GND
OTHER PLL	CONF_DONE	nSTATUS	GNDA_PLL
OTHER DUAL-PURPOSE	DCLK	nIO_PULLUP	GNDG_PLL
NO CONNECT			

× NO CONNECT			

Clock Resources for High Speed Differential I/O (DIFFIO) Receiver and Transmitter channels. *Notes (5),(7)*										
Device	**Pin Count**	**Source FAST PLL**	**Rx Channels** ***Note (1)***		**Tx channels** ***Note (2)***		**Total Rx Channels per PLL** ***Note (3)***		**Total Tx Channels per PLL** ***Note (4)***	
			High ***(6)***	**Low** ***(6)***	**High** ***(6)***	**Low** ***(6)***	**Direct** ***(8)***	**Cross Bank** ***(9)***	**Direct** ***(8)***	**Cross Bank** ***(9)***
EP1S25	672	PLL1	[21-23,25-27,29-31,34-38]	-	[20-21,24-27,30,32-38]	-	14	15	14	14
		PLL2	[0-4,6-8,10,12-14,16-18]	-	[0-5,7-8,12-15,18-19]	-	15	14	14	14
		PLL3	[59-61,63-65,67,69-71,73-77]	-	[58-59,62-65,69-70,72-77]	-	15	14	14	14
		PLL4	[39-43,46-48,50-52,54-56]	-	[39-45,47,50-53,56-57]	-	14	15	14	14
	780	PLL1	[20-36]	-	[20-37]	-	17	16	18	17
		PLL2	[4-19]	-	[3-19]	-	16	17	17	18
		PLL3	[58-73]	-	[58-74]	-	16	17	17	18
		PLL4	[41-57]	-	[40-57]	-	17	16	18	17
	1020	PLL1	[20-38]	-	[20-38]	-	19	20	19	20
		PLL2	[0-19]	-	[0-19]	-	20	19	20	19
		PLL3	[58-77]	-	[58-77]	-	20	19	20	19
		PLL4	[39-57]	-	[39-57]	-	19	20	19	20

Notes:
1. These Rx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.
2. These Tx channels can be clocked by the PLL listed in the "FAST PLL Source location" column.
3. This column shows the total number of Rx channels that can be driven by the PLL listed in the "FAST PLL Source location" column.
4. This column shows the total number of Tx channels that can be driven without by the PLL listed in the "FAST PLL Source location" column.
5. Each range of channel numbers are shown in [ ] brackets.
6. Data channels designated as "high" speed support a maximum data rate of 840 Mbps for -5 and -6 speed grade devices and 624 Mbps for -7 speed grade devices. Data channels designated as "low" speed support a maximum data rate of 462 Mbps for all speed grades.
7. The high speed differential I/O (DIFFIO) channels span across two banks on both sides of the device. Each Fast PLL can normally only feed channels in one bank. However, the center PLLs can also clock the channels associated with the adjacent center PLL on the same side of the device through a mux that is shown in figures 5-16 and 5-17 in volume 2 of the Stratix Device Handbook. These channels are called "cross-bank" channels. When cross-bank channels are used only one center PLL on each side can be used.
8. This column shows the total number of channels in one I/O bank that can be driven by the PLL listed in the "FAST PLL Source location" column.
9. This column shows the total number of cross-bank channels on the same side of the device that can be driven by the PLL the "FAST PLL Source location" column.

Version Number	Date	Changes Made
3.4	2/4/2005	Revised package diagrams.
3.5	11/11/2005	Update all package diagram for EP1S25.
3.6	3/2/2006	Added CRC_ERROR pin in Pin List and Pin Definition