Technical Brief

High-Speed Board Design Advisor
Thermal Management

Introduction

This document contains a step-by-step tutorial and checklist with a best-practice set of step-by-step guidelines to support users to design and review their thermal design with Stratix® II GX FPGAs.

This document assumes familiarity with the following sites, tools, and support collateral:

- *Stratix II GX Handbook*:
  www.altera.com/literature/lit-s2gx.jsp
- Stratix II GX PowerPlay Early Power Estimator (EPE) Spreadsheet and User Guide:
  www.altera.com/support/devices/estimator/pow-powerplay.html
- *Quartus® II Handbook*:
  www.altera.com/literature/lit-qts.jsp
- Power Management Resource Center:
  www.altera.com/support/software/quartus2/power/sof-qts-power.html
- *Package Information for Stratix II GX Devices*:
  www.altera.com/literature/hb/stx2/stx2_sii52010.pdf
- *Altera® Device Package Information*:
  www.altera.com/literature/ds/dspkg.pdf
- *Stratix Series Device Thermal Resistance*:
  www.altera.com/literature/ds/stxthrml.pdf
- *AN 358: Thermal Management for FPGAs:*
  www.altera.com/literature/an/an358.pdf

Altera's Stratix II GX FPGA-based development kits deliver quality-proven implementations and comprise board schematics, layout files, and board-specific guidelines documents that can be used as a starting point for user designs:

- Transceiver Signal Integrity Development Kit, Stratix II GX Edition:
  www.altera.com/products/devkits/altera/kit-signal_integrity_s2gx.html
- PCI Express Development Kit, Stratix II GX Edition:
  www.altera.com/products/devkits/altera/kit-pciexpress_s2gx.html
- Audio Video Development Kit, Stratix II GX Edition:
  www.altera.com/products/devkits/altera/kit-dsp-professional.html

As process technologies shrink and FPGA densities increase, thermal management becomes an important design task. The process involves:

- Specifying the operating conditions
- Estimating the total power consumption
- Determining the necessity of a cooling solution
- Selecting a cooling solution using a heatsink and thermal interface material and/or airflow
- Validating the cooling solution
- Additional topics:
  - Power optimization methods with Quartus II development software
  - Temperature-sensing diode for power management
  - Thermal analysis simulations

Use the EPE Spreadsheet to specify the operating conditions, estimate the power and calculate the junction temperature for a given device, package, or design. The spreadsheet will determine the need of a cooling solution

based on meeting or exceeding the maximum junction temperature. Once selected, use the EPE to validate the cooling solution.

Specifying the Operating Conditions

- Get the latest version of the PowerPlay EPE Spreadsheet.
- At the main tab, select the Stratix II GX device and package combination.
- Select the temperature grade (T_{JMAX}): industrial or commercial (see "Junction Temperature TJ and TJMAX").
- Select maximum power characteristics to get worst-case total power.
- Enter the ambient temperature T_A from the system specification.
- Thermal resistance values are provided by the EPE (see "Thermal Resistance Values for Stratix II GX FPGAs").

Estimate the Total Power Consumption

- Enter or import the design details to get the total power consumption (for guidance, see "Power Analysis—Before Starting the FPGA Design").

Determine the Necessity of a Cooling Solution

- With no heatsink and still air, the tool will tell if the maximum junction temperature is exceeded and if a cooling solution is required. The calculated T_J will turn red when exceeding 85°C for commercial and 100°C for industrial temperature grade.

Select Cooling Solution—Heatsink and Thermal Interface Material and/or Airflow

- Select a cooling solution.

AN 358: Thermal Management for FPGAs gives more information about evaluations of heatsinks and thermal interface materials:
www.altera.com/literature/an/an358.pdf.

- Select a heatsink and thermal interface material vendor (see "Guidance to Select a Cooling Solution").
- Note that the EPE assumes a default case-to-heatsink thermal resistance θ_{CS} = 0.1°C/W (for manual calculation, see "Manual Calculation of Junction Temperature TJ").

Validate the Cooling Solution

- Use the EPE to validate the cooling solution.
- Option 1: Using standard values for heatsink and airflow
  - Heatsink: low (15 mm), medium (23 mm), high (33 mm) profile
  - Airflow: 100 lfm (0.5 m/s), 200 lfm (1.0 m/s), 400 lfm (2.0 m/s)
  - Board thermal model: none (conservative) or typical board
  - Analyze the results under Thermal Analysis in the EPE
- Option 2: Using custom values for heatsink and airflow
  - Heatsink: custom solution
  - Airflow: not applicable, included in θ_{SA}
  - Enter the custom θ_{SA} from the cooling solution
  - Board thermal model: custom
  - Enter the custom θ_{JB} from the board
  - Analyze the results under Thermal Analysis in the EPE

References

Junction Temperature T_J and T_{JMAX}

- Get the maximum junction temperatures T_{JMAX}, T_J from the Stratix II GX DC and Switching Characteristics chapter of the handbook:
  www.altera.com/literature/hb/stx2gx/stxiigx_sii51006.pdf.
  - Stratix II GX device absolute maximum ratings: -55°C < T_J < 125°C
  - Stratix II GX device recommended operating conditions: T_J
- For commercial use: 0°C < T_J < 85°C (T_{JMAX})
- For industrial use: -40°C < T_J < 100°C (T_{JMAX})
  - When selecting the cooling solution, the calculated T_J should not exceed T_{JMAX} for the device's recommended operating condition.

Thermal Resistance Values for Stratix II GX FPGAs

- Get the thermal resistance for the FPGA device and package from the Stratix Series Device Thermal Resistance Data Sheet:
  www.altera.com/literature/ds/stxthrml.pdf.
  - Junction-to-ambient thermal resistance (θ_{JA}) at still air, 100 lfm (0.5 m/s), 200 lfm (1.0 m/s), 400 lfm (2.0 m/s) without a heatsink
  - Junction-to-case thermal resistance (θ_{JC})
  - Junction-to-board thermal resistance (θ_{JB})

Guidance to Select a Cooling Solution

- Select the cooling solution and get the thermal resistance including heatsink and airflow (n).
  - Heatsink-to-ambient thermal resistance (θ_{SA})
- Thermal resistance for thermal interface material from the vendors data sheet (n):
  - Case-to heatsink thermal resistance (θ_{CS})

Manual Calculation of Junction Temperature T_J

- Estimate the board temperature T_B (T_A < T_B < T_J)
  - Worst-case estimation: T_B = T_J
  - Best-case estimation: T_B = T_A
- Calculate T_J using the following formula:

$$T_J = \frac{P \times \theta_{JA} \times \theta_{JB} + T_A \times \theta_{JB} + T_B \times \theta_{JA(Total)}}{\theta_{JA} + \theta_{JB}}, \quad \theta_{JA(Total)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

$\theta_{JA(Total)}$ refers to the total thermal resistance including the heatsink solution. θ_{JA} usually refers to the thermal resistance (junction-to-ambient) from the device package data sheet.

Power Analysis—Before Starting the FPGA Design

- Select Stratix II GX FPGAs as the target family, device, and package.

The Stratix II GX EPE User Guide provides more information on how to enter the information in the EPE:
www.altera.com/support/software/quartus2/power/sof-qts-power.html

- Select the operating conditions, environment conditions, and junction temperature.
- Specify the device resources, operating frequency, and toggle rates of the design.
- The PowerPlay EPE displays the estimated power usage in the Total section.

Power Analysis—While Creating the FPGA Design

- Compile the partial FPGA design in the Quartus II software.
- Generate the PowerPlay EPE file (<revisionname>_early_pwr.csv) in the Quartus II software by clicking Generate PowerPlay Early Power Estimator File in the Project menu.
- Import the PowerPlay EPE file (click on Import Quartus II File) into the PowerPlay EPE spreadsheet to populate the spreadsheet entries automatically.
- After importing the file to populate the PowerPlay EPE, manually edit the cells to reflect final device resource estimates.
- The PowerPlay EPE will display the estimated power usage in the Total section.

PowerPlay Power Analyzer in Quartus II Software

- Compile the FPGA design with realistic timing constraints in the Quartus II software.

The *Power Analysis* chapter of the *Quartus II Handbook* provides more information on using the power analyzer tool:
www.altera.com/literature/hb/qts/qts_qii53013.pdf.

- Simulate the design (preferably with gate-level simulation) and create a signal activity file (**.saf**) or value change dump (**.vcd**) file containing the toggle rate data information of the design, using Quartus II simulator or any supported third-party simulator.
- Specify the operating conditions of the design in Quartus II software from the Assignment menu.
- Choose the PowerPlay Power Analyzer tool from the Processing menu.
- To use the Signal Activity File(s), Value Change Dump File(s), or both as an input to the PowerPlay Power Analyzer, turn on Use Input File(s) to utilize toggle rates and static probabilities during power analysis.
- If the simulation output files are not available, then enter the default toggle rate or use vectorless estimation.
- The PowerPlay Power Analyzer estimates the total thermal power consumption of the design based on input data entered and generates comprehensive power estimation reports.
- Use these power analyzer reports for power planning and power optimization purposes.

PowerPlay Power Optimization

- Use a smaller device that fits the design as it will have less static power consumption.
- Use a better cooling solution, such as a heatsink or airflow, or reduce dynamic or I/O power to reduce the junction temperature. This will result in lower device static power.
- Set the PowerPlay power optimization option value as “Extra effort” for Analysis and Synthesis Settings in Quartus II software. This optimization option allows the synthesis netlist to fully optimize the design for power.
- Set the PowerPlay power optimization option value as “Extra effort” for Fitter Settings in Quartus II software. This setting can be applied only on a project-wide basis and performs place-and-route optimization during fitting to fully optimize the design for power.
- Use area optimization rather than timing or delay optimization to save power.
- Use gate-level register retiming to reduce circuit switching activity.
- Use clock control blocks to dynamically enable or disable the clock networks.
- Use clock enable signals for the memory blocks.
- Use pipelining and retiming for designs with many glitches.

The *Power Optimization* chapter in the *Quartus II Handbook* provides more information on different techniques to further optimize the design for power:
www.altera.com/literature/hb/qts/qts_qii52016.pdf.

Temperature-Sensing Diode for Power Management

Refer to the "Configuration and Testing" chapter of the *Stratix II GX Handbook* (Keyword: *Temperature Sensing Diode*):
www.altera.com/literature/hb/stx2gx/stxiigx_sii51005.pdf.

Thermal Analysis Simulation

- Perform thermal analysis and test design modifications in the early stages of the design process to
  - Solve thermal problems before the hardware is built
  - Reduce design respins and product unit costs
  - Improve reliability and overall engineering design
- Altera provides compact thermal models (CTM) defined by JEDEC, please contact an Altera sales representative for futher information:
  www.altera.com/corporate/contact/con-index.html
  - Two-resistor (2-R) model
  - DELPHI model:
    www.ansys.com
- Thermal simulation tools
  - Flomerics:
    www.flomerics.com
  - Icepak:
    www.icepak.com

Further Information

- Heatsink vendors:
  - Alpha Novatech:
    www.alphanovatech.com
  - Malico Inc.:
    www.malico.com.tw
  - Aavid Thermalloy:
    www.aavidthermalloy.com
  - Wakefield Thermal Solutions:
    www.wakefield.com
  - Radian Heatsinks:
    www.radianheatsinks.com
  - Cool Innovations:
    www.coolinnovations.com
  - Heat Technology, Inc.:
    www.heattechnology.com
- Thermal interface material vendors:
  - Shin-Etsu MicroSi:
    www.microsi.com
  - LORD Corporation:
    www.lord.com
  - Laird Technologies:
    www.lairdtech.com
  - Chomerics:
    www.chomerics.com
  - The Bergquist Company:
    www.bergquistcompany.com

- *High-Speed Board Design Advisor: Power Distribution Network*: **www.altera.com/literature/tb/tb-092.pdf**
- *High-Speed Board Design Advisor: Pinout Definition*: **www.altera.com/literature/tb/tb-094.pdf**
- *High-Speed Board Design Advisor: High-Speed Channel Design and Layout*: **www.altera.com/literature/tb/tb-095.pdf**
- *High-Speed Board Design Advisor: Hardware Integration, Test, and Debug*: **www.altera.com/literature/tb/tb-096.pdf**

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