Pin Name (1)	100-Pin TQFP EPF6016A	100-Pin FineLine BGA EPF6016A	144-Pin TQFP EPF6016A	208-Pin PQFP EPF6016A	256-Pin FineLine BGA EPF6016A
MSEL (2)	22	H2	33	46	L5
nSTATUS (2)	39	G5	56	80	K8
nCONFIG (2)	36	K5	53	77	N8
DCLK (2)	89	D6	128	184	G9
CONF_DONE (2)	72	C9	105	150	F12
INIT_DONE (3)	64	E10	94	135	H13
nCE (2)	4	C2	4	6	F5
nCEO (4)	49	K9	70	102	N12
nWS (4)	81	C7	117	169	F10
nRS (4)	83	A7	120	174	D10
nCS (4)	77	A9	111	159	D12
CS (4)	78	C8	114	162	F11
RDYnBUSY (4)	67	D10	97	140	G13
CLKUSR	69 (4)	C10 (4)	100 (4)	144	F13
DATA (2), (5)	86	A6	125	181	D9
TDI (6)	10	D2	13	19	G5
TDO (6)	51	K10	73	107	N13
TCK	23 (6), (7)	G3 (6), (7)	34 (6), (7)	47	K6
TMS	18 (6)	G2 (6)	27 (6)	38	K5
Dedicated Inputs	12, 13, 62, 63	E1, E2, F9, F10	17, 20, 89, 92	24, 28, 128, 132	H4, H5, J12, J13
DEV_CLRn (3)	91	B5	130	187	E8
DEV_OE (3)	85	B6	123	178	E9
VCCINT	6, 21, 38, 54, 71, 88	D7, E4, E5, F6, F7, G4	6, 31, 77, 103	8, 26, 44, 111, 130, 148	G10, H7, H8, J9, J10, K7
VCCIO	–	–	7, 19, 32, 55, 78, 91, 104, 127	9, 27, 45, 63, 79, 96, 112, 131, 149, 166, 183, 200	B5, B8, C13, C16, E2, G1, J16, N16, P1, P12, R4, R8
GND	5, 20, 37, 53, 70, 87	D4, E6, E7, F4, F5, G7	5, 18, 30, 54, 76, 90, 102, 126	7, 25, 43, 62, 78, 95, 110, 129, 147, 165, 182, 199	A1, A16, B2, B15, G7, J7, J8, K10, P3, H9, H10, R15, T16
No connect (N.C.)	–	–	–	–	A2, A7, A9, A10, A13, A14, B1, B3, B7, B9, B11, B16, C1, C2, C7, D2, D15, D16, E14, F2, G15, G16, H16, J1, J2, K3, L2, L16, M15, N3, N15, P11, P15, R1, R5, R6, R9, R11, R16, T1, T2, T4, T6, T10, T11, T12, T14 (8)
Total user I/O pins (9)	81	81	117	171	171

Notes:
(1) All pins not listed are user I/O pins.
(2) This pin is a dedicated configuration or JTAG pin; therefore, it is not available for use as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its chip-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin. If the JTAG BST circuitry device option is not used, JTAG testing may still be performed before configuration.
(7) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
(8) To maintain pin compatibility when migrating from an EPF6024AF256 device to an EPF6016F256 device, do not use these pins as user I/O pins.
(9) The user I/O count includes dedicated input and I/O pins.