Pin Name (1)	100-Pin TQFP EPF6010A	100-Pin FineLine BGA EPF6010A	144-Pin TQFP EPF6010A
MSEL (2)	22	H2	33
nSTATUS (2)	39	G5	56
nCONFIG (2)	36	K5	53
DCLK (2)	89	D6	128
CONF_DONE (2)	72	C9	105
INIT_DONE (3)	64	E10	94
nCE (2)	4	C2	4
nCEO (4)	49	K9	70
nWS (4)	81	C7	117
nRS (4)	83	A7	120
nCS (4)	77	A9	111
CS (4)	78	C8	114
RDYnBUSY (4)	67	D10	97
CLKUSR	69 (2)	C10 (4)	100 (2)
DATA (2), (5)	86	A6	125
TDI (6)	10	D2	13
TDO (6)	51	K10	73
TCK	23 (2)	G3 (6), (7)	34 (2)
TMS	18 (2)	G2 (6)	27 (2)
Dedicated Inputs	12, 13, 62, 63	E1, E2, F9, F10	17, 20, 89, 92
DEV_CLRn (3)	91	B5	130
DEV_OE (3)	85	B6	123
VCCINT	6, 21, 38, 54, 71, 88	D7, E4, E5, F6, F7, G4	6, 31, 77, 103
VCCIO	–	–	7, 19, 32, 55, 78, 91, 104, 127
GND	5, 20, 37, 53, 70, 87	D4, E6, E7, F4, F5, G7	5, 18, 30, 54, 76, 90, 102, 126
No connect (N.C.)	3, 7, 19, 52, 55, 56, 68 (8)	–	3, 8, 9, 28, 29, 74, 75, 79, 80, 98, 99, 101 (9)
Total user I/O pins (10)	71	81	102

Notes:
(1) All pins not listed are user I/O pins.
(2) This pin is a dedicated configuration or JTAG pin; therefore, it is not available for use as a user I/O pin.
(3) This pin can be used as a user I/O pin if it is not used for its chip-wide or configuration function.
(4) This pin can be used as a user I/O pin after configuration.
(5) This pin is tri-stated in user mode.
(6) If the device is not configured to use the JTAG BST circuitry, this pin is available as a user I/O pin. If the JTAG BST circuitry device option is not used, JTAG testing may still be performed before configuration.
(7) If this pin is used as an input in user mode, ensure that it does not toggle before or during configuration.
(8) To maintain pin compatibility when migrating from an EPF6016AT100 device to an EPF6010AT100 device, do not use these pin as user I/O pins.
(9) To maintain pin compatibility when migrating to an EPF6010AT144 from a larger device, do not use these pins as user I/O pins.
(10) The user I/O count includes dedicated input and I/O pins.