Table 1 shows output standards and the associated drive strength settings for note 21.

Table 1. Output Standard & Drive Strength Support for Note 21	
Output Standard	**Drive Strength**
LVTTL (3.3 V)	4 mA
	8 mA
	12 mA
	16 mA
	24 mA
LVTTL (2.5 V)	4 mA
	8 mA
	12 mA
	16 mA
LVTTL (1.8 V)	2 mA
	4 mA
SSTL-3 class I and II	Minimum
SSTL-2 class I and II	Minimum

Table 2 shows all pins for the EP1M350 780-pin FineLine BGA package.

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
1	-	HSDI_CLK1n	-	-	A13
1	-	HSDI_CLK1p	-	-	B13
1	VREF1	IO (21)	HSDI_RX1p	-	A3
1	VREF1	IO (21)	HSDI_RX2n	-	B4
1	VREF1	IO (21)	HSDI_RX3p	-	A5
1	VREF1	IO (21)	HSDI_RX4n	-	B6
1	VREF1	IO (21)	HSDI_RX5p	-	A7
1	VREF1	IO (21)	HSDI_RX6n	-	B9
1	VREF1	IO (21)	HSDI_RX7p	-	A10
1	VREF1	IO (21)	HSDI_RX8n	-	B11
1	VREF1	IO (21)	HSDI_RX9p	-	A12
1	VREF1	IO (21)	HSDI_RX1n	-	B3
1	VREF1	IO (21)	HSDI_RX2p	-	A4
1	VREF1	IO (21)	HSDI_RX3n	-	B5
1	VREF1	IO (21)	HSDI_RX4p	-	A6
1	VREF1	IO (21)	HSDI_RX5n	-	B7
1	VREF1	IO (21)	HSDI_RX6p	-	A9
1	VREF1	IO (21)	HSDI_RX7n	-	B10
1	VREF1	IO (21)	HSDI_RX8p	-	A11
1	VREF1	IO (21)	HSDI_RX9n	-	B12
1	VREF1	IO (21)	VREF1 (5)	-	M10
3	-	HSDI_CLK2n	-	-	B16
3	-	HSDI_CLK2p	-	-	A16
3	VREF3	IO (21)	HSDI_RX10n	-	B17

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
3	VREF3	IO (21)	HSDI_RX11p	-	A18
3	VREF3	IO (21)	HSDI_RX12n	-	B19
3	VREF3	IO (21)	HSDI_RX13p	-	A20
3	VREF3	IO (21)	HSDI_RX14n	-	B22
3	VREF3	IO (21)	HSDI_RX15p	-	A23
3	VREF3	IO (21)	HSDI_RX16n	-	B24
3	VREF3	IO (21)	HSDI_RX17p	-	A25
3	VREF3	IO (21)	HSDI_RX18n	-	B26
3	VREF3	IO (21)	HSDI_RX10p	-	A17
3	VREF3	IO (21)	HSDI_RX11n	-	B18
3	VREF3	IO (21)	HSDI_RX12p	-	A19
3	VREF3	IO (21)	HSDI_RX13n	-	B20
3	VREF3	IO (21)	HSDI_RX14p	-	A22
3	VREF3	IO (21)	HSDI_RX15n	-	B23
3	VREF3	IO (21)	HSDI_RX16p	-	A24
3	VREF3	IO (21)	HSDI_RX17n	-	B25
3	VREF3	IO (21)	HSDI_RX18p	-	A26
3	VREF3	IO (21)	VREF3 (5)	-	K15
2	-	HSDI_TXCLKOUT1n	-	-	K14
2	-	HSDI_TXCLKOUT1p	-	-	L14
2	VREF2	IO	VREF2 (5)	-	N10
2	VREF2	IO	HSDI_TX1n	-	K5
2	VREF2	IO	HSDI_TX2p	-	L6
2	VREF2	IO	HSDI_TX3n	-	K7
2	VREF2	IO	HSDI_TX4p	-	L8
2	VREF2	IO	HSDI_TX5n	-	K9
2	VREF2	IO	HSDI_TX6p	-	L10
2	VREF2	IO	HSDI_TX7n	-	K11
2	VREF2	IO	HSDI_TX8p	-	L12
2	VREF2	IO	HSDI_TX9n	-	K13
2	VREF2	IO	HSDI_TX1p	-	L5
2	VREF2	IO	HSDI_TX2n	-	K6
2	VREF2	IO	HSDI_TX3p	-	L7
2	VREF2	IO	HSDI_TX4n	-	K8
2	VREF2	IO	HSDI_TX5p	-	L9
2	VREF2	IO	HSDI_TX6n	-	K10
2	VREF2	IO	HSDI_TX7p	-	L11
2	VREF2	IO	HSDI_TX8n	-	K12
2	VREF2	IO	HSDI_TX9p	-	L13
4	VREF4	IO	VREF4 (5)	-	L15
4	VREF4	IO	HSDI_TX10p	-	L16

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
4	VREF4	IO	HSDI_TX11n	-	K17
4	VREF4	IO	HSDI_TX12p	-	L18
4	VREF4	IO	HSDI_TX13n	-	K19
4	VREF4	IO	HSDI_TX14p	-	L20
4	VREF4	IO	HSDI_TX15n	-	K21
4	VREF4	IO	HSDI_TX16p	-	L22
4	VREF4	IO	HSDI_TX17n	-	K23
4	VREF4	IO	HSDI_TX18p	-	L24
4	VREF4	IO	HSDI_TX10n	-	K16
4	VREF4	IO	HSDI_TX11p	-	L17
4	VREF4	IO	HSDI_TX12n	-	K18
4	VREF4	IO	HSDI_TX13p	-	L19
4	VREF4	IO	HSDI_TX14n	-	K20
4	VREF4	IO	HSDI_TX15p	-	L21
4	VREF4	IO	HSDI_TX16n	-	K22
4	VREF4	IO	HSDI_TX17p	-	L23
4	VREF4	IO	HSDI_TX18n	-	K24
5	-	CLK3n	CLK3VREF	-	T14
5	-	CLK3p	-	-	R14
5	-	CLK4n	CLK4VREF	-	T13
5	-	CLK4p	-	-	R13
5	-	CLKLK_FB3n	CLKLK_FB3VREF	-	AB11
5	-	CLKLK_FB3p (11), (18)	-	-	AB10
5	-	CLKLK_FB4n	CLKLK_FB4VREF	-	E10
5	-	CLKLK_FB4p (11), (18)	-	-	E9
5	VREF5	IO	-	FlexDiff_RX17n	T3
5	VREF5	IO	-	FlexDiff_RX19n	T1
5	VREF5	IO	-	FlexDiff_RX23n	J4
5	VREF5	IO	-	FlexDiff_RX23p	J3
5	VREF5	IO	-	FlexDiff_RX24n	D6
5	VREF5	IO	-	FlexDiff_RX24p	C6
5	VREF5	IO	-	FlexDiff_RX25n	D9
5	VREF5	IO	-	FlexDiff_RX25p	C9
5	VREF5	IO	-	FlexDiff_RX26n	D11
5	VREF5	IO	-	FlexDiff_RX26p	C11
5	VREF5	IO	-	FlexDiff_RX27n	C4
5	VREF5	IO	DEV_CLRn (8)	FlexDiff_RX27p	C3
5	VREF5	IO	INIT_DONE (8)	FlexDiff_RX28n	D3
5	VREF5	IO	nRS (7)	FlexDiff_RX28p	D4
5	VREF5	IO	CS (7)	FlexDiff_RX29n	E3
5	VREF5	IO	CLKUSR (7)	FlexDiff_RX29p	E4

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
5	VREF5	IO	DATA2 (7)	FlexDiff_RX30n	D1
5	VREF5	IO	DATA4 (7)	FlexDiff_RX30p	D2
5	VREF5	IO	DATA5 (7)	FlexDiff_RX31n	E1
5	VREF5	IO	DATA1 (7)	FlexDiff_RX31p	E2
5	VREF5	IO	-	FlexDiff_TX17n	L3
5	VREF5	IO	-	FlexDiff_TX19n	M2
5	VREF5	IO	-	FlexDiff_TX20n	R4
5	VREF5	IO	-	FlexDiff_TX20p	P4
5	VREF5	IO	-	FlexDiff_TX21n	C7
5	VREF5	IO	-	FlexDiff_TX21p	D7
5	VREF5	IO	-	FlexDiff_TX22n	C10
5	VREF5	IO	-	FlexDiff_TX22p	D10
5	VREF5	IO	-	FlexDiff_TX23n	C12
5	VREF5	IO	-	FlexDiff_TX23p	D12
5	VREF5	IO	LOCK4 (10)	FlexDiff_TX24n	C5
5	VREF5	IO	VREF5 (5)	FlexDiff_TX24p	D5
5	VREF5	IO	DEV_OE (8)	FlexDiff_TX25n	F4
5	VREF5	IO	RDYnBSY (7)	FlexDiff_TX25p	F3
5	VREF5	IO	nCS (7)	FlexDiff_TX26n	G4
5	VREF5	IO	nWS (7)	FlexDiff_TX26p	G3
5	VREF5	IO	DATA7 (7)	FlexDiff_TX27n	F2
5	VREF5	IO	DATA6 (7)	FlexDiff_TX27p	F1
5	VREF5	IO	DATA3 (7)	FlexDiff_TX28n	G2
5	VREF5	IO	-	FlexDiff_TX28p	G1
6	VREF6	IO	-	-	P5
6	VREF6	IO	FAST_ROW2 (6)	-	P13
6	VREF6	IO	VREF6 (5)	-	H5
6	VREF6	IO	-	FlexDiff_RX16n	N3
6	VREF6	IO	-	FlexDiff_RX16p	N4
6	VREF6	IO	-	FlexDiff_RX17p	T4
6	VREF6	IO	-	FlexDiff_RX18n	N1
6	VREF6	IO	-	FlexDiff_RX18p	N2
6	VREF6	IO	-	FlexDiff_RX19p	T2
6	VREF6	IO	-	FlexDiff_RX20n	K3
6	VREF6	IO	-	FlexDiff_RX20p	K4
6	VREF6	IO	-	FlexDiff_RX21n	J1
6	VREF6	IO	-	FlexDiff_RX21p	J2
6	VREF6	IO	-	FlexDiff_RX22n	K1
6	VREF6	IO	-	FlexDiff_RX22p	K2
6	VREF6	IO	-	FlexDiff_TX16n	M4
6	VREF6	IO	-	FlexDiff_TX16p	M3

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
6	VREF6	IO	-	FlexDiff_TX17p	L4
6	VREF6	IO	-	FlexDiff_TX18n	L2
6	VREF6	IO	-	FlexDiff_TX18p	L1
6	VREF6	IO	-	FlexDiff_TX19p	M1
7	-	CLK1n	CLK1VREF	-	T16
7	-	CLK1p	-	-	R16
7	-	CLK2n	CLK2VREF	-	T15
7	-	CLK2p	-	-	R15
7	-	CLKLK_FB1n	CLKLK_FB1VREF	-	E19
7	-	CLKLK_FB1p (11), (18)	-	-	E20
7	-	CLKLK_FB2n	CLKLK_FB2VREF	-	AB18
7	-	CLKLK_FB2p (11), (18)	-	-	AB19
7	VREF7	IO	-	-	P17
7	VREF7	IO	FAST_ROW1 (6)	-	P16
7	VREF7	IO	-	FlexDiff_RX11n	J25
7	VREF7	IO	-	FlexDiff_RX11p	J26
7	VREF7	IO	-	FlexDiff_RX12n	K25
7	VREF7	IO	-	FlexDiff_RX12p	K26
7	VREF7	IO	-	FlexDiff_RX13n	N27
7	VREF7	IO	-	FlexDiff_RX13p	N28
7	VREF7	IO	-	FlexDiff_RX14n	N25
7	VREF7	IO	-	FlexDiff_RX14p	N26
7	VREF7	IO	-	FlexDiff_RX15n	P20
7	VREF7	IO	-	FlexDiff_RX15p	N19
7	VREF7	IO	-	FlexDiff_RX10n	K27
7	VREF7	IO	-	FlexDiff_RX10p	K28
7	VREF7	IO	-	FlexDiff_TX11n	L26
7	VREF7	IO	-	FlexDiff_TX11p	L25
7	VREF7	IO	-	FlexDiff_TX12n	M26
7	VREF7	IO	-	FlexDiff_TX12p	M25
7	VREF7	IO	-	FlexDiff_TX13n	T28
7	VREF7	IO	-	FlexDiff_TX13p	T27
7	VREF7	IO	-	FlexDiff_TX14n	N21
7	VREF7	IO	VREF7 (5)	FlexDiff_TX14p	P21
7	VREF7	IO	-	FlexDiff_TX15n	P18
7	VREF7	IO	-	FlexDiff_TX15p	P19
7	VREF7	IO	-	FlexDiff_TX10n	L27
7	VREF7	IO	-	FlexDiff_TX10p	L28
8	VREF8	IO	LOCK1 (10)	FlexDiff_RX1n	D17
8	VREF8	IO	-	FlexDiff_RX1p	C17
8	VREF8	IO	-	FlexDiff_RX2n	D19

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
8	VREF8	IO	-	FlexDiff_RX2p	C19
8	VREF8	IO	-	FlexDiff_RX3n	D22
8	VREF8	IO	-	FlexDiff_RX3p	C22
8	VREF8	IO	-	FlexDiff_RX4n	D24
8	VREF8	IO	-	FlexDiff_RX4p	C24
8	VREF8	IO	-	FlexDiff_RX5n	D27
8	VREF8	IO	-	FlexDiff_RX5p	D28
8	VREF8	IO	-	FlexDiff_RX6n	E27
8	VREF8	IO	-	FlexDiff_RX6p	E28
8	VREF8	IO	-	FlexDiff_RX7n	D25
8	VREF8	IO	-	FlexDiff_RX7p	D26
8	VREF8	IO	-	FlexDiff_RX8n	E25
8	VREF8	IO	-	FlexDiff_RX8p	E26
8	VREF8	IO	-	FlexDiff_RX9n	J27
8	VREF8	IO	-	FlexDiff_RX9p	J28
8	VREF8	IO	-	FlexDiff_TX1n	C18
8	VREF8	IO	-	FlexDiff_TX1p	D18
8	VREF8	IO	-	FlexDiff_TX2n	C20
8	VREF8	IO	-	FlexDiff_TX2p	D20
8	VREF8	IO	-	FlexDiff_TX3n	C23
8	VREF8	IO	-	FlexDiff_TX3p	D23
8	VREF8	IO	-	FlexDiff_TX4n	C25
8	VREF8	IO	VREF8 (5)	FlexDiff_TX4p	C26
8	VREF8	IO	-	FlexDiff_TX5n	G28
8	VREF8	IO	-	FlexDiff_TX5p	G27
8	VREF8	IO	-	FlexDiff_TX6n	F27
8	VREF8	IO	-	FlexDiff_TX6p	F28
8	VREF8	IO	-	FlexDiff_TX7n	G25
8	VREF8	IO	-	FlexDiff_TX7p	G26
8	VREF8	IO	-	FlexDiff_TX8n	F25
8	VREF8	IO	-	FlexDiff_TX8p	F26
8	VREF8	IO	-	FlexDiff_TX9n	M27
8	VREF8	IO	-	FlexDiff_TX9p	M28
9	VREF9	IO	-	FlexDiff_RX55n	P8
9	VREF9	IO	-	FlexDiff_RX55p	N7
9	VREF9	IO	-	FlexDiff_RX56n	V6
9	VREF9	IO	-	FlexDiff_RX56p	U6
9	VREF9	IO	-	FlexDiff_RX57n	V5
9	VREF9	IO	-	FlexDiff_RX57p	U5
9	VREF9	IO	-	FlexDiff_RX58n	U3
9	VREF9	IO	-	FlexDiff_RX58p	U4

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
9	VREF9	IO	-	FlexDiff_RX59n	V4
9	VREF9	IO	-	FlexDiff_RX59p	V3
9	VREF9	IO	-	FlexDiff_RX60n	U1
9	VREF9	IO	-	FlexDiff_RX60p	U2
9	VREF9	IO	-	FlexDiff_RX61n	V1
9	VREF9	IO	-	FlexDiff_RX61p	V2
9	VREF9	IO	-	FlexDiff_RX62n	P7
9	VREF9	IO	-	FlexDiff_RX62p	N6
9	VREF9	IO	-	FlexDiff_RX63n	P6
9	VREF9	IO	-	FlexDiff_RX63p	N5
9	VREF9	IO	-	FlexDiff_TX56n	R7
9	VREF9	IO	-	FlexDiff_TX56p	T7
9	VREF9	IO	-	FlexDiff_TX57n	W6
9	VREF9	IO	-	FlexDiff_TX57p	Y6
9	VREF9	IO	-	FlexDiff_TX58n	W5
9	VREF9	IO	-	FlexDiff_TX58p	Y5
9	VREF9	IO	-	FlexDiff_TX59n	W4
9	VREF9	IO	-	FlexDiff_TX59p	W3
9	VREF9	IO	-	FlexDiff_TX60n	Y4
9	VREF9	IO	VREF9 (5)	FlexDiff_TX60p	Y3
9	VREF9	IO	-	FlexDiff_TX61n	W2
9	VREF9	IO	-	FlexDiff_TX61p	W1
9	VREF9	IO	-	FlexDiff_TX62n	Y2
9	VREF9	IO	-	FlexDiff_TX62p	Y1
9	VREF9	IO	-	FlexDiff_TX63n	R6
9	VREF9	IO	-	FlexDiff_TX63p	T6
9	VREF9	IO	-	FlexDiff_TX64n	R5
9	VREF9	IO	-	FlexDiff_TX64p	T5
10	VREF10	IO	-	-	P12
10	VREF10	IO	-	-	P11
10	VREF10	IO	-	-	P10
10	VREF10	IO	FAST4 (9)	FlexDiff_RX49n	R12
10	VREF10	IO	FAST6 (9)	FlexDiff_RX49p	T12
10	VREF10	IO	-	FlexDiff_RX50n	V13
10	VREF10	IO	-	FlexDiff_RX50p	V12
10	VREF10	IO	-	FlexDiff_RX51n	Y14
10	VREF10	IO	-	FlexDiff_RX51p	W14
10	VREF10	IO	-	FlexDiff_RX52n	T10
10	VREF10	IO	-	FlexDiff_RX52p	R10
10	VREF10	IO	-	FlexDiff_RX53n	T9
10	VREF10	IO	-	FlexDiff_RX53p	R9

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
10	VREF10	IO	-	FlexDiff_RX54n	T8
10	VREF10	IO	-	FlexDiff_RX54p	R8
10	VREF10	IO	FAST_ROW4 (6)	FlexDiff_TX47n	U14
10	VREF10	IO	FAST5 (9)	FlexDiff_TX47p	V14
10	VREF10	IO	-	FlexDiff_TX48n	W13
10	VREF10	IO	-	FlexDiff_TX48p	Y13
10	VREF10	IO	-	FlexDiff_TX49n	W12
10	VREF10	IO	-	FlexDiff_TX49p	Y12
10	VREF10	IO	-	FlexDiff_TX50n	R11
10	VREF10	IO	VREF10 (5)	FlexDiff_TX50p	T11
10	VREF10	IO	-	FlexDiff_TX51n	W11
10	VREF10	IO	-	FlexDiff_TX51p	Y11
10	VREF10	IO	-	FlexDiff_TX52n	W10
10	VREF10	IO	-	FlexDiff_TX52p	Y10
10	VREF10	IO	-	FlexDiff_TX53n	N8
10	VREF10	IO	-	FlexDiff_TX53p	P9
10	VREF10	IO	-	FlexDiff_TX54n	W9
10	VREF10	IO	-	FlexDiff_TX54p	Y9
10	VREF10	IO	-	FlexDiff_TX55n	W7
10	VREF10	IO	-	FlexDiff_TX55p	W8
11	VREF11	IO	-	FlexDiff_RX41n	V24
11	VREF11	IO	-	FlexDiff_RX41p	V23
11	VREF11	IO	-	FlexDiff_RX42n	U24
11	VREF11	IO	-	FlexDiff_RX42p	U23
11	VREF11	IO	-	FlexDiff_RX43n	T21
11	VREF11	IO	-	FlexDiff_RX43p	R21
11	VREF11	IO	-	FlexDiff_RX44n	T20
11	VREF11	IO	-	FlexDiff_RX44p	R20
11	VREF11	IO	-	FlexDiff_RX45n	T19
11	VREF11	IO	-	FlexDiff_RX45p	R19
11	VREF11	IO	-	FlexDiff_RX46n	T18
11	VREF11	IO	-	FlexDiff_RX46p	R18
11	VREF11	IO	-	FlexDiff_RX47.n	Y15
11	VREF11	IO	-	FlexDiff_RX47p	W15
11	VREF11	IO	FAST1 (9)	FlexDiff_RX48n	R17
11	VREF11	IO	FAST3 (9)	FlexDiff_RX48p	T17
11	VREF11	IO	-	FlexDiff_TX38n	Y23
11	VREF11	IO	-	FlexDiff_TX38p	Y24
11	VREF11	IO	-	FlexDiff_TX39n	W23
11	VREF11	IO	-	FlexDiff_TX39p	W24
11	VREF11	IO	-	FlexDiff_TX40n	W21

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
11	VREF11	IO	-	FlexDiff_TX40p	W22
11	VREF11	IO	-	FlexDiff_TX41n	W20
11	VREF11	IO	-	FlexDiff_TX41p	Y20
11	VREF11	IO	-	FlexDiff_TX42n	W19
11	VREF11	IO	VREF11 (5)	FlexDiff_TX42p	Y19
11	VREF11	IO	-	FlexDiff_TX43n	W18
11	VREF11	IO	-	FlexDiff_TX43p	Y18
11	VREF11	IO	-	FlexDiff_TX44n	W17
11	VREF11	IO	-	FlexDiff_TX44p	Y17
11	VREF11	IO	-	FlexDiff_TX45n	W16
11	VREF11	IO	-	FlexDiff_TX45p	Y16
11	VREF11	IO	FAST2 (9)	FlexDiff_TX46n	U15
11	VREF11	IO	FAST_ROW3 (6)	FlexDiff_TX46p	V15
12	VREF12	IO	-	FlexDiff_RX32n	T25
12	VREF12	IO	-	FlexDiff_RX32p	T26
12	VREF12	IO	-	FlexDiff_RX33n	N23
12	VREF12	IO	-	FlexDiff_RX33p	N24
12	VREF12	IO	-	FlexDiff_RX34n	P23
12	VREF12	IO	-	FlexDiff_RX34p	P24
12	VREF12	IO	-	FlexDiff_RX35n	P22
12	VREF12	IO	-	FlexDiff_RX35p	N22
12	VREF12	IO	-	FlexDiff_RX36n	U27
12	VREF12	IO	-	FlexDiff_RX36p	U28
12	VREF12	IO	-	FlexDiff_RX37n	V27
12	VREF12	IO	-	FlexDiff_RX37p	V28
12	VREF12	IO	-	FlexDiff_RX38n	U25
12	VREF12	IO	-	FlexDiff_RX38p	U26
12	VREF12	IO	-	FlexDiff_RX39n	V25
12	VREF12	IO	-	FlexDiff_RX39p	V26
12	VREF12	IO	-	FlexDiff_RX40n	AA25
12	VREF12	IO	-	FlexDiff_RX40p	AA24
12	VREF12	IO	-	FlexDiff_TX29n	R25
12	VREF12	IO	-	FlexDiff_TX29p	P25
12	VREF12	IO	-	FlexDiff_TX30n	R24
12	VREF12	IO	-	FlexDiff_TX30p	R23
12	VREF12	IO	-	FlexDiff_TX31n	T24
12	VREF12	IO	-	FlexDiff_TX31p	T23
12	VREF12	IO	-	FlexDiff_TX32n	R22
12	VREF12	IO	VREF12 (5)	FlexDiff_TX32p	T22
12	VREF12	IO	-	FlexDiff_TX33n	W28
12	VREF12	IO	-	FlexDiff_TX33p	W27

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
12	VREF12	IO	-	FlexDiff_TX34n	Y28
12	VREF12	IO	-	FlexDiff_TX34p	Y27
12	VREF12	IO	-	FlexDiff_TX35n	W26
12	VREF12	IO	-	FlexDiff_TX35p	W25
12	VREF12	IO	-	FlexDiff_TX36n	Y26
12	VREF12	IO	-	FlexDiff_TX36p	Y25
12	VREF12	IO	-	FlexDiff_TX37n	AB25
12	VREF12	IO	-	FlexDiff_TX37p	AB26
13	VREF13	IO	-	FlexDiff_RX92n	AG5
13	VREF13	IO	-	FlexDiff_RX92p	AH5
13	VREF13	IO	-	FlexDiff_RX93n	AG4
13	VREF13	IO	-	FlexDiff_RX93p	AH4
13	VREF13	IO	-	FlexDiff_RX94n	AG3
13	VREF13	IO	-	FlexDiff_RX94p	AH3
13	VREF13	IO	-	FlexDiff_RX95n	AC5
13	VREF13	IO	-	FlexDiff_RX95p	AD5
13	VREF13	IO	-	FlexDiff_RX96n	AD3
13	VREF13	IO	-	FlexDiff_RX96p	AD4
13	VREF13	IO	-	FlexDiff_RX97n	AC3
13	VREF13	IO	-	FlexDiff_RX97p	AC4
13	VREF13	IO	-	FlexDiff_RX98n	AD2
13	VREF13	IO	-	FlexDiff_RX98p	AD1
13	VREF13	IO	-	FlexDiff_RX99n	AE2
13	VREF13	IO	-	FlexDiff_RX99p	AE1
13	VREF13	IO	-	FlexDiff_RX91n	AG6
13	VREF13	IO	-	FlexDiff_RX91p	AH6
13	VREF13	IO	-	FlexDiff_TX93n	AF5
13	VREF13	IO	-	FlexDiff_TX93p	AE5
13	VREF13	IO	-	FlexDiff_TX94n	AF4
13	VREF13	IO	-	FlexDiff_TX94p	AE4
13	VREF13	IO	-	FlexDiff_TX95n	AF3
13	VREF13	IO	-	FlexDiff_TX95p	AE3
13	VREF13	IO	-	FlexDiff_TX96n	AC6
13	VREF13	IO	VREF13 (5)	FlexDiff_TX96p	AB5
13	VREF13	IO	-	FlexDiff_TX97n	AA5
13	VREF13	IO	-	FlexDiff_TX97p	AA4
13	VREF13	IO	-	FlexDiff_TX98n	AB4
13	VREF13	IO	-	FlexDiff_TX98p	AB3
13	VREF13	IO	-	FlexDiff_TX99n	AB1
13	VREF13	IO	-	FlexDiff_TX99p	AB2
13	VREF13	IO	-	FlexDiff_TX100n	AC1

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
13	VREF13	IO	LOCK3 (10)	FlexDiff_TX100p	AC2
13	VREF13	IO	-	FlexDiff_TX92n	AF6
13	VREF13	IO	-	FlexDiff_TX92p	AE6
14	VREF14	IO	FAST_ROW6 (6)	FlexDiff_RX82n	AC14
14	VREF14	IO	-	FlexDiff_RX82p	AD14
14	VREF14	IO	-	FlexDiff_RX83n	AG13
14	VREF14	IO	-	FlexDiff_RX83p	AH13
14	VREF14	IO	-	FlexDiff_RX84n	AG12
14	VREF14	IO	-	FlexDiff_RX84p	AH12
14	VREF14	IO	-	FlexDiff_RX85p	AH11
14	VREF14	IO	-	FlexDiff_RX86n	AD9
14	VREF14	IO	-	FlexDiff_RX86p	AD10
14	VREF14	IO	-	FlexDiff_RX87p	AH10
14	VREF14	IO	-	FlexDiff_RX88n	AG9
14	VREF14	IO	-	FlexDiff_RX88p	AH9
14	VREF14	IO	-	FlexDiff_RX89n	AD6
14	VREF14	IO	-	FlexDiff_RX89p	AD7
14	VREF14	IO	-	FlexDiff_RX90n	AG7
14	VREF14	IO	-	FlexDiff_RX90p	AH7
14	VREF14	IO	-	FlexDiff_TX83n	AF14
14	VREF14	IO	-	FlexDiff_TX83p	AE14
14	VREF14	IO	-	FlexDiff_TX84n	AF13
14	VREF14	IO	-	FlexDiff_TX84p	AE13
14	VREF14	IO	-	FlexDiff_TX85p	AE12
14	VREF14	IO	-	FlexDiff_TX86n	AF11
14	VREF14	IO	VREF14 (5)	FlexDiff_TX86p	AE11
14	VREF14	IO	-	FlexDiff_TX87n	AD12
14	VREF14	IO	-	FlexDiff_TX87p	AD11
14	VREF14	IO	-	FlexDiff_TX88n	AF10
14	VREF14	IO	-	FlexDiff_TX88p	AE10
14	VREF14	IO	-	FlexDiff_TX89p	AE9
14	VREF14	IO	-	FlexDiff_TX90n	AE8
14	VREF14	IO	-	FlexDiff_TX90p	AD8
14	VREF14	IO	-	FlexDiff_TX91p	AE7
14	VREF14	IO	-	FlexDiff_RX85n	AG11
14	VREF14	IO	-	FlexDiff_RX87n	AG10
14	VREF14	IO	-	FlexDiff_TX85n	AF12
14	VREF14	IO	-	FlexDiff_TX89n	AF9
14	VREF14	IO	-	FlexDiff_TX91n	AF7
15	VREF15	IO	-	FlexDiff_RX73n	AD21
15	VREF15	IO	-	FlexDiff_RX73p	AD22

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
15	VREF15	IO	-	FlexDiff_RX74n	AG20
15	VREF15	IO	-	FlexDiff_RX74p	AH20
15	VREF15	IO	-	FlexDiff_RX75n	AC19
15	VREF15	IO	-	FlexDiff_RX75p	AD19
15	VREF15	IO	-	FlexDiff_RX76n	AG19
15	VREF15	IO	-	FlexDiff_RX76p	AH19
15	VREF15	IO	-	FlexDiff_RX77n	AG18
15	VREF15	IO	-	FlexDiff_RX77p	AH18
15	VREF15	IO	-	FlexDiff_RX78n	AC17
15	VREF15	IO	-	FlexDiff_RX78p	AD17
15	VREF15	IO	-	FlexDiff_RX79n	AG17
15	VREF15	IO	-	FlexDiff_RX79p	AH17
15	VREF15	IO	-	FlexDiff_RX80n	AG16
15	VREF15	IO	-	FlexDiff_RX80p	AH16
15	VREF15	IO	-	FlexDiff_RX81n	AD15
15	VREF15	IO	FAST_ROW5 (6)	FlexDiff_RX81p	AC15
15	VREF15	IO	-	FlexDiff_TX74n	AE21
15	VREF15	IO	-	FlexDiff_TX74p	AD20
15	VREF15	IO	-	FlexDiff_TX75n	AF20
15	VREF15	IO	-	FlexDiff_TX75p	AE20
15	VREF15	IO	-	FlexDiff_TX76n	AD18
15	VREF15	IO	-	FlexDiff_TX76p	AC18
15	VREF15	IO	-	FlexDiff_TX77n	AF19
15	VREF15	IO	-	FlexDiff_TX77p	AE19
15	VREF15	IO	-	FlexDiff_TX78n	AF18
15	VREF15	IO	VREF15 (5)	FlexDiff_TX78p	AE18
15	VREF15	IO	-	FlexDiff_TX79n	AD16
15	VREF15	IO	-	FlexDiff_TX79p	AC16
15	VREF15	IO	-	FlexDiff_TX80n	AF17
15	VREF15	IO	-	FlexDiff_TX80p	AE17
15	VREF15	IO	-	FlexDiff_TX81n	AF16
15	VREF15	IO	-	FlexDiff_TX81p	AE16
15	VREF15	IO	-	FlexDiff_TX82n	AF15
15	VREF15	IO	-	FlexDiff_TX82p	AE15
16	VREF16	IO	-	FlexDiff_RX64n	AD28
16	VREF16	IO	-	FlexDiff_RX64p	AD27
16	VREF16	IO	-	FlexDiff_RX65n	AE28
16	VREF16	IO	-	FlexDiff_RX65p	AE27
16	VREF16	IO	-	FlexDiff_RX66n	AD25
16	VREF16	IO	-	FlexDiff_RX66p	AD26
16	VREF16	IO	-	FlexDiff_RX67n	AC24

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
16	VREF16	IO	-	FlexDiff_RX67p	AD24
16	VREF16	IO	-	FlexDiff_RX68n	AG26
16	VREF16	IO	-	FlexDiff_RX68p	AH26
16	VREF16	IO	-	FlexDiff_RX69n	AG25
16	VREF16	IO	-	FlexDiff_RX69p	AH25
16	VREF16	IO	-	FlexDiff_RX70n	AG24
16	VREF16	IO	-	FlexDiff_RX70p	AH24
16	VREF16	IO	-	FlexDiff_RX71n	AG23
16	VREF16	IO	-	FlexDiff_RX71p	AH23
16	VREF16	IO	-	FlexDiff_RX72n	AG22
16	VREF16	IO	-	FlexDiff_RX72p	AH22
16	VREF16	IO	-	FlexDiff_TX65n	AB27
16	VREF16	IO	LOCK2 (10)	FlexDiff_TX65p	AB28
16	VREF16	IO	-	FlexDiff_TX66n	AC27
16	VREF16	IO	-	FlexDiff_TX66p	AC28
16	VREF16	IO	-	FlexDiff_TX67n	AC26
16	VREF16	IO	-	FlexDiff_TX67p	AC25
16	VREF16	IO	-	FlexDiff_TX68n	AD23
16	VREF16	IO	VREF16 (5)	FlexDiff_TX68p	AC23
16	VREF16	IO	-	FlexDiff_TX69n	AF26
16	VREF16	IO	-	FlexDiff_TX69p	AE26
16	VREF16	IO	-	FlexDiff_TX70n	AF25
16	VREF16	IO	-	FlexDiff_TX70p	AE25
16	VREF16	IO	-	FlexDiff_TX71n	AF24
16	VREF16	IO	-	FlexDiff_TX71p	AE24
16	VREF16	IO	-	FlexDiff_TX72n	AF23
16	VREF16	IO	-	FlexDiff_TX72p	AE23
16	VREF16	IO	-	FlexDiff_TX73n	AF22
16	VREF16	IO	-	FlexDiff_TX73p	AE22
17	-	CLKLK_ENA (11), (16)	-	-	C15
17	-	CONF_DONE (11)	-	-	C16
17	-	DATA0 (11), (12)	-	-	E13
17	-	DCLK (11)	-	-	C14
17	-	MSEL0 (11)	-	-	C13
17	-	MSEL1 (11)	-	-	D15
17	-	nCE (11)	-	-	E17
17	-	nCEO (11)	-	-	D8
17	-	nCONFIG (11)	-	-	D13
17	-	nSTATUS (11)	-	-	E15
17	-	PLLRDY (11), (13)	-	-	D16
17	-	VCCSEL (14)	-	-	E11

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
18	-	TCK (11)	-	-	AC13
18	-	TDI (11)	-	-	AC11
18	-	TDO (11)	-	-	AC10
18	-	TMS (11)	-	-	AC12
18	-	TRST (11)	-	-	AD13
19	-	CLKLK_OUT1n (11)	-	-	J24
19	-	CLKLK_OUT1p (11), (17)	-	-	J23
19	-	VCC_CKOUT1	-	-	J21
20	-	CLKLK_OUT2n (11)	-	-	Y22
20	-	CLKLK_OUT2p (11), (17)	-	-	Y21
20	-	VCC_CKOUT2	-	-	AA22
21	-	CLKLK_OUT3n (11)	-	-	Y8
21	-	CLKLK_OUT3p (11), (17)	-	-	Y7
21	-	VCC_CKOUT3	-	-	AA7
22	-	CLKLK_OUT4n (11)	-	-	J6
22	-	CLKLK_OUT4p (11), (17)	-	-	J5
22	-	VCC_CKOUT4	-	-	J8
-	-	VCCA_CKLK1	-	-	F20
-	-	VCCA_CKLK1	-	-	F22
-	-	VCCA_CKLK2	-	-	AC20
-	-	VCCA_CKLK2	-	-	AC22
-	-	VCCA_CKLK3	-	-	AC7
-	-	VCCA_CKLK3	-	-	AC9
-	-	VCCA_CKLK4	-	-	F7
-	-	VCCA_CKLK4	-	-	F9
-	-	VCCA_HSDI1	-	-	G15
-	-	VCCA_HSDI2	-	-	G14
-	-	VCCD_CKLK1	-	-	F21
-	-	VCCD_CKLK2	-	-	AC21
-	-	VCCD_CKLK3	-	-	AC8
-	-	VCCD_CKLK4	-	-	F8
-	-	VCCD_HSDI1	-	-	H17
-	-	VCCD_HSDI2	-	-	H13
-	-	VCCD_RXTX	-	-	G9
-	-	VCCD_RXTX	-	-	G10
-	-	VCCD_RXTX	-	-	G11
-	-	VCCD_RXTX	-	-	G12
-	-	VCCD_RXTX	-	-	G13
-	-	VCCD_RXTX	-	-	G16
-	-	VCCD_RXTX	-	-	G17
-	-	VCCD_RXTX	-	-	G18

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
-	-	VCCD_RXTX	-	-	G19
-	-	VCCD_RXTX	-	-	G20
-	-	VCCD_RXTX	-	-	F10
-	-	VCCD_RXTX	-	-	F11
-	-	VCCD_RXTX	-	-	F12
-	-	VCCD_RXTX	-	-	F13
-	-	VCCD_RXTX	-	-	F14
-	-	VCCD_RXTX	-	-	F15
-	-	VCCD_RXTX	-	-	F16
-	-	VCCD_RXTX	-	-	F17
-	-	VCCD_RXTX	-	-	F18
-	-	VCCD_RXTX	-	-	F19
-	-	VCCINT	-	-	C1
-	-	VCCINT	-	-	AF1
-	-	VCCINT	-	-	H2
-	-	VCCINT	-	-	AA2
-	-	VCCINT	-	-	AF2
-	-	VCCINT	-	-	H3
-	-	VCCINT	-	-	P3
-	-	VCCINT	-	-	R3
-	-	VCCINT	-	-	AA3
-	-	VCCINT	-	-	C8
-	-	VCCINT	-	-	AF8
-	-	VCCINT	-	-	AG8
-	-	VCCINT	-	-	AF21
-	-	VCCINT	-	-	AG21
-	-	VCCINT	-	-	C21
-	-	VCCINT	-	-	H26
-	-	VCCINT	-	-	P26
-	-	VCCINT	-	-	R26
-	-	VCCINT	-	-	AA26
-	-	VCCINT	-	-	C27
-	-	VCCINT	-	-	H27
-	-	VCCINT	-	-	AA27
-	-	VCCINT	-	-	C28
-	-	VCCINT	-	-	AF27
-	-	VCCINT	-	-	AF28
-	-	VCCIO1	-	-	B8
-	-	VCCIO1	-	-	H10
-	-	VCCIO1	-	-	H11
-	-	VCCIO3	-	-	H18

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
-	-	VCCIO3	-	-	H19
-	-	VCCIO3	-	-	B21
-	-	VCCIO2	-	-	H9
-	-	VCCIO2	-	-	J9
-	-	VCCIO2	-	-	J10
-	-	VCCIO2	-	-	J11
-	-	VCCIO2	-	-	J14
-	-	VCCIO2	-	-	J15
-	-	VCCIO2	-	-	H22
-	-	VCCIO2	-	-	J18
-	-	VCCIO2	-	-	J19
-	-	VCCIO2	-	-	H20
-	-	VCCIO2	-	-	J20
-	-	VCCIO5	-	-	N9
-	-	VCCIO5	-	-	N11
-	-	VCCIO5	-	-	N12
-	-	VCCIO5	-	-	N13
-	-	VCCIO5	-	-	N14
-	-	VCCIO5	-	-	P14
-	-	VCCIO7	-	-	N15
-	-	VCCIO7	-	-	P15
-	-	VCCIO7	-	-	N16
-	-	VCCIO7	-	-	N17
-	-	VCCIO7	-	-	N18
-	-	VCCIO7	-	-	N20
-	-	VCCIO9	-	-	U7
-	-	VCCIO9	-	-	U8
-	-	VCCIO9	-	-	U9
-	-	VCCIO9	-	-	U10
-	-	VCCIO9	-	-	U11
-	-	VCCIO9	-	-	U12
-	-	VCCIO9	-	-	U13
-	-	VCCIO11	-	-	U16
-	-	VCCIO11	-	-	U17
-	-	VCCIO11	-	-	U18
-	-	VCCIO11	-	-	U19
-	-	VCCIO11	-	-	U20
-	-	VCCIO11	-	-	U21
-	-	VCCIO11	-	-	U22
-	-	VCCIO13	-	-	AA8
-	-	VCCIO13	-	-	AA9

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
-	-	VCCIO13	-	-	AA10
-	-	VCCIO13	-	-	AA11
-	-	VCCIO13	-	-	AA12
-	-	VCCIO13	-	-	AA13
-	-	VCCIO13	-	-	AA14
-	-	VCCIO15	-	-	AA15
-	-	VCCIO15	-	-	AA16
-	-	VCCIO15	-	-	AA17
-	-	VCCIO15	-	-	AA18
-	-	VCCIO15	-	-	AA19
-	-	VCCIO15	-	-	AA20
-	-	VCCIO15	-	-	AA21
-	-	VCCIO17	-	-	E14
-	-	VCCIO18	-	-	AB12
-	-	GND	-	-	G8
-	-	GND	-	-	G21
-	-	GND	-	-	G7
-	-	GND	-	-	H8
-	-	GND	-	-	H21
-	-	GND	-	-	G22
-	-	GND	-	-	H14
-	-	GND	-	-	H16
-	-	GND	-	-	J7
-	-	GND	-	-	J22
-	-	GND	-	-	AA6
-	-	GND	-	-	AA23
-	-	GND	-	-	AB7
-	-	GND	-	-	AB8
-	-	GND	-	-	AB21
-	-	GND	-	-	AB22
-	-	GND	-	-	AB9
-	-	GND	-	-	AB20
-	-	GND	-	-	H15
-	-	GND	-	-	H28
-	-	GND	-	-	H1
-	-	GND	-	-	P1
-	-	GND	-	-	R1
-	-	GND	-	-	AA1
-	-	GND	-	-	AG1
-	-	GND	-	-	A2
-	-	GND	-	-	B2

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
-	-	GND	-	-	P2
-	-	GND	-	-	R2
-	-	GND	-	-	AG2
-	-	GND	-	-	AH2
-	-	GND	-	-	E5
-	-	GND	-	-	F5
-	-	GND	-	-	G5
-	-	GND	-	-	M5
-	-	GND	-	-	E6
-	-	GND	-	-	F6
-	-	GND	-	-	G6
-	-	GND	-	-	H6
-	-	GND	-	-	M6
-	-	GND	-	-	AB6
-	-	GND	-	-	E7
-	-	GND	-	-	H7
-	-	GND	-	-	M7
-	-	GND	-	-	V7
-	-	GND	-	-	A8
-	-	GND	-	-	E8
-	-	GND	-	-	M8
-	-	GND	-	-	V8
-	-	GND	-	-	AH8
-	-	GND	-	-	M9
-	-	GND	-	-	V9
-	-	GND	-	-	H4
-	-	GND	-	-	V10
-	-	GND	-	-	E12
-	-	GND	-	-	M11
-	-	GND	-	-	V11
-	-	GND	-	-	H25
-	-	GND	-	-	H12
-	-	GND	-	-	M12
-	-	GND	-	-	C2
-	-	GND	-	-	J13
-	-	GND	-	-	M13
-	-	GND	-	-	AB13
-	-	GND	-	-	A14
-	-	GND	-	-	B14
-	-	GND	-	-	M14
-	-	GND	-	-	AB14

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
-	-	GND	-	-	AG14
-	-	GND	-	-	AH14
-	-	GND	-	-	A15
-	-	GND	-	-	B15
-	-	GND	-	-	B28
-	-	GND	-	-	M15
-	-	GND	-	-	AB15
-	-	GND	-	-	AG15
-	-	GND	-	-	AH15
-	-	GND	-	-	B1
-	-	GND	-	-	J16
-	-	GND	-	-	M16
-	-	GND	-	-	AB16
-	-	GND	-	-	M17
-	-	GND	-	-	AB17
-	-	GND	-	-	E18
-	-	GND	-	-	M18
-	-	GND	-	-	V18
-	-	GND	-	-	M19
-	-	GND	-	-	V19
-	-	GND	-	-	M20
-	-	GND	-	-	V20
-	-	GND	-	-	AH21
-	-	GND	-	-	A21
-	-	GND	-	-	E21
-	-	GND	-	-	M21
-	-	GND	-	-	V21
-	-	GND	-	-	E22
-	-	GND	-	-	D21
-	-	GND	-	-	M22
-	-	GND	-	-	V22
-	-	GND	-	-	E23
-	-	GND	-	-	F23
-	-	GND	-	-	G23
-	-	GND	-	-	H23
-	-	GND	-	-	M23
-	-	GND	-	-	AB23
-	-	GND	-	-	AB24
-	-	GND	-	-	E24
-	-	GND	-	-	F24
-	-	GND	-	-	G24

Table 2. EP1M350 Device Pin-Outs					
IO Bank	**VREF Pin Reference** (1), (2)	**Pin Name/Function** (3)	**Dual Purpose Function** (20)	**Flexible-LVDS Function** (4)	**780-Pin FineLine BGA**
-	-	GND	-	-	H24
-	-	GND	-	-	M24
-	-	GND	-	-	V17
-	-	GND	-	-	A27
-	-	GND	-	-	B27
-	-	GND	-	-	P27
-	-	GND	-	-	R27
-	-	GND	-	-	AG27
-	-	GND	-	-	AH27
-	-	GND	-	-	V16
-	-	GND	-	-	P28
-	-	GND	-	-	R28
-	-	GND	-	-	AA28
-	-	GND	-	-	AG28
-	-	GND	-	-	J12
-	-	GND	-	-	J17
-	-	GND	-	-	E16
		GND			D14
Total User I/Os (19), (20)					486

Notes:

(1) For EP1M350 devices, each I/O bank (1 through 16) supports its own VREF setting for input standards. However, some of the banks must be set to the same V_{CCIO} level. The bank pairs that must match are 2 and 4, 5 and 6, 7 and 8, 9 and 10, 11 and 12, 13 and 14, 15 and 16. Therefore, only one set of VCCIO pins is shown for each of the pairs (see bank diagram).

(2) The HSDI receive banks are banks 1 and 3. When used as regular I/O, banks 1 and 3 can have one VREF each and can be set to different V_{CCIO} Levels. HSDI transmit banks are banks 2 an 4. When used as regular I/O, banks 2 and 4 can have unique VREF settings, but must have the same VCCIO level.

(3) This column tells whether a pin is a regular I/O or is a dedicated pin function.

(4) Flexible-LVDS™ circuitry is the lower speed x1 LVDS that does not use HSDI circuitry. Some I/O pins have built-in dual-purpose LVDS buffers shown in the Flexible-LVDS Column. All buffers shown connect to pins; there are 99 LVDS inputs and 100 LVDS outputs.

(5) This pin is the voltage reference pin for the left or right side VREF bus of an I/O bank only if the bank is used for a voltage referenced I/O standard (SSTL2, SSTL3, GTL+, HSTL). If no voltage referenced standard is used, this pin is a user I/O pin.

(6) Dual-purpose pins for driving the row global signals within an I/O bank's, or a row's associated logic array block (LAB) row. These pins are regular I/O pins if not used to drive row global signals.

(7) This pin can be used as a regular I/O after configuration.

(8) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(9) Dual-purpose pins for driving the dedicated global fast lines within the entire device. These are regular I/O pins if not used to drive fast global signals.

(10) This pin shows the status of general-purpose phase-locked loops (GPLLs). When general-purpose PLLs are locked to the incoming clock , `LOCK` is driven high. `LOCK` remains high if a periodic clock remains clocking. The `LOCK` function is optional. If the `LOCK` output is not used, this pin is a user I/O pin.

(11) This pin is a dedicated pin; it is not available as a user I/O pin.

(12) This pin is tri-stated in user mode.

(13) Dedicated output that shows the `LOCK` status of all PLLs. This signal is the `AND` gate of all PLL `LOCK` signals (for all enabled HSDI PLLs and GPLLs) and `CONF_DONE`. This pin should be unconnected if its function is not used.

(14) Dedicated input that is used to choose whether programming input pins (dedicated configuration and JTAG pins) can accept 3.3 V, 2.5 V, or 1.8 V during configuration. A "1" denotes 3.3 V or 2.5 V; a "0" denotes 1.8 V. This pin's input voltage is determined by `VCCIO17`. If `VCCIO17` is 3.3 V, a logic high is determined by a 3.3-V LVTTL V_{IH} minimum. If `VCCIO17` is 2.5 V, a logic high is determined by a 2.5-V LVTTL V_{IH} minimum. If `VCCIO17` is 1.8 V, a logic high is deternined by a 1.8-V LVTTL V_{IH} minimum.

(15) This note number is not used.

(16) Dedicated input pin that is the active-high enable pin for all of the GPLL circuits in the device. When de-asserted, all GPLLs are reset to their default unlocked state and will stop clocking. Once re-asserted,

the PLLs will lock again and start clocking. This PLL enable control can be selected on a per GPLL basis. If this pin feature is not used, it should be connected to GND on the board.

(17) Dedicated external clock output from the General Purpose PLLs. CLKLK_OUT1p is from GPLL1, is from GPLL2, CLKLK_OUT3p is from GPLL3, and CLKLK_OUT4p is from GPLL4. Each dedicated clock outputhas its own V_{CCIO} power for output-standard selection. If this pin feature is not used, it should be connected to GND on the board.

(18) Dedicated external clock feedback from the general-purpose PLLs. CLKLK_FB1p feeds GPLL1, CLKLK_FB2p feeds GPLL2, CLKLK_FB3p feeds GPLL3, and CLKLK_FB4p feeds GPLL4. The external clock feedback must use the same I/O standard as the external clock output and the global clock input to the GPLL. If this pin feature is not used, it should be connected to GND on the board.

(19) The user I/O pin count includes dedicated clock inputs and HSDI pins.

(20) If HSDI is used (source synchronous or clock-data recovery), then any unused regular I/Os in banks 1, 3, and 4 cannot be used. The unused pins should be connected to GND on the board to help noise immunity.

(21) When used for regular I/O pins, the receiver balls HSDI_RX1p/n through HSDI_RX18p/n, support a subset of the I/O standards and drive strengths. Table 2 shows the I/O standards and drive strengths that are supported for HSDI_RX1p/n through HSDI_RX18p/n when used as regular I/O pins. All other regular I/O pins include support for all standards and drive strengths shown in the data sheet.

Table 3 shows the output pin placement guideline with respect to VREF pins. Output pins should be placed two balls away from a VREF pin that is used within a bank. Table 3 shows which pins cannot be used as outputs because they are neighbors to the specified VREF pin. These pins can still be used as inputs. If a VREF pin is being used as a regular I/O, this output pin placement guideline does not apply

Table 3. Output Pin-to-VREF Pin Placement Guidelines

VREF Pin	Adjacent Pins That Cannot Be Outputs
VREF1	—
VREF2	L16
VREF3	A16
	B16
VREF4	—
VREF5	C3
	C4
	C5
	C12
	D11
VREF6	N3
	T3
	T4
VREF7	N21
	N25
	N26
	N27
	T28
VREF8	C23
	C24
	C25
	D22
	D24
VREF9	U3
	V3
	V4
	W4
	Y4
VREF10	P12
	R11
	W12
	Y14
VREF11	R19
	T19
	T20
	W19
	W20
VREF12	N22
	P22
	P23
	R22
	T24
VREF13	AC5
	AC6
	AD5
	AF3
	AG3

Table 3. Output Pin-to-VREF Pin Placement Guidelines	
VREF Pin	**Adjacent Pins That Cannot Be Outputs**
VREF14	AF11
	AF12
	AG11
	AG12
	AH11
VREF15	AF18
	AF19
	AG18
	AG19
	AH18
VREF16	AC24
	AC26
	AD23
	AD24
	AD25

Table 4 provides descriptions for all power, HSDI, and general-purpose phase-locked loop (PLL) related pins.

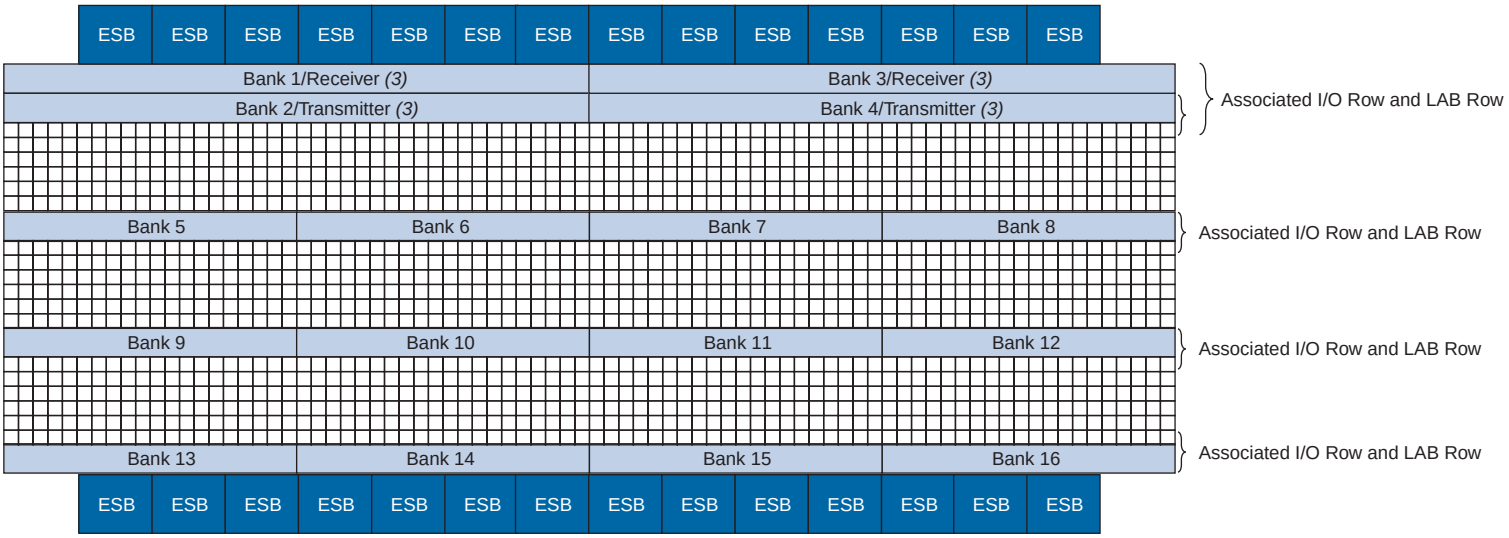
Table 4. Power, HSDI & General-Purpose PLL Pins	
Pin Name	**Pin Description**
HSDI_CLK1p	Dedicated input pin that drives HSDI PLL1 for high-speed differential interface.
HSDI_CLK1n	Dedicated negative terminal input for differential clock into HSDI PLL1.
HSDI_CLK2p	Dedicated input pin that drives HSDI PLL2 for high-speed differential interface.
HSDI_CLK2n	Dedicated negative terminal input for differential clock into HSDI PLL2.
HSDI_TXCLKOUT1p	Dedicated output pin for source synchronous transmission from HSDI.
HSDI_TXCLKOUT1n	Dedicated negative terminal output for differential source synchronous clock from HSDI.
HSDI_RX[1..18]p/n	Dual-purpose pins for HSDI reciever channels 1 through 8. "p" is positive terminal, "n" is negative terminal. These pins can only be used as regular I/O pins if HSDI circuitry is not used.
HSDI_TX[1..18]p/n	Dual-purpose pins for HSDI transmitter channels 1 through 8. "p" is positive terminal, "n" is negative terminal. These pins can only be used as regular I/O pins if HSDI circuitry is not used.
VREF[1..12]	VREF pins for each I/O bank; VREF1 is the reference voltage pin for BANK1, VREF2 for BANK2, VREF3 for BANK3. These pins are regular I/O pins if the I/O Bank is not using a VREF I/O standard.
FAST_ROW[1..6]	Dual-purpose pins for driving the row global signals within an I/O bank are associated with a LAB row. These pins are regular I/O pins if not used to drive row globals.
FAST[1..6]	Dual-purpose pins for driving the dedicated global fast lines within the entire device. These pins are regular I/O pins if not used to drive fast global signals.
CLK1p	Dedicated global clock input. Also, the clock input to the general-purpose PLL 1.
CLK1n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLK1VREF) for the CLK1p input.
CLK2p	Dedicated global clock input. Also, the clock input to general-purpose PLL 2.
CLK2n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLK2VREF) for the CLK2p input.
CLK3p	Dedicated global clock input.
CLK3n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLK3VREF) for the CLK3p input.
CLK4p	Dedicated global clock input.
CLK4n	Dedicated negative terminal input for differential global clock input. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLK3VREF) for the CLK3p input.
CLKLK_OUT1p	Dedicated external output for general-purpose PLL 1.
CLKLK_OUT1n	Dedicated negative terminal output for differential output from general-purpose PLL 1.
CLKLK_OUT2p	Dedicated external output for general-purpose PLL 2.
CLKLK_OUT2n	Dedicated negative terminal output for differential output from general-purpose PLL 2.
CLKLK_OUT3p	Dedicated external output for general-purpose PLL 3.
CLKLK_OUT3n	Dedicated negative terminal output for differential output from general-purpose PLL 3.
CLKLK_OUT4p	Dedicated external output for general-purpose PLL 4.

Table 4. Power, HSDI & General-Purpose PLL Pins	
Pin Name	**Pin Description**
CLKLK_OUT4n	Dedicated negative terminal output for differential output from general-purpose PLL 4.
CLKLK_FBIN1p	Dedicated clock input for the external feedback to general-purpose PLL 1.
CLKLK_FBIN1n	Dedicated negative terminal input for differential external feedback from general-purpose PLL 1. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLKLK_FBIN1VREF) for the clock feedback input.
CLKLK_FBIN2p	Dedicated clock input for the external feedback to general-purpose PLL 2.
CLKLK_FBIN2n	Dedicated negative terminal input for differential external feedback from general-purpose PLL 2. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLKLK_FBIN2VREF) for the clock feedback input
CLKLK_FBIN3p	Dedicated clock input for the external feedback to GPLL 3
CLKLK_FBIN3n	Dedicated negative terminal input for differential external feedback from GPLL3. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLKLK_FBIN3VREF) for the clock feedback input.
CLKLK_FBIN4p	Dedicated clock input for the external feedback to general-purpose PLL 4.
CLKLK_FBIN4n	Dedicated negative terminal input for differential external feedback from general-purpose PLL 4. If the clock is a voltage referenced standard such as SSTL2, then this pin is the VREF input (CLKLK_FBIN4VREF) for the clock feedback input
PLLRDY	Dedicated output that shows the lock status of all PLLs. This signal is the AND gate of all PLL Lock signals (HSDI PLL and general-purpose PLL) and CONF_DONE. If used, this pin should be left unconnected.
VCCSEL	Dedicated input that is used to choose whether programming input pins (dedicated configuration and JTAG pins) can accept 3.3 V, 2.5 V, or 1.8 V during configuration. A "1" means 3.3 V or 2.5 V, and a "0" means 1.8 V (see note 14).
VCCINT	Internal core voltage. This must be 1.8 V.
VCCIO[1..22]	I/O and configuration pin voltage. For I/O banks these can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V. For configuration and JTAG banks, these can be 3.3 V, 2.5 V or 1.8 V.
VCCD_RXTX	Digital power for HSDI receiver and transmitter circuitry. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCA_HSDI1	Analog power for HSDI PLL 1. These must be connected to 1.8 V. HSDI 1 and 2 analog power should be isolated with its own partition in the VCCINT plane.
VCCD_HSDI1	Digital power for HSDI PLL 1. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCA_HSDI2	Analog power for HSDI PLL 2. These must be connected to 1.8 V. HSDI 1 and 2 analog power should be isolated with its own partition in the VCCINT plane.
VCCD_HSDI2	Digital power for HSDI PLL 2. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCA_CKLK1	Analog power for general-purpose PLL 1. These must be connected to 1.8 V. General-purpose PLL 1, 2, 3, and 4 analog power should be isolated with its own partition in the VCCINT plane.
VCCD_CKLK1	Digital power for general-purpose PLL 1. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCA_CKLK2	Analog power for general-purpose PLL 2. These must be connected to 1.8 V. General-purpose PLL 1, 2, 3, and 4 analog power should be isolated with its own partition in the VCCINT plane.

Table 4. Power, HSDI & General-Purpose PLL Pins	
Pin Name	**Pin Description**
VCCD_CKLK2	Digital power for general-purpose PLL 2. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCA_CKLK3	Analog power for general-purpose PLL 3. These must be connected to 1.8 V. General-purpose PLL 1, 2, 3, and 4 analog power should be isolated with its own partition in the VCCINT plane.
VCCD_CKLK3	Digital power for general-purpose PLL 3. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCCA_CKLK4	Analog power for general-purpose PLL 4. These must be connected to 1.8 V. General-purpose PLL 1, 2, 3, and 4 analog power should be isolated with its own partition in the VCCINT plane.
VCCD_CKLK4	Digital power for general-purpose PLL 4. These must be connected to 1.8 V. These pins can be connected to the VCCINT plane on the board.
VCC_CKOUT1	External clock output buffer power for CLKLK_OUT1p/n of general-purpose PLL 1. This voltage can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
VCC_CKOUT2	External clock output buffer power for CLKLK_OUT2p/n of general-purpose PLL 2. This voltage can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
VCC_CKOUT3	External clock output buffer power for CLKLK_OUT3p/n of general-purpose PLL 3. This voltage can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
VCC_CKOUT4	External clock output buffer power for CLKLK_OUT4p/n of GPLL4. This voltage can be 3.3 V, 2.5 V, 1.8 V, or 1.5 V.

Figure 1 shows the I/O and HSDI bank block diagram for the EP1M350 device.

Figure 1. I/O & HSDI Banks *Notes (1), (2)*



Notes:
(1) The following banks are not shown: Bank 17 (contains dedicated configuration and control pins), Bank 18 (contains dedicated JTAG pins: `TCK`, `TDI`, `TDO`, `TMS`, and `TRST`), Bank 19 (contains `CLKLK_OUT1p/n` and its output power), Bank 20 (contains `CLKLK_OUT2p/n` and its output power), Bank 21 (contains `CLKLK_OUT3p/n` and its output power), and Bank 22 (contains `CLK_OUT4p/n` and its output power).
(2) Banks 1 and 3 can have their own V_{CCIO} and VREF setting. Banks 2, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16 must have the same V_{CCIO} power, but can have unique VREF settings. Banks 5 through 16 must have the same V_{CCIO} power, but can have unique VREF settings.
(3) The top I/O banks 1, 2, 3, and 4 only support non-HSDI I/O pins when the HSDI circuitry is unused. If any HSDI channel is used, banks 1, 2, 3, and 4 do not support regular I/O pins.

Copyright © 1995, 1996, 1997, 1998, 1999 Altera Corporation, 101 Innovation Drive, San Jose, CA 95134, USA, all rights reserved.

By accessing this information, you agree to be bound by the terms of Altera's Legal Notice.