Pin Name (1)	**144-Pin TQFP**	**208-Pin PQFP**	**256-Pin FineLine BGA**
MSEL0 (2)	77	108	P1
MSEL1 (2)	76	107	R1
nSTATUS (2)	35	52	T16
nCONFIG (2)	74	105	N4
DCLK (2)	107	155	B2
CONF_DONE (2)	2	2	C15
INIT_DONE (3)	14	19	G16
nCE (2)	106	154	B1
nCEO (2)	3	3	B16
nWS (4)	142	206	B14
nRS (4)	141	204	C14
nCS (4)	144	208	A16
CS (4)	143	207	A15
RDYnBUSY (4)	11	16	G14
CLKUSR (4)	7	10	D15
DATA7 (4)	116	166	B5
DATA6 (4)	114	164	D4
DATA5 (4)	113	162	A4
DATA4 (4)	112	161	B4
DATA3 (4)	111	159	C3
DATA2 (4)	110	158	A2
DATA1 (4)	109	157	B3
DATA0 (2), (5)	108	156	A1
TDI (2)	105	153	C2
TDO (2)	4	4	C16
TCK (2)	1	1	B15
TMS (2)	34	50	P15
TRST (2)	(6)	51	R16
Dedicated Inputs	54, 56, 124, 126	78, 80, 182, 184	B9, E8, M9, R8
Dedicated Clock Pins	55, 125	79, 183	A9, L8
GCLK1 (7)	55	79	L8
LOCK (8)	42	62	P12
DEV_CLRn (3)	122	180	D8
DEV_OE (3)	128	186	C9
VCCINT (2.5 V)	16, 50, 75, 85, 103, 127	21, 33, 48, 72, 91, 106, 124, 130, 152, 185, 201	E11, F5, F7, F9, F12, H6, H7, H10, J7, J10, J11, K9, L5, L7, L12, M11, R2
VCCIO (2.5 or 3.3 V)	5, 24, 45, 61, 71, 94, 115, 134	5, 22, 34, 42, 66, 84, 98, 110, 118, 138, 146, 165, 178, 194	D12, E6, F8, F10, G6, G8, G11, H11, J6, K6, K8, K11, L10, M6, N12
VCC_CKLK (9)	53	77	L9
GNDINT	6, 15, 25, 40, 52, 58, 66, 84, 93, 104, 123, 129, 139	6, 20, 23, 32, 35, 43, 49, 59, 76, 82, 109. 117, 123, 129, 137, 145, 151, 171, 181, 188	A3, A14, C7, E5, E12, F6, F11, G7, G9, G10, H8, H9, J8, J9, K5, K7, K10, L1, L6, L11, M5, M12
GND_CKLK (9)	57	81	T8
No Connect (N.C.)	–	–	D1, E3, E16, G3, H1, H16, J1, K3, K14, K16, L2, L4, M14, M16, N15
Total User I/O Pins (10)	102	147	171

Notes:

(1) All pins that are not listed are user I/O pins.

(2) This pin is a dedicated pin; it is not available as a user I/O pin.

(3) This pin can be used as a user I/O pin if it is not used for its device-wide or configuration function.

(4) This pin can be used as a user I/O pin after configuration.

(5) This pin is tri-stated in user mode.

(6) The optional JTAG pin TRST is not used in the 144-pin TQFP package.

(7) This pin drives the ClockLock and ClockBoost circuitry.

(8) This pin shows the status of the ClockLock and ClockBoost circuitry. When the ClockLock and ClockBoost circuitry is locked to the incoming clock and generates an internal clock, LOCK is driven high. LOCK goes low if a periodic clock stops clocking. The LOCK pin is optional; if the LOCK output is not used, this pin is a user I/O pin.

(9) This pin is the power or ground for the ClockLock and ClockBoost circuitry of a PLL. To ensure noise resistance, the power and ground supply to the ClockLock and ClockBoost circuitry should be isolated from the power and ground to the rest of the device. If the PLL is not used, this power or ground pin should bew connected to VCCINT or GNDINT, respectively.

(10) The user I/O pin count includes dedicated inputs, dedicated clock inputs, and all I/O pins.