Cyclone® III Device Family Pin Connection Guidelines
PCG-01003-1.0

The pin connection guidelines are considered preliminary. These pin connection guidelines should only be used as a recommendation, not as a specification.
The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

PLEASE REVIEW THE FOLLOWING TERMS AND CONDITIONS CAREFULLY BEFORE USING THE PIN CONNECTION GUIDELINES("GUIDELINES") PROVIDED TO YOU. BY USING THESE GUIDELINES, YOU INDICATE YOUR ACCEPTANCE OF SUCH TERMS AND CONDITIONS, WHICH CONSTITUTE THE LICENSE AGREEMENT ("AGREEMENT") BETWEEN YOU AND ALTERA CORPORATION ("ALTERA"). IF YOU DO NOT AGREE WITH ANY OF THESE TERMS AND CONDITIONS, DO NOT DOWNLOAD, COPY, INSTALL, OR USE OF THESE GUIDELINES.

1. Subject to the terms and conditions of this Agreement, Altera grants to you the use of this pin connection guideline to determine the pin connections of an Altera® programmable logic device-based design. You may not use this pin connection guideline for any other purpose.

2. Altera does not guarantee or imply the reliability, or serviceability, of the pin connection guidelines or other items provided as part of these guidelines. The files contained herein are provided 'AS IS'. ALTERA DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

3. In no event shall the aggregate liability of Altera relating to this Agreement or the subject matter hereof under any legal theory (whether in tort, contract, or otherwise), exceed One US Dollar (US$1.00). In no event shall Altera be liable for any lost revenue, lost profits, or other consequential, indirect, or special damages caused by your use of these guidelines even if advised of the possibility of such damages.

4. This Agreement shall be governed by the laws of the State of California, without regard to conflict of law or choice of law principles. You agree to submit to the exclusive jurisdiction of the courts in the County of Santa Clara, State of California for the resolution of any dispute or claim arising out of or relating to this Agreement. The parties hereby agree that the party who is not the substantially prevailing party with respect to a dispute, claim, or controversy relating to this Agreement shall pay the costs actually incurred by the substantially prevailing party in relation to such dispute, claim, or controversy, including attorneys' fees.

BY DOWNLOADING OR USING THESE GUIDELINES, YOU ACKNOWLEDGE THAT YOU HAVE READ THIS AGREEMENT, UNDERSTAND IT, AND AGREE TO BE BOUND BY ITS TERMS AND CONDITIONS. YOU AND ALTERA FURTHER AGREE THAT IT IS THE COMPLETE AND EXCLUSIVE STATEMENT OF THE AGREEMENT BETWEEN YOU AND ALTERA, WHICH SUPERSEDES ANY PROPOSAL OR PRIOR AGREEMENT, ORAL OR WRITTEN, AND ANY OTHER COMMUNICATIONS BETWEEN YOU AND ALTERA RELATING TO THE SUBJECT MATTER OF THIS AGREEMENT.

Cyclone® III Device Family Pin Connection Guidelines
PCG-01003-1.0 *(Note 1)*

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
		Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins.	All VCCINT pins must be connected to 1.2V supply. Decoupling depends on the design decoupling requirements of the specific board. See Note (8)
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards. VCCIO powers up the JTAG pins (TCK, TMS, TDI and TDO) and the following configuration pins: nCONFIG, DCLK, DATA[15..0], nCE, nCEO, nWE, nRESET, nOE, FLASH_nCE, nCSO and CLKUSR.	Decoupling depends on the design decoupling requirements of the specific board. See Note (8)
VREFB[1..8]N[0..2] (Note 2)	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins. All of the VREF pins within a bank are shorted together.	If VREF pins are not used, the designer should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note (8)
VCCA[1..4] (Note 3)	Power	Supply (analog) voltage for PLLs[1..4] and other analog circuits in the device.	The designer must connect these pins to 2.5V, even if the PLL is not used. These pins must be powered up and powered down at the same time. Connect VCCA[1..4] pins together. VCCA supply to the chip should be isolated. See Note(9) for details. See Note(10) for recommended decoupling.
VCCD_PLL[1..4] (Note 3)	Power	Supply (digital) voltage for PLLs[1..4].	The designer must connect these pins to 1.2V, even if the PLL is not used. Connect VCCD_PLL[1..4] pins together. VCCD_PLL supply to the chip should be isolated. See Note(9) for details. See Note (11) for recommended decoupling.
RUP[1..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5 and 7. The external precision resistor Rup must be connected to the designated RUP pin within the same bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O, it is recommended that the pin be connected to VCCIO of the bank in which the RUP pin resides.
RDN[1..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 2, 4, 5 and 7. The external precision resistor Rdn must be connected to the designated RDN pin within the same bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O, it is recommended that the pin be connected to GND.
GND	Ground	Device ground pins.	All GND pins should be connected to the board GND plane.

Cyclone® III Device Family Pin Connection Guidelines PCG-01003-1.0 *(Note 1)*			
Pin Name	**Pin Type (1st, 2nd, & 3rd Function)**	**Pin Description**	**Connection Guidelines**
GNDA[1..4] (Note 3)	Ground	Ground for PLLs[1..4] and other analog circuits in the device.	The designer should connect these pins to an isolated analog ground plane on the board.
NC	No Connect	No Connect	Do not connect these pins to any signal.
Dedicated Configuration/JTAG Pins			
DCLK	Input (PS,FPP) Output (AS,AP)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Cyclone III device. In AS and AP mode, DCLK is an output from the Cyclone III device that provides timing for the configuration interface.	DCLK should not be left floating. In JTAG configuration and schemes that use an external host, designer should drive it high or low, whichever is more convenient on the board. In AS and AP mode, the DCLK has an internal pull-up resistor (typically 25-kOhm) that is always active.
DATA[0]	Input (PS,FPP,AS) Bidirectional open drain (AP)	Dedicated configuration data input pin. In serial configuration modes, bit-wide configuration data is received through this pin. In AS mode, DATA[0] has an internal pull-up resistor that is always active. After AS configuration, DATA[0] is a dedicated input pin with optional user control. After PS or PP configuration, DATA[0] is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA[0] is a dedicated bidirectional pin with optional user control.	If you are using a serial configuration device in AS configuration mode, you must connect a 25-Ohm series resistor at the near end of the serial configuration device for the DATA[0]. If DATA[0] is not used, it should be driven high or low, whichever is more convenient on the board.
MSEL[3..0]	Input	Configuration input pins that set the Cyclone III device configuration scheme. Some of the smaller devices or package options do not support the AP flash programming and do not have the MSEL[3] pin.	These pins are internally connected to 5-kOhm resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used, these pins should be tied to VCCA or GND. Refer to Chapter 10 of Cyclone III Handbook: Configuring Cyclone III Devices. If only JTAG configuration is used, then connect these pins to GND.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE is tied low.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration. The input buffer on this pin supports hysteresis using Schmitt trigger circuitry.	If you are using PS configuration scheme with a download cable, connect this pin through a 10-kOhm resistor to VCCA. For other configuration schemes, if this pin is not used, this pin must be connected directly or through a 10-kOhm resistor to VCCIO.

Cyclone® III Device Family Pin Connection Guidelines
PCG-01003-1.0 *(Note 1)*

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode.	This pin is not available as a user I/O pin. CONF_DONE should be pulled high by an external 10-kΩ pull-up resistor.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization.	This pin is not available as a user I/O pin. nSTATUS should be pulled high by an external 10-kΩ pull-up resistor.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.	Connect this pin to a 1-kOhm resistor to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.	When interfacing with 2.5V/3.0V/3.3V configuration voltage standards, connect this pin through a 1-kOhm resistor to VCCA. Otherwise, connect this pin through a 1-kOhm resistor to VCCIO. See Note (4).
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.	When interfacing with 2.5V/3.0V/3.3V configuration voltage standards, connect this pin through a 1-kOhm resistor to VCCA. Otherwise, connect this pin through a 1-kOhm resistor to VCCIO. See Note (4).
TDO	Output	Dedicated JTAG output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected.
Clock and PLL Pins			
CLK[0,2,4,6,9,11,13,15], DIFFCLK_[0..7]p (Note 5)	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.	Connect unused pins to GND. See Note (12).
CLK[1,3,5,7,8,10,12,14], DIFFCLK_[0..7]n (Note 5)	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.	Connect unused pins to GND. See Note (12).
PLL[1..4]_CLKOUTp (Note 3)	I/O, Output	Optional positive terminal for external clock outputs from PLL [1..4]. These pins can only use the differential I/O standard if it is being fed by a PLL output.	Connect unused pins to GND. See Note (12).

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
PLL[1..4]_CLKOUTn (Note 3)	I/O, Output	Optional negative terminal for external clock outputs from PLL[1..4]. These pins can only use the differential I/O standard if it is being fed by a PLL output.	Connect unused pins to GND. See Note (12).
Optional/Dual-Purpose Configuration Pins			
nCEO	I/O, Output	Output that drives low when device configuration is complete.	During multi-device configuration, this pin feeds a subsequent device's nCE pin and must be pulled high to VCCIO by an external 10-kOhm pull-up resistor. During single device configuration and for the last device in multi-device configuration, this pin can be left floating or used as a user I/O after configuration.
FLASH_nCE, nCSO	I/O, Output	This pin functions as FLASH_nCE in AP mode, and nCSO in AS mode. This pin has an internal pull-up resistor that is always active. nCSO: Output control signal from the Cyclone III device to the serial configuration device in AS mode that enables the configuration device. FLASH_nCE: Output control signal from the Cyclone III device to the parallel flash in AP mode that enables the flash.	When not programming the device in AS mode, nCSO is not used. Similarly, FLASH_nCE is not used when not programming the device in AP mode. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
DATA[1], ASDO	Input (FPP) Output (AS) Bidirectional open-drain (AP)	This pin functions as DATA[1] in PS, FPP and AP modes, and as ASDO in AS mode. DATA[1]: Data input in non-AS mode. Byte-wide or word-wide configuration data is presented to the target device on DATA[7..0] or DATA[15..0] respectively. In PS configuration scheme, DATA[1] functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA[1] is available as a user I/O pin and the state of this pin depends on the Dual-Purpose Pin settings. After AP configuration, DATA[1] is a dedicated bidirectional pin with optional user control. ASDO: Control signal from the Cyclone III device to the serial configuration device in AS mode used to read out configuration data. In AS mode, this ASDO pin has an internal pull-up resistor that is always active. After AS configuration, this pin is a dedicated output pin with optional user control.	When not programming the device in AS or AP mode, this pin is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines
PADD[23..0]	Output	24-bit address bus from the Cyclone III device to the parallel flash in AP mode.	When not programming the device in AP mode, these pins are available as user I/O pins. If these pins are not used as I/Os, then it is recommended to leave these pins unconnected.
nRESET	Output	Active-low reset output. Driving the nRESET pin low resets the parallel flash.	When not programming the device in AP mode, nRESET is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
nAVD	Output	Active-low address valid output. Driving the nAVD pin low during read or write operation indicates to the parallel flash that valid address is present on the PADD[23..0] address bus.	When not programming the device in AP mode, nAVD is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
nOE	Output	Active-low output enable to the parallel flash. Driving the nOE pin low during read operation enables the parallel flash outputs (DATA[15..0] and RDY).	When not programming the device in AP mode, nOE is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
nWE	Output	Active-low write enable to the parallel flash. Driving the nWE pin low during write operation indicates to the parallel flash that data on the DATA[15..0] bus is valid.	When not programming the device in AP mode, nWE is not used and is available as a user I/O pin. If the pin is not used as an I/O then it is recommended to leave the pin unconnected.
RDY	Input	Control signal (WAIT) from the parallel flash is connected to this pin in the Cyclone III device to indicate when synchronous data is ready on the data bus.	The current implementation for AP configuration ignores the RDY pin. However it is highly recommended to connect this pin to the AP flash.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.	When the output for CRC_ERROR is not used and this pin is not used as an I/O then it is recommended to leave the pin unconnected.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional chip-wide reset pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. The DEV_CLRn pin does not affect JTAG boundary-scan or programming operations. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.	When the input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to VCCIO or GND.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.	When the input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to VCCIO or GND.

Cyclone® III Device Family Pin Connection Guidelines PCG-01003-1.0 *(Note 1)*			
Pin Name	**Pin Type (1st, 2nd, & 3rd Function)**	**Pin Description**	**Connection Guidelines**
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose status pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.	Connect this pin to a 10-kOhm resistor to VCCIO.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to GND.
Dual-Purpose Differential & External Memory Interface Pins			
DIFFIO_[L,R,T,B][0..61][n,p] (Note 6)	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).
DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],DPCLK[0..11] (Note 7)	I/O, DQS/CQ,DPCLK	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).

Cyclone® III Device Family Pin Connection Guidelines PCG-01003-1.0 *(Note 1)*			
Pin Name	**Pin Type (1st, 2nd, & 3rd Function)**	**Pin Description**	**Connection Guidelines**
DQS[0..5][L,R,T,B]/CQ[1,3,5][L,R,T,B][#],CDPCLK[0..7] (Note 7)	I/O, DQS/CQ,CDPCLK	Dual-purpose CDPCLK/DQS pins can connect to the global clock network for high fan-out control signals such as clocks, asynchronous clears, presets and clock enables. Only one of the two CDPCLK in each corner can feed the clock control block at a time. The other pin can be used as general-purpose I/O pin. The CDPCLK signals incur more delay to the clock block control because they are multiplexed before driving into the clock block control. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).
DQ[0..5][L,R,T,B] (Note 7)	I/O, DQ	Optional data signal for use in external memory interface.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).
DM[0..5][L,R,B,T][0..1]/BWS#[0..5][L,R,T,B]	I/O, DM/BWS#	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDRII SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.	When these I/O pins are not used they can be tied to the VCCIO of the bank they reside in or GND. See Note (12).

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device function

Notes:

(1) This pin connection guideline is created based on the largest Cyclone III device (EP3C120F780).

(2) EP3C5 and EP3C10 only have VREFB[1..8]N0.

(3) EP3C5 and EP3C10 only have PLL(1 & 2). EP3C16 and other larger densities have PLL (1,2,3 & 4).

(4) You must follow specific requirements when interfacing Cyclone III devices with 2.5V/3.0V/3.3V configuration voltage standards. All I/O inputs must maintain a maximum AC voltage of 4.1V. Refer to Configuration and JTAG Pin I/O Requirements of Chapter 10 in Cyclone III Handbook: Configuring Cyclone III Devices.

(5) The number of dedicated global clocks for each device density is different. EP3C5 and EP3C10 support four dedicated clock pins on the left and right sides of the device, that can drive a total of 10 global clock networks. EP3C16 and other larger densities support four dedicated clock pins on each side of the device that can drive a total of 20 global clock networks.

(6) The differential TX/RX channels for each device density and package is different. Please refer to the Cyclone III Handbook Chapter 8: High-Speed Differential Interfaces in Cyclone III Devices.

(7) For details on the DQ and DQS bus modes support in different device densities, refer to the Cyclone III Handbook Chapter 9: External Memory Interfaces in Cyclone III Devices.

(8) Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage drop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling.

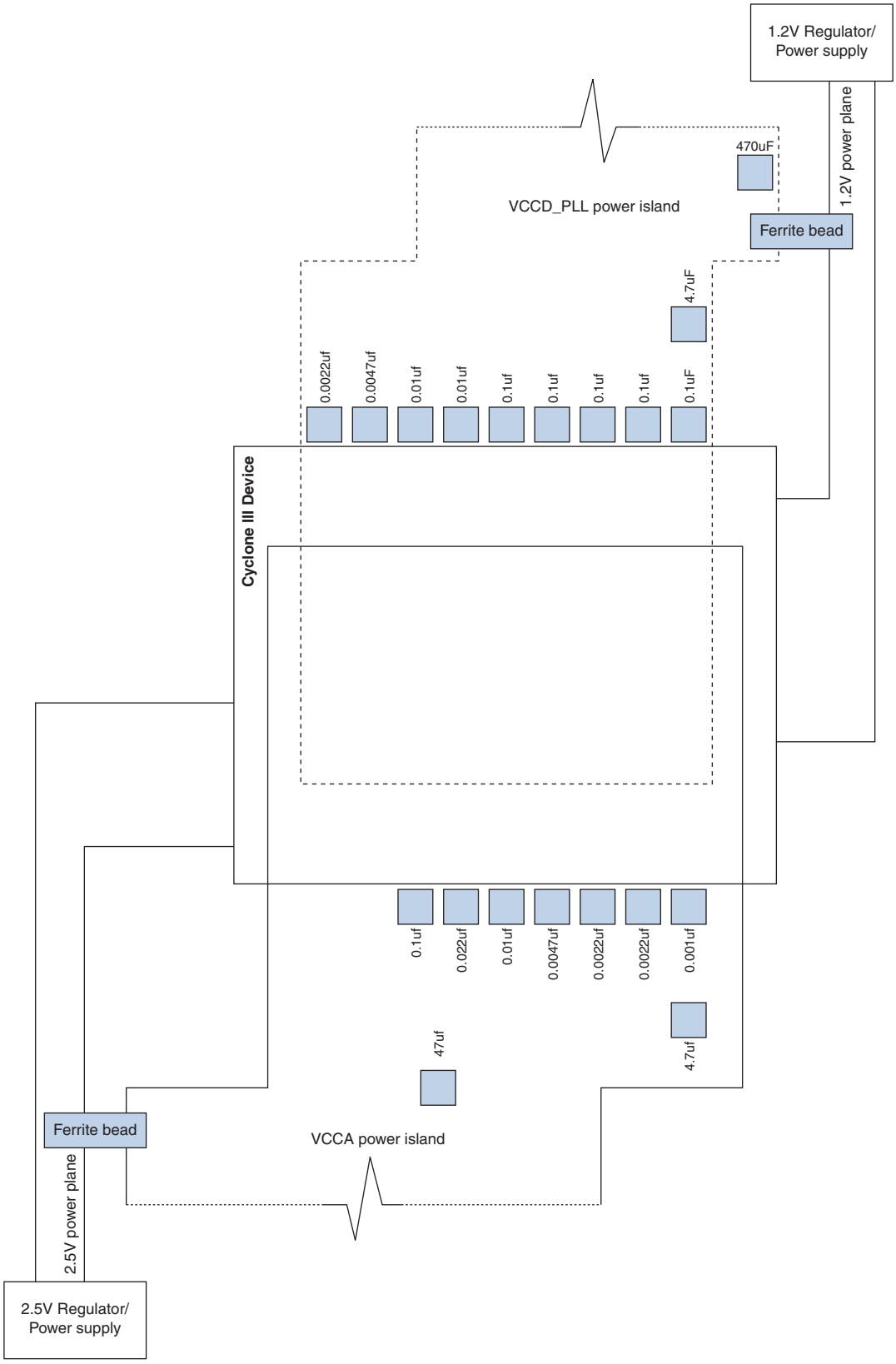
(9) Use a power island for VCCA and VCCD_PLL. PLL power supply may originate from another plane on the board but must be isolated using a ferrite bead or other equivalent methods. If using a ferrite bead, choose an 0402 package with low DC resistance, higher current rating than the maximum steady state current for the supply it is connected to (VCCA or VCCD_PLL) and high impedance at 100MHz.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description	Connection Guidelines

(10) Decouple VCCA power island with a parallel combination of 1x47uF, 1x4.7uF, 1x0.1uF, 1x0.022uF, 1x0.01uF, 1x0.0047uF, 2x0.022uF, 1x0.001uF. Use 0402 package for 0.1uF and smaller capacitors for lower mounting inductance. Place 0.1uF and smaller capacitors as close to the device as possible. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To minimize impact on jitter, a 20mV ripple voltage was used in the analysis for VCCA decoupling. Refer to the figure on page 11 for decoupling capacitor placement guidelines. The figure on page 11 depicts symbolic representation of decoupling scheme and not the exact layout.

(11) Decouple VCCD_PLL power island with a parallel combination of 1x470uF(low ESR Tantalum), 1x4.7uF, 5x0.1uF, 2x0.01uF, 1x0.0047uF, 1x0.0022uF. Use 0402 package for 0.1uF and smaller capacitors for lower mounting inductance. Place 0.1uF and smaller capacitors as close to the device as possible. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To minimize impact on jitter, a 20mV ripple voltage was used in the analysis for VCCD_PLL decoupling. Refer to the figure on page 11 for decoupling capacitor placement guidelines. The figure on page 11 depicts symbolic representation of decoupling scheme and not the exact layout.

(12) The unused pins must be connected as specified in the Quartus II software settings. The default Quartus II setting for unused pins is 'As inputs tri-stated with weak pull-up resistors'. To change the setting, go to 'Assignments', then 'Device'. Click on 'Device & Pin options' dialog box and go to 'Unused Pins' tab. You may choose the desired setting from the 'Reserve all unused pins' drop down list.


1.2V Regulator/
Power supply
1.2V power plane
470uF
VCCD_PLL power island
Ferrite bead
4.7uF
0.0022uf
0.0047uf
0.01uf
0.01uf
0.1uf
0.1uf
0.1uf
0.1uf
0.1uF
Cyclone III Device
0.1uf
0.022uf
0.01uf
0.0047uf
0.0022uf
0.0022uf
0.001uf
4.7uf
47uf
Ferrite bead
VCCA power island
2.5V power plane
2.5V Regulator/
Power supply

Version Number	Date	Changes Made
1.0	10/17/2007	Initial release to Altera Literature site