Arria® V Device Family Pin Connection Guidelines
Preliminary PCG-01013-1.4

The pin connection guidelines are considered preliminary. These pin connection guidelines should only be used as a recommendation, not as a specification.
The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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Arria V (transceiver-based device) Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins			
CLK[0:23][p:n]	I/O, Clock	Dedicated positive and negative clock input pins that can also be used for data inputs. OCT Rd is supported on these pins. When you use the single-ended I/O standard, only the CLK[0:23]p pins serve as the dedicated input pins to the PLL.	When you do not use these pins, Altera recommends tying them to GND or leave them unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUT0, FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUTp, FPLL_[BL,BC,BR,TL,TC,TR]_FB0	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended clock output pins , one differential clock output pair or single ended feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUT1, FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUTn	I/O, Clock		These pins can be tied to GND or left unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUT2, FPLL_[BL,BC,BR,TL,TC,TR]_FBp, FPLL_[BL,BC,BR,TL,TC,TR]_FB1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs, differential external feedback input pin or single ended feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
FPLL_[BL,BC,BR,TL,TC,TR]_CLKOUT3, FPLL_[BL,BC,BR,TL,TC,TR]_FBn	I/O, Clock		These pins can be tied to GND or left unconnected. If unconnected, use the Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
Dedicated Configuration/JTAG Pins			
MSEL[0:4]	Input	Use these pins to set the configuration scheme and POR delay. These pins have an internal 25-kΩ pull-down that is always active.	When you use these pins, tie them directly to VCCPGM or GND to get the combination for the configuration scheme as specified in the "Configuration, Design Security, and Remote System Upgrades in Arria V Devices" chapter in the Arria V Handbook. These pins are not used in the JTAG configuration scheme. Tie the MSEL pins to GND if you are using the JTAG configuration scheme. Use only MSEL pin settings defined in the Arria V device datasheet.
AS_DATA0 / ASDO / DATA[0]	Bidirectional	In a passive serial (PS) or fast passive parallel (FPP) configuration scheme, DATA[0] is a dedicated input data pin. In an active serial (AS) x1 and AS x4 configuration schemes, AS_DATA0 and ASDO are dedicated bidirectional data pins.	When you do not use this pin, Altera recommends leaving the pin unconnected.
AS_DATA[1:3] / DATA[1:3]	Bidirectional	In an AS configuration scheme, AS_DATA[1:3] pins are used. In an FPP x8 or FPP x16 configuration scheme, the DATA[1:3] pins are used.	When you do not use this pin, Altera recommends leaving the pin unconnected.
nCSO/ DATA[4]	Bidirectional	In an AS configuration scheme, the nCSO pin is used. nCSO drives the control signal from the Arria V device to the EPCS or EPCQ device in the AS configuration scheme. In an FPP configuration scheme, the DATA4 pin is used.	When you are not programming the device in the AS configuration scheme, the nCSO pin is not used. When you do not use this pin as an output pin, Altera recommends leaving the pin unconnected.

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nCE	Input	nCE is an active-low chip enable pin. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In a multi-device configuration, the nCE pin of the first device is tied low while its nCEO pin drives the nCE pin of the next device in the chain. In a single-device configuration and JTAG programming, connect the nCE pin to GND.
nCONFIG	Input	Pulling this pin low during configuration and user mode causes the Arria V device to lose its configuration data, enter a reset state, and tri-states all I/O pins. A low-to-high logic initiates a reconfiguration.	When you use the nCONFIG pin in a passive configuration scheme, connect the pin directly to the configuration controller. When you use the nCONFIG pin in an AS configuration scheme, connect the pin through a 10-kΩ resistor tied to VCCPGM. When you do not use the nCONFIG pin, connect the pin directly or through a 10-kΩ resistor to VCCPGM. During JTAG programming, the nCONFIG status is ignored.
CONF_DONE	Bidirectional (open-drain)	As a status output, the CONF_DONE pin drives low before and during configuration. After all configuration data is received without error and the initialization cycle starts, the CONF_DONE pin is released. As a status input, the CONF_DONE pin goes high after all data is received. Then the device initializes and enters user mode. This pin is not available as a user I/O pin.	Connect an external 10-kΩ pull-up resistor to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host.
nCEO	I/O, Output (open-drain)	Dual-purpose open-drain output pin. This pin drives low when device configuration completes.	During multi-device configuration, this pin feeds the nCE pin of the next device in the chain. If this pin is not feeding the nCE pin of the next device, you can use this pin as a regular I/O pin. In a single-device configuration, use this pin as a regular I/O pin. During single-device configuration, you may leave this pin floating. Connect this pin to an external 10-kΩ pull-up resistor to VCCPGM.
nSTATUS	Bidirectional (open-drain)	The Arria V device drives the nSTATUS pin low immediately after power-up and releases it after the Arria V device exits power-on reset (POR). As a status output, the nSTATUS pin is pulled low to indicate an error during configuration. As a status input, the device enters an error state when the nSTATUS pin is driven low by an external source during configuration or initialization. This pin is not available as a user I/O pin.	Connect an external 10-kΩ pull-up resistor to VCCPGM. VCCPGM must be high enough to meet the VIH specification of the I/O on the device and the external host.

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Arria V (transceiver-based device) Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
TCK	Input	JTAG test clock input pin that clock input to the boundary-scan testing (BST) circuitry. Some operations occur at the rising edge, while others occur at the falling edge. It is expected that the clock input waveform have a nominal 50% duty cycle. This pin has an internal 25-kΩ pull-down that is always active.	Connect this pin to a 1-kΩ pull-down resistor to GND.
TMS	Input	JTAG test mode select input pin that provides the control signal to determine the transitions of the test access port (TAP) controller state machine. The TMS pin is evaluated on the rising edge of the TCK pin. Transitions in the state machine occur on the falling edge of the TCK after the signal is applied to the TMS pin. This pin has an internal 25-kΩ pull-up that is always active.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to the VCCPD in the dedicated I/O bank which the JTAG pin resides. To disable the JTAG circuitry, connect the TMS pin to VCCPD using a 1-kΩ resistor.
TDI	Input	JTAG test data input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of the TCK pin. This pin has an internal 25-kΩ pull-up that is always active.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCPD in the dedicated IO bank which the JTAG pin resides. To disable the JTAG circuitry, connect the TDI pin to VCCPD using a 1-kΩ resistor.
TDO	Output	JTAG test data output pin for instructions as well as test and programming data. Data is shifted out on the falling edge of the TCK pin. This pin is tri-stated if the data is not being shifted out of the device.	To disable the JTAG circuitry, leave the TDO pin unconnected. In cases where the TDO pin uses VCCPD = 2.5 V to drive a 3.3 V JTAG interface, there may be leakage current in the TDI input buffer of the interfacing devices. An external pull-up resistor tied to 3.3 V on their TDI pin may be used to eliminate the leakage current if needed.
Optional/Dual-Purpose Configuration			
DCLK	Input (PS, FPP) Output (AS)	Dedicated bidirectional clock pin. In the PS and FPP configuration schemes, the DCLK pin is the clock input used to clock configuration data from an external source into the Arria V device. In the AS configuration scheme, the DCLK pin is an output clock to clock the EPCS or EPCQ device.	Do not leave this pin floating. Drive this pin either high or low.

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CRC_ERROR	I/O, Output (open-drain)	Optional output pin. This pin is an open-drain output pin by default and requires a 10-kΩ pull-up resistor. Active high signal that indicates that the error detection circuitry has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuitry is enabled.	When you use the dedicated CRC_ERROR pin configured as an open-drain output, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the dedicated CRC_ERROR configured as an open-drain output, and when this pin is not used as an I/O pin, connect this pin as defined in the Quartus II software.
DEV_CLRn	I/O, Input	Optional input pin that allows you to override all clears on all the device registers. When this pin is driven low, all registers are cleared. When this pin is driven high (VCCPGM), all registers behave as programmed.	When you do not use the dedicated input DEV_CLRn pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin to GND.
DEV_OE	I/O, Input	Optional input pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated. When this pin is driven high (VCCPGM), all I/O pins behave as programmed.	When you do not use the dedicated input DEV_OE pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin to GND.
DATA[5:15]	I/O, Input	Dual-purpose configuration data input pins. These pins are required for the FPP configuration scheme. Use DATA [5:7] pins for FPP x8, DATA [5:15] pins for FPP x16. You can use the pins that are not required for configuration as regular I/O pins.	When you do not use the DATA[5:15] input pins, and when these pins are not used as I/O pins, Altera recommends leaving these pins unconnected.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as an INIT_DONE pin in the Quartus II software. When this pin is enabled, a transition from low to high on the pin indicates that the device has entered user mode. If the INIT_DONE output pin option is enabled in the Quartus II software, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	When you use the dedicated INIT_DONE pin configured as an open-drain output pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. In Active Serial (AS) multi-device configuration mode, Altera recommends that the INIT_DONE output pin option is enabled in the Quartus II software for devices in the configuration chain. Do not tie INIT_DONE pins together between master and slave devices. Monitor the INIT_DONE status for each device to ensure successful transition into user-mode. When you do not use the dedicated INIT_DONE pin configured as open-drain output pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin as defined in the Quartus II software.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.	When you do not use the CLKUSR pin as a configuration clock input pin, and when the pin is not used as an I/O pin, Altera recommends connecting this pin to GND.

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CvP_CONFDONE	I/O, Output (open-drain)	The CVP_CONFDONE pin is driven low during configuration. When Configuration via Protocol (CvP) is complete, this signal is released and is pulled high by an external pull-up resistor. Status of this pin is only valid if the CONF_DONE pin is high.	When you use the dedicated CvP_CONFDONE pin configured as an open-drain output pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the dedicated CvP_CONFDONE pin configured as open-drain output pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin as defined in the Quartus II software.
nPERST[L0,R0]	I/O, Input	Dedicated fundamental reset pins. These pins are only available when you use them together with the PCI Express® (PCIe®) hard IP. When these pins are low, the transceivers are in reset. When these pins are high, the transceivers are out of reset. When these pins are not used as the fundamental reset, these pins may be used as user I/O pins.	Connect these pins as defined in the Quartus II software.
Partial Reconfiguration Pins			
PR_REQUEST	I/O, Input	Partial reconfiguration request pin. Drive this pin high to start partial reconfiguration. Drive this pin low to end reconfiguration. This pin can only be used in partial reconfiguration using the external host mode in the FPP x16 configuration scheme.	When you do not use the dedicated input PR_REQUEST pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin to GND.
PR_READY	I/O, Output or Output (open-drain)	The partial reconfiguration ready pin is driven low until the device is ready to begin partial reconfiguration. When the device is ready to start reconfiguration, this signal is released and is pulled high by an external pull-up resistor.	When you use the dedicated PR_READY pin configured as an open-drain output pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the dedicated PR_READY pin configured as open-drain output pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin as defined in the Quartus II software.
PR_ERROR	I/O, Output or Output (open-drain)	The partial reconfiguration error pin is driven low during partial reconfiguration unless the device detects an error. If an error is detected, this signal is released and pulled high by an external pull-up resistor.	When you use the dedicated PR_ERROR pin configured as an open-drain output pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the dedicated PR_ERROR pin configured as open-drain output pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin as defined in the Quartus II software.

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PR_DONE	I/O, Output or Output (open-drain)	The partial reconfiguration done pin is driven low until the partial reconfiguration is complete. When the reconfiguration is complete, this signal is released and is pulled high by an external pull-up resistor.	When you use the dedicated PR_DONE pin configured as an open-drain output pin, connect this pin to an external 10-kΩ pull-up resistor to VCCPGM. When you do not use the dedicated PR_DONE pin configured as open-drain output pin, and when this pin is not used as an I/O pin, Altera recommends connecting this pin as defined in the Quartus II software.
Differential I/O Pins			
DIFFIO_RX_[B,T][#:#]p, DIFFIO_RX_[B,T][#:#]n	I/O, RX channel	These are true LVDS receiver channels on column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. OCT Rd is supported on all DIFFIO_RX pins.	Connect unused pins as defined in the Quartus II software.
DIFFIO_TX_[B,T][#:#]p, DIFFIO_TX_[B,T][#:#]n	I/O, TX channel	These are true LVDS transmitter channels on column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.	Connect unused pins as defined in the Quartus II software.
DIFFOUT_[B,T][#:#]p, DIFFOUT_[B,T][#:#]n	I/O, TX channel	These are emulated LVDS output channels. All the user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. External resistor network is needed for emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins	Connect unused pins as defined in the Quartus II software.
External Memory Interface Pins			
DQS[#][B,T,R]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in the Quartus II software.

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DQSn[#][B,T,R]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Quartus II software.
DQ[#][B,T,R]	I/O, bidirectional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in the Quartus II software.
CQ[#][B,T,R]/CQn[#][B,T,R]	I/O, Input	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	Connect unused pins to the CQ/CQn pins in the Pin Planner of the Quartus II software.
QK[#][B,T,R]	I/O, Input	Optional data strobe signal for use in RLDRAM II.	Connect unused pins to the QK[#] pins in the Pin Planner of the Quartus II software. (Sbar in the Quartus II Pin Planner)
QKn[#][B,T,R]	I/O, Input	Optional complementary data strobe signal for use in RLDRAM II.	Connect unused pins to the QKn[#] pins in the Pin Planner of the Quartus II software. (S in the Quartus II Pin Planner)
Hard PHY Only			
DQS[#]_[1:8]	I/O, bidirectional	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	Connect unused pins as defined in the Quartus II software.
DQS#[#]_[1:8]	I/O, bidirectional	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	Connect unused pins as defined in the Quartus II software.
DQ[#]_[1:8]_[#]	I/O, bidirectional	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	Connect unused pins as defined in the Quartus II software.
CQ[#]_[1:8]/CQ#[#]_[1:8]	I/O, Input	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.	Connect unused pins to the CQ/CQn pins in the Pin Planner of the Quartus II software.
QK[#]_[1:8]	I/O, Input	Optional data strobe signal for use in RLDRAM II.	Connect unused pins to the QK[#] pins in the Pin Planner of the Quartus II software. (Sbar in the Quartus II Pin Planner)

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QK#[#]_[1:8]	I/O, Input	Optional complementary data strobe	Connect unused pins to the QKn[#] pins in the Pin Planner of the Quartus II software. (S in the Quartus II Pin Planner)
DM[#]_[1:8]	I/O, Output	Optional Write Data Mask, edge-aligned to DQ during Write.	Connect unused pins as defined in the Quartus II software.
WE#_[1:8]	I/O, Output	Write enable. Write-enable input for DDR2, DDR3 SDRAM and RLDRAM II	Connect unused pins as defined in the Quartus II software.
CAS#_[1:8]	I/O, Output	Column Address Strobe for DDR2 & DDR3 SDRAM	Connect unused pins as defined in the Quartus II software.
RAS#_[1:8]	I/O, Output	Row Address Strobe for DDR2 & DDR3 SDRAM.	Connect unused pins as defined in the Quartus II software.
RPS#_[1:8]	IO, Output	Read signal to QDRII memory. Active low and reset in the inactive state	Connect unused pins as defined in the Quartus II software.
WPS#_[1:8]	IO, Output	Write signal to QDRII memory. Active low & reset in the inactive state.	Connect unused pins as defined in the Quartus II software.
RESET#_[1:8]	IO, Output	Active low reset signal.	Connect unused pins as defined in the Quartus II software.
CK_[1:8]	IO, Output	Input clock for external memory devices	Connect unused pins as defined in the Quartus II software.
CK#_[1:8]	IO, Output	Input clock for external memory devices, inverted CK	Connect unused pins as defined in the Quartus II software.
CKE_[1:8]_[#]	IO, Output	Active low clock enable.	Connect unused pins as defined in the Quartus II software.
BA_[1:8]_[#]	IO, Output	Bank address input for DDR2, DDR3 SDRAM and RLDRAM II	Connect unused pins as defined in the Quartus II software.
A_[1:8]_[#]	IO, Output	Address input for DDR2, DDR3 SDRAM, RLDRAM II and QDRII/+ SRAM	Connect unused pins as defined in the Quartus II software.
CS#_[1:8]_[#]	IO, Output	Active low Chip Select.	Connect unused pins as defined in the Quartus II software.
CA_[1:8]_[#]	IO, Output	Command and address input for LPDDR SDRAM	Connect unused pins as defined in the Quartus II software.
REF#_[1:8]	IO, Output	Auto-refresh control input for RLDRAM II	Connect unused pins as defined in the Quartus II software.
ODT_[1:8]_[#]	IO, Output	On die termination signal to set the termination resistors to each pin.	Connect unused pins as defined in the Quartus II software.
Reference Pins			
RZQ_[0,1,5,6]	I/O, Input	Reference pins for I/O banks. The RZQ pins share the same VCCIO with the I/O bank where they are located. The external precision resistor must be connected to the designated pin within the bank. If not required, this pin is a regular I/O pin.	If the device does not use this dedicated input for the external precision resistor or as an I/O, Altera recommends connecting the pin to GND. If used for OCT calibration, the RZQ pin is connected to GND through an external 100- or 240- reference resistor depending on the desired OCT impedance. Refer to the Arria V handbook for the OCT impedance options for the desired OCT scheme.
DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, ground, or any other signal. These pins must be left floating.
NC	No Connect	Do not drive signals into these pins.	When designing for device migration these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.

Arria® V Device Family Pin Connection Guidelines
Preliminary PCG-01013-1.4

Altera recommends that you create a Quartus® II design, enter your device I/O assignments, and compile the design. The Quartus II software will check your pin connections according to I/O assignment and placement rules. The rules differ from one device to another based on device density, package, I/O assignments, voltage assignments, and other factors that are not fully described in this document or the device handbook.

Arria V (transceiver-based device) Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Supply Pins (See Notes 4 through 7)			
VCC	Power	VCC supplies power to the core.	Connect all VCC pins to a 1.1V low noise switching regulator for the Arria V GX -C4, -C5, -I5, -C6, and Arria V GT -I5 devices. Connect all VCC pins to a 1.15V low noise switching regulator for the Arria V GX -I3 and GT -I3 devices. VCCP maybe sourced from the same regulator as VCC with proper isolation filters. Use Arria V Early Power Estimator to determine the current requirements for VCC and other power supplies. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 6, and 7.
VCCP	Power	VCCP supplies power to the periphery, HIP, and PCS.	Connect VCCP pins to a 1.1V low noise switching regulator for the Arria V GX -C4, -C5, -I5, -C6, and Arria V GT -I5 devices. Connect all VCCP pins to a 1.15V low noise switching regulator for the Arria V GX - I3 and GT -I3 devices. These pins may be tied to the same regulator as VCC with proper isolation filters. Separate VCC and VCCP planes into two different power layers on the PCB. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 6, and 7.
VCCD_FPLL	Power	PLL Digital power.	Connect all VCCD_FPLL pins to a 1.5V linear or low noise switching power supply. These pins may be tied to the same regulator as VCCH_GXB and VCCBAT. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCCA_FPLL	Power	PLL Analog power.	Connect these pins to a 2.5V low noise switching power supply through a proper isolation filter. This power rail may be shared with VCCAUX and VCCA_GXB. With a proper isolation filter these pins may be sourced from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCCAUX	Power	Auxiliary supply for the programmable power technology.	Connect all VCCAUX pins to a 2.5V low noise switching power supply through a proper isolation filter. This power rail may be shared with VCCA_GXB and VCCA_FPLL. With a proper isolation filter these pins may be sourced from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 7.
VCCIO[3,4,7,8]	Power	These are I/O supply voltage pins for I/O banks. Each bank can support a different voltage level from 1.2V to 3.3V. Supported IO standards are LVTTL/ LVCMOS (3.3, 3.0, 2.5, 1.8, 1.5, 1.2V), SSTL(2,18,15 Class-I/II), SSTL(135, 125), HSTL(18,15,12 Class-I/II), HSUL12, LVDS, LVPECL, PCI/PCI-X.	Connect these pins to 1.2V, 1.25V, 1.35V, 1.5V, 1.8V, 2.5V, 3.0V, or 3.3V supplies, depending on the I/O standard connected to the specified bank. When these pins require 2.5V they may be tied to the same regulator as VCCPD and VCCPGM, but only if each of these supplies require 2.5V sources. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, and 8.
VCCPGM	Power	Configuration pins power supply which support 1.8, 2.5, 3.0 & 3.3V	Connect these pins to either 1.8V, 2.5V, 3.0V, or 3.3V power supply. When these pins require 2.5V they may be tied to the same regulator as VCCIO and VCCPD, but only if each of these supplies require 2.5V sources. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2 and 3.
VCCPD[3,4,7,8]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 2.5V, 3.0 & 3.3V.	The VCCPD pins require 2.5V, 3.0V, or 3.3V power supply. When these pins have the same voltage requirements as VCCPGM and VCCIO, they maybe tied to the same regulator. The voltage on VCCPD is dependent on the VCCIO voltage. When VCCIO is 3.3V, VCCPD must be 3.3V. When VCCIO is 3.0V, VCCPD must be 3.0V. When VCCIO is 2.5V or less, VCCPD must be 2.5V. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 4, and 8.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.	If you are using design security volatile key, connect this pin to a non-volatile battery power source in the range of 1.2V to 3.0V. If you are not using the volatile key, connect this pin to a 1.5V, 2.5V, or 3.0V power supply. Arria V devices will not exit POR if VCCBAT stays at logic low.
GND	Ground	Device ground pins.	Connect all GND pins to the board ground plane.

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Arria V (transceiver-based device) Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VREF[#]N0	I/O, Power	Input reference voltage for each I/O bank. If a bank uses a voltage referenced I/O standard for input operation, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.	If VREF pins are not used, connect these pins to either the VCCIO in the bank in which the pin resides or GND. When VREF pins are used as I/O, they have higher capacitance than regular I/O pins which will slow the edge rates and affect I/O timing. Decoupling depends on the design decoupling requirements of the specific board. See Notes 2 and 8.
Transceiver Pins (See Notes 4 through 10)			
VCCR_GXB[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.	Connect VCCR_GXB pins to a 1.1V low noise switching regulator for the Arria V GX -C4, -C5, -I3, -I5, and -C6 devices with transceiver data rates <= 3.125Gbps. Connect VCCR_GXB pins to a 1.15V low noise switching regulator for the Arria V GX -C4, -C5, -I3 and -I5 devices with transceiver data rates > 3.125Gbps. Connect VCCR_GXB pins to a 1.2V low noise switching regulator for the Arria V GT devices. For Arria V GX -C4, -C5, -I5, and -C6 devices with transceiver data rates <= 3.125Gbps, these pins may be tied to the same 1.1V regulator as VCC with a proper isolation filter. For Arria V GX -C4, -C5, and -I5 devices with transceiver data rates >3.125Gbps, Arria V GX -I3 devices, and Arria V GT devices, these pins may be tied to the same regulator as VCCL_GXB. Decoupling of these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 7, and 10.
VCCT_GXB[L,R][0..3]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.	Connect VCCT_GXB pins to a 1.1V low noise switching regulator for the Arria V GX -C4, -C5, -I3, -I5, and -C6 devices with transceiver data rates <= 3.125Gbps. Connect VCCT_GXB pins to a 1.15V low noise switching regulator for the Arria V GX -C4, -C5, -I3 and -I5 devices with transceiver data rates > 3.125Gbps. Connect VCCT_GXB pins to a 1.2V low noise switching regulator for the Arria V GT devices. For Arria V GX -C4, -C5, -I5, and -C6 devices with transceiver data rates <= 3.125Gbps, these pins may be tied to the same 1.1V regulator as VCC with a proper isolation filter. For Arria V GX -C4, -C5, and -I5 devices with transceiver data rates >3.125Gbps, Arria V GX -I3 devices, and Arria V GT devices, these pins may be tied to the same regulator as VCCR_GXB and VCCL_GXB with a proper isolation filter. Decoupling of these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 7, and 10.
VCCL_GXB[L,R][0..3]	Power	Analog power, Clock network power, specific to the left (L) or the right (R) of the device.	Connect VCCL_GXB pins to a 1.1V low noise switching regulator for the Arria V GX -C4, -C5, -I3, -I5, and -C6 devices with transceiver data rates <= 3.125Gbps. Connect VCCL_GXB pins to a 1.15V low noise switching regulator for the Arria V GX -C4, -C5, -I3 and -I5 devices with transceiver data rates > 3.125Gbps. Connect VCCL_GXB pins to a 1.2V low noise switching regulator for the Arria V GT devices. For Arria V GX -C4, -C5, -I5, and -C6 devices with transceiver data rates <= 3.125Gbps, these pins may be tied to the same 1.1V regulator as VCC with a proper isolation filter. For Arria V GX -C4, -C5, and -I5 devices with transceiver data rates >3.125Gbps, Arria V GX -I3 devices, and Arria V GT devices, these pins may be tied to the same regulator as VCCR_GXB. Decoupling of these pins depends on the design decoupling requirements of the specific board. See Notes 2, 3, 7, and 10.
VCCH_GXB[L,R][0..3]	Power	Analog power, transmitter output buffer power, specific to the left (L) or the right (R) of the device.	Connect VCCH_GXB to a 1.5V linear or low noise switching regulator. These pins may be sourced from the same regulator as VCCD_FPLL and VCCBAT. Decoupling of these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 7, and 10.
VCCA_GXB[L,R][0..3]	Power	Analog power, transceiver high voltage power, specific to the left (L) side or right (R) side of the device.	Connect VCCA_GXB to a 2.5V low noise switching regulator. This power rail may be shared with VCCA_FPLL and VCCAUX. With a proper isolation filter these pins may be sourced from the same regulator as VCCIO, VCCPD and VCCPGM when each of these power supplies require 2.5V. Decoupling of these pins depends on the design decoupling requirements of the specific board design. See Notes 2, 3, 4, 7, and 10.
GXB_RX_[L,R][0:11][p,n], GXB_REFCLK_[L,R][0:11][p,n]	Input	High speed positive (p) or negative (n) differential receiver channels. High speed positive (p) or negative (n) differential reference clock Specific to the left (L) side or right (R) side of the device.	These pins are AC-coupled when used. Connect all unused pins directly to GND. Some GXB_RX pins have the 10Gbps capability in the Arria V GT device. For details, refer to the Transceiver Architecture chapter in the Arria V Device Handbook. See Note 9.

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Arria V (transceiver-based device) Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
GXB_TX_[L,R][0:11][p,n]	Output	High speed positive (p) and negative (n) differential transmitter channels. Specific to the left (L) side or right (R) side of the device.	Leave all unused GXB_TXp pins floating. Some GXB_TX pins have the 10Gbps capability in the Arria V GT device. For details, refer to the Transceiver Architecture chapter in the Arria V Device Handbook.
REFCLK[0:3][L,R]_[p:n]	Input	High speed positive (p) & negative (n) differential reference clock, specific to the left (L) side or right (R) side of the device.	These pins may be AC-coupled or DC-coupled when used. For HCSL I/O standard, it only support DC coupling. Connect all unused pins directly to GND. See Note 9.
RREF_BR	Input	Reference resistor for right (R) side transceiver, and bottom (B) and right (R) sides PLL of the device.	If any PLL on the right and bottom sides of the device is used, or any REFCLK pin or transceiver channel on right side of the device is used, you must connect each RREF pin on that side of the device to its own individual 2.0-kΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.
RREF_TL	Input	Reference resistor for left (L) side transceiver, and top (T) and left (L) sides PLL of the device.	If any PLL on the left and top sides of the device is used, or any REFCLK pin or transceiver channel on left side of the device is used, you must connect each RREF pin on that side of the device to its own individual 2.0-kΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

1) These pin connection guidelines are based on the Arria V GX and GT device variants.
2) Select the capacitance values for the power supply after you consider the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. Calculate the target impedance for the power plane based on current draw and voltage droop requirements of the device/supply. Then, decouple the power plane using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to “Equivalent Series Inductance” of the mounting of the packages. Consider proper board design techniques such as interplane capacitance with low inductance for higher frequency decoupling.

3) Use the Arria V Early Power Estimator to determine the current requirements for VCC and other power supplies.
4) These supplies may share power planes across multiple Arria V devices.
5) Example 1 and Figure 1 illustrate the power supply sharing guidelines for Arria V GX -C4, -C5, -I5, and -C6 devices with transceiver data rates <=3.125Gbps. Example 2 and Figure 2 illustrate the power supply sharing guidelines for Arria V GX -C4, -C5, and -I5 devices with transceiver data rates >3.125Gbps. Example 3 and Figure 3 illustrate the power supply sharing guidelines for Arria V GX -I3 devices. Example 4 and Figure 4 illustrate the power supply sharing guidelines for Arria V GT -I3 devices. Example 5 and Figure 5 illustrate the power supply sharing guidelines for Arria V GT -I5 devices.
6) Power pins should not share breakout vias from the BGA. Each ball on the BGA must have its own dedicated breakout via. VCC and VCCP must not share breakout vias.
7) Low Noise Switching Regulator - a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800 kHz and 1 MHz and has fast transient response.
Line Regulation < 0.4%
Load Regulation < 1.2%
8) The number of modular I/O banks on Arria V devices depends on the device density. For the indexes available for a specific device, refer to the I/O Bank section in the Arria V handbook.
9) For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires that the AC-coupling capacitor is placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
10) If all the transceivers on one side of the device are not used, you may tie the transceiver power pins on that side to GND.
11) For item [#], refer to the device pin table for the pin-out mapping.

Example 1. Power Supply Sharing Guidelines for Arria V GX -C4, -C5, -I5, and -C6 with Transceiver Data Rates <= 3.125Gbps

Example Requiring 3 Power Regulators

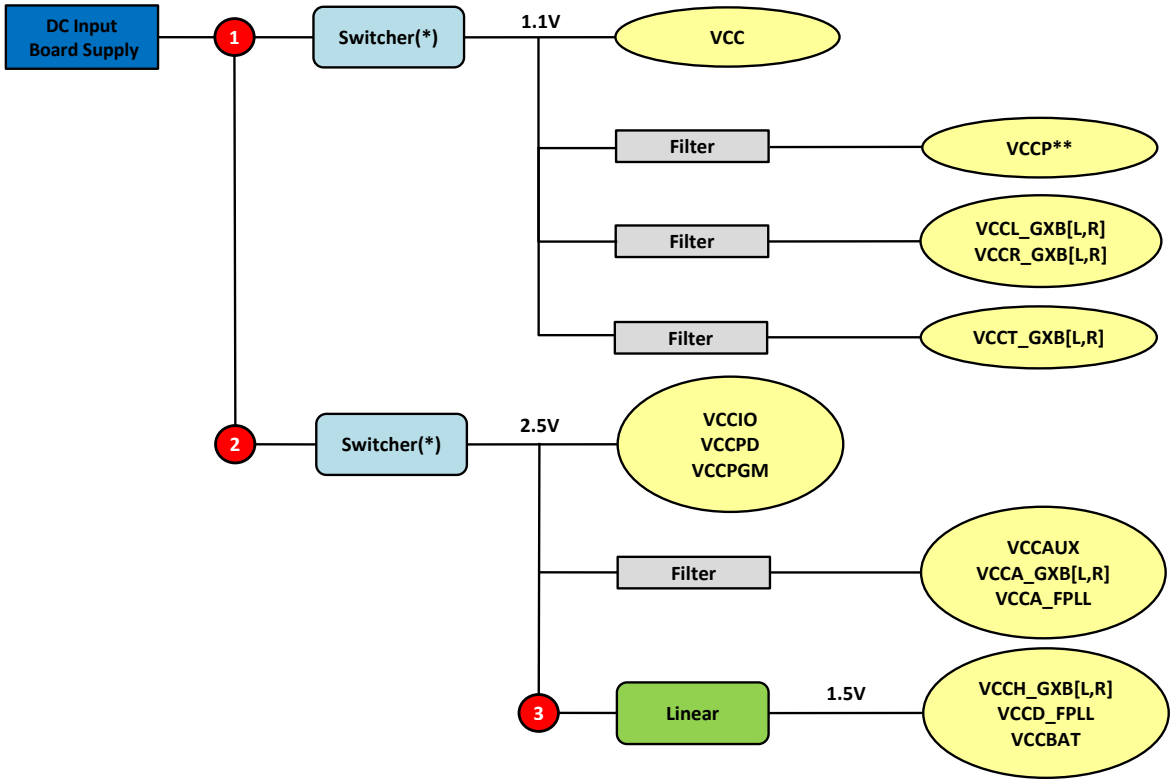
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP, VCCL_GXB, VCCR_GXB and VCCT_GXB with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]					Isolate	
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	2	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCCAUX		2.5			Isolate	May be able to share VCCAUX, VCCA_GXB and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCH_GXB[L,R]	3	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GX is provided in Figure 1.

Figure 1. Example Power Supply Block Diagram for Arria V GX -C4, -C5, -I5, and -C6 with Transceiver Data Rates <= 3.125Gbps



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping VCC and VCCP power rails isolated from each and on separate layers of the PCB.

Example 2. Power Supply Sharing Guidelines for Arria V GX -C4, -C5, and -I5 with Transceiver Data Rates > 3.125Gbps

Example Requiring 4 Power Regulators

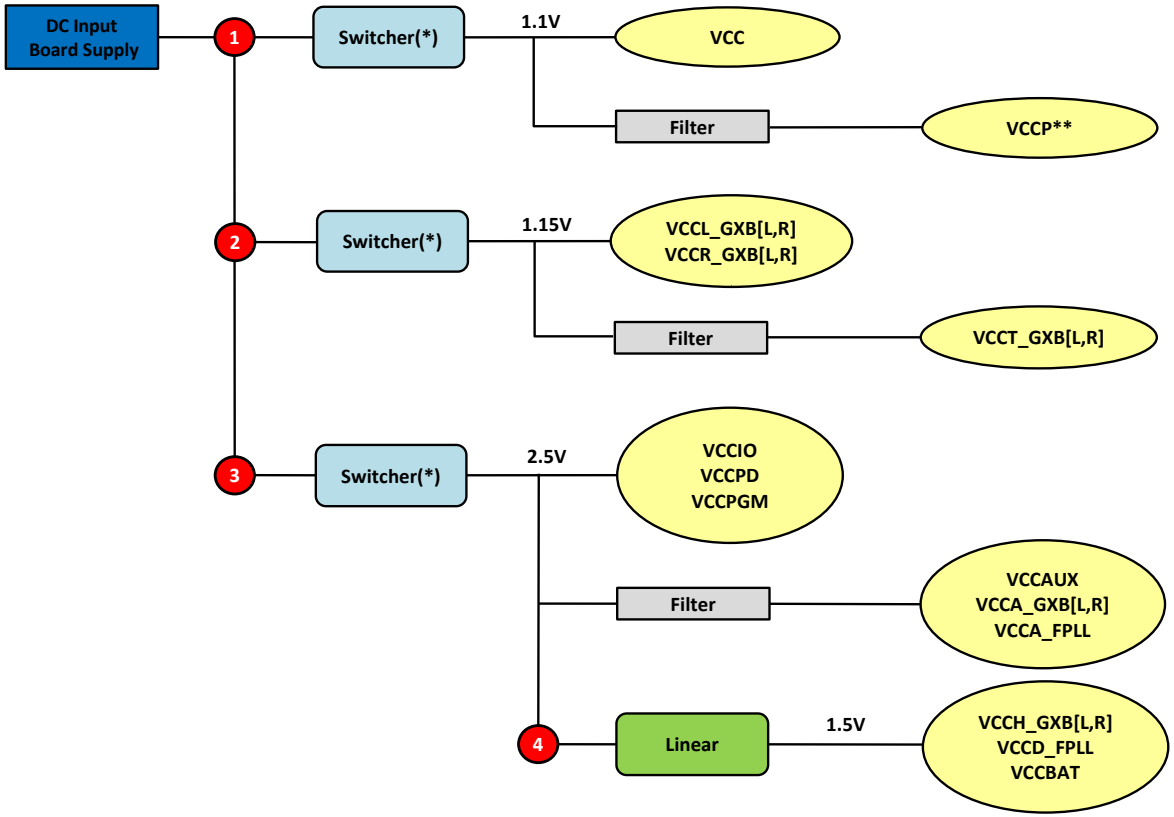
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCCAUX		2.5			Isolate	May be able to share VCCAUX, VCCA_GXB and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GX is provided in Figure 2.

Figure 2. Example Power Supply Block Diagram for Arria V GX -C4, -C5, and -I5 with Transceiver Data Rates > 3.125Gbps



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping VCC and VCCP power rails isolated from each and on separate layers of the PCB.

Example 3. Power Supply Sharing Guidelines for Arria V GX -I3

Example Requiring 4 Power Regulators

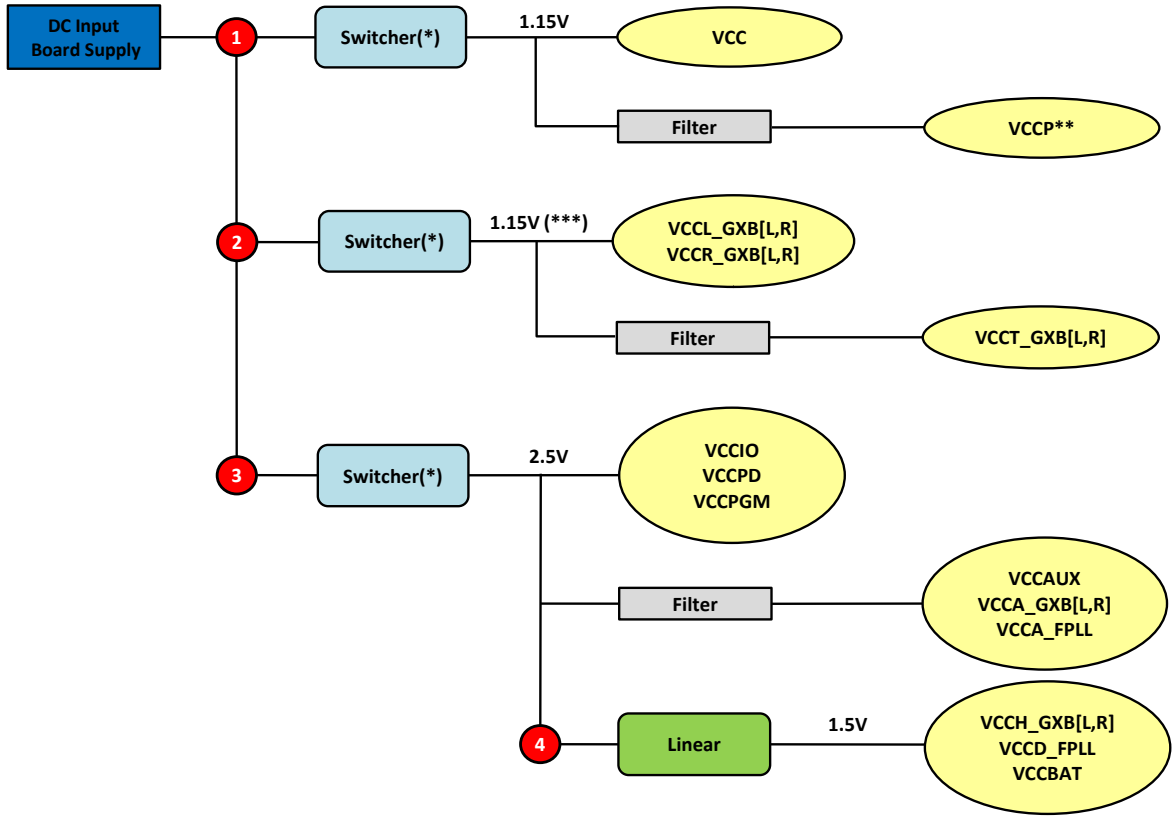
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.15 (**)	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCCAUX		2.5			Isolate	May be able to share VCCAUX, VCCA_GXB and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** VCCL_GXB[L,R], VCCR_GXB[L,R], and VCCT_GXB[L,R] can be 1.1V when the transceiver data rate is <= 3.125Gbps.

Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GX -I3 is provided in Figure 3.

Figure 3. Example Power Supply Block Diagram for Arria V GX -I3



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping VCC and VCCP power rails isolated from each and on separate layers of the PCB.
*** VCCL_GXB[L,R], VCCR_GXB[L,R], and VCCT_GXB[L,R] can be 1.1V when the transceiver data rate is <= 3.125Gbps.

Example 4. Power Supply Sharing Guidelines for Arria V GT -I3

Example Requiring 4 Power Regulators

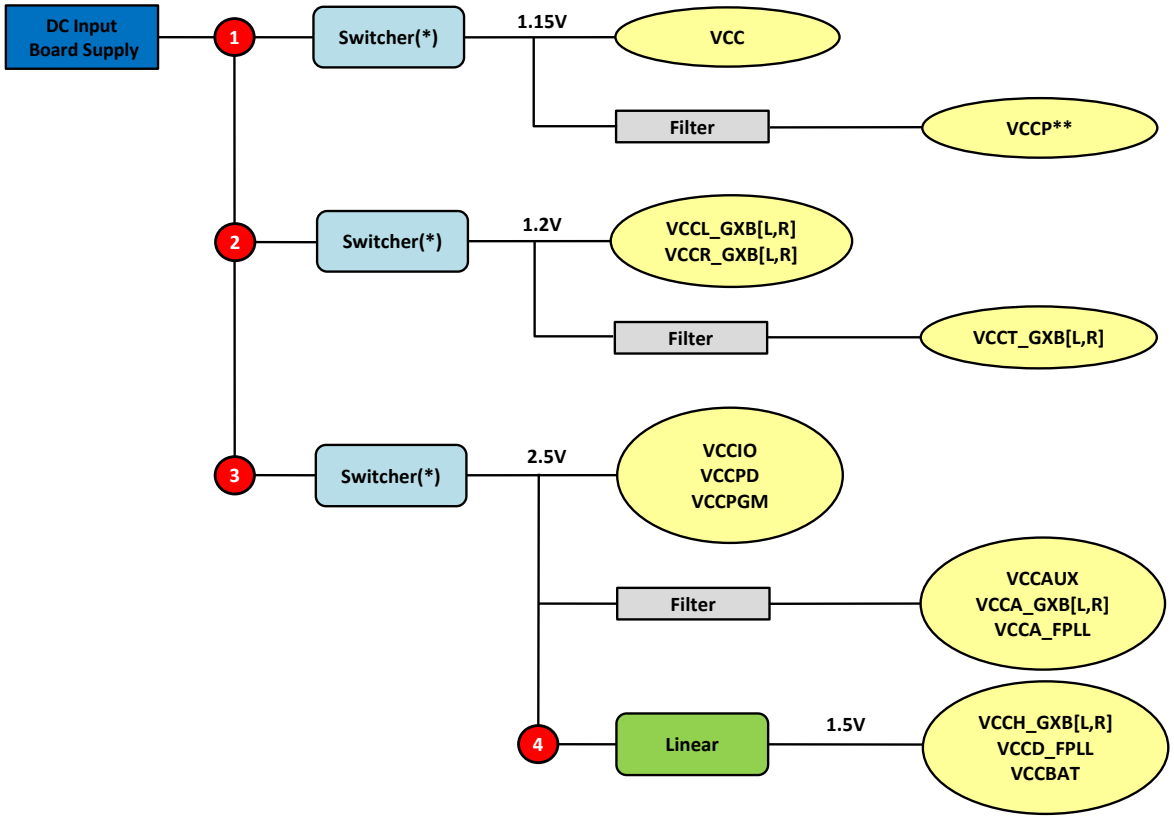
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.15	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.2	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCCAUX		2.5			Isolate	May be able to share VCCAUX, VCCA_GXB and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GT -I3 is provided in Figure 4.

Figure 4. Example Power Supply Block Diagram for Arria V GT -I3



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping VCC and VCCP power rails isolated from each and on separate layers of the PCB.

Example 5. Power Supply Sharing Guidelines for Arria V GT -I5

Example Requiring 4 Power Regulators

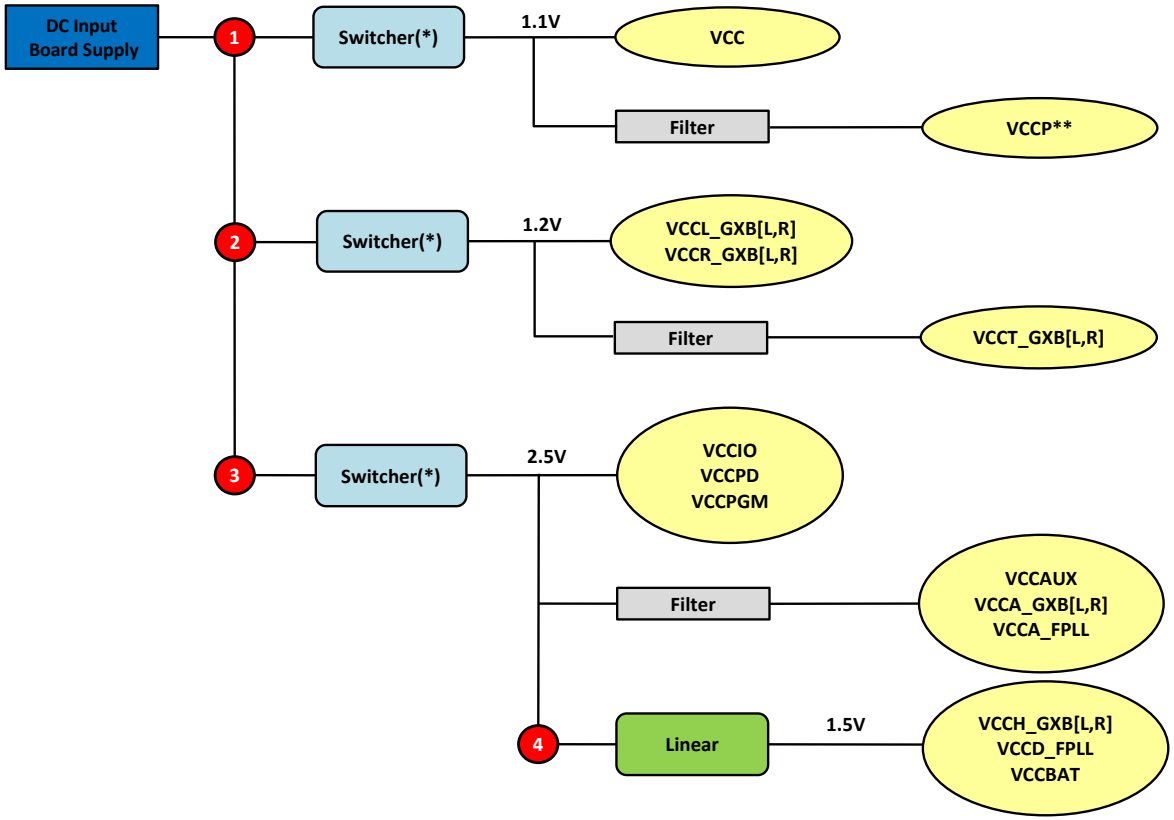
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC	1	1.1	± 30mV	Switcher (*)	Share	May be able to share VCCP with VCC with proper isolation filters.
VCCP					Isolate	
VCCL_GXB[L,R]	2	1.2	± 30mV	Switcher (*)	Share	May be able to share VCCT_GXB with the same regulator as VCCL_GXB and VCCR_GXB with proper isolation filters.
VCCR_GXB[L,R]						
VCCT_GXB[L,R]					Isolate	
VCCIO	3	Varies	± 5%	Switcher (*)	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require as many regulators as there are variations of supplies in your specific design. VCCPD must be greater than or equal to VCCIO. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD						
VCCPGM						
VCCAUX		2.5			Isolate	May be able to share VCCAUX, VCCA_GXB and VCCA_FPLL with the same regulator as VCCIO, VCCPD and VCCPGM when all power rails require 2.5V, but only with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCA_GXB[L,R]						
VCCA_FPLL						
VCCH_GXB[L,R]	4	1.5	± 5%	Linear	Share	VCCH_GXB, VCCD_FPLL and VCCBAT may share regulators. Depending on the regulator capabilities this supply may be shared with multiple Arria V devices.
VCCD_FPLL						
VCCBAT						

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.

Use the EPE (Early Power Estimation) tool to assist in determining the power required for your specific design.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria V GT -I5 is provided in Figure 5.

Figure 5. Example Power Supply Block Diagram for Arria V GT -I5



*When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 7.
** Altera recommends keeping VCC and VCCP power rails isolated from each and on separate layers of the PCB.

Arria ® V Device Family Pin Connection Guidelines Preliminary PCG-01013-1.4		
Revision History		
Revision	**Description of Changes**	**Date**
1.0	Initial Release.	8/17/2011
1.1	Split VCC to VCC and VCCP.	1/9/2012
1.2	Updated the transceivers voltages.	6/1/2012
1.3	Updated the transceivers voltages for the Arria V GX -C4, -C5, -I5, and -C6 devices.	6/22/2012
1.4	Added Arria V GX -I3 information, updated VCCPD connection guidelines, and RREF connection guidelines.	7/24/2012