PLS167-33, PLSCE167H-33
PLS168-33, PLSCE168H-33

24-Pin TTL/CMOS Programmable Logic Sequencers

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- Field-programmable replacement for sequential control logic
- Advanced Mealy state machine/sequencer architecture
- Programmable AND/programmable OR array for flexibility
- Full drive: 24 mA I_{OL}, three-state outputs
- Dedicated hardware features to enhance testability
  - Diagnostic Mode access to buried state register
  - Register Preload and Power-up Preset of all flip-flops
- User-programmable pin for asynchronous flip-flop Preset/Output Enable
- Automatic "Hold" state via S-R flip-flops
- Security bit hides proprietary designs from competitors
- Supported by PALASM® software and standard PLD programmers
- Available in 24-pin plastic SKINNYDIP® and 28-pin PLCC packages
- Fabricated with high-performance bipolar and electrically erasable CMOS technology

GENERAL DESCRIPTION

The PLS167 and PLS168 are field-programmable replacements for sequential logic. The devices function as Mealy state machines with a registered output. The PLS utilizes the familiar AND/OR PLA logic structure to implement sum-of-product equations. Both arrays are user-programmable to implement transition terms causing changes in the internal state register or output register. The PLS167/8-33 devices are fabricated in Advanced Micro Devices' advanced oxide-isolated bipolar process. The PLSCE167/8H-37 devices are fabricated in a high-speed, EE CMOS process; they offer significant power improvement (I_{CC} of 100 mA) over competing parts.

The PLS devices are fully supported by industry-standard CAD tools, including the PALASM design software package. Device programming is accomplished by using standard PLD programmers.

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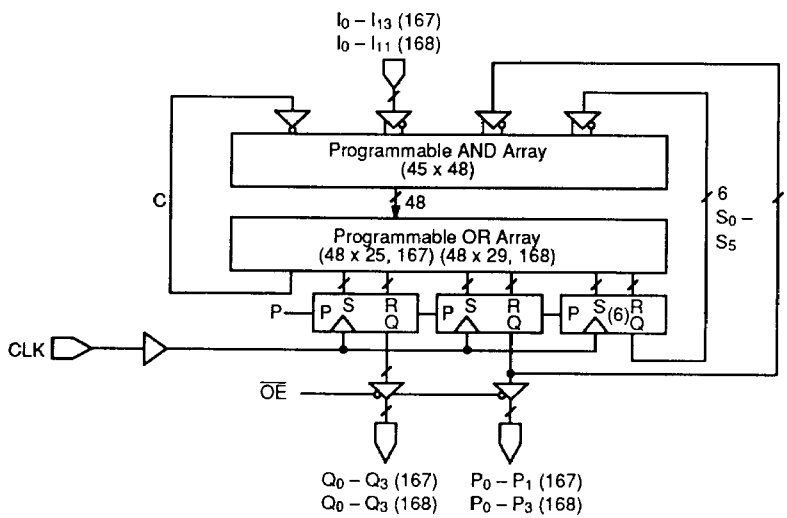
BLOCK DIAGRAM

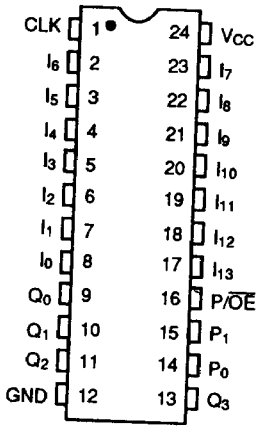


14081-001A

Publication # 14081 Rev. A Amendment /0
Issue Date: January 1990

CONNECTION DIAGRAMS

PLS167 SKINNYDIP



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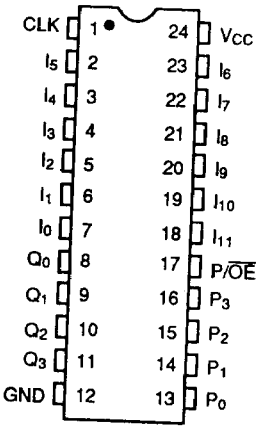
PLS168 SKINNYDIP



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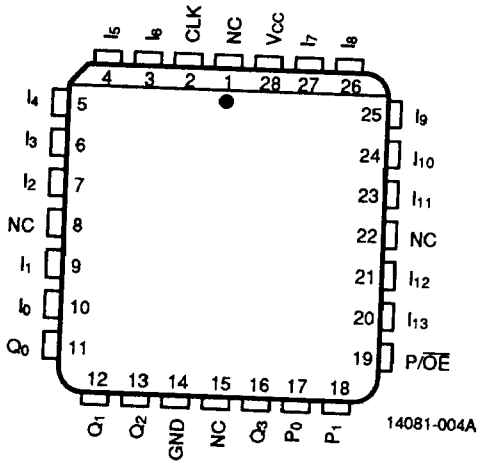
PLCC



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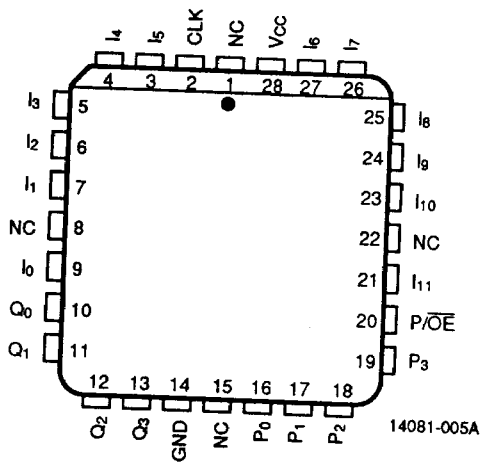

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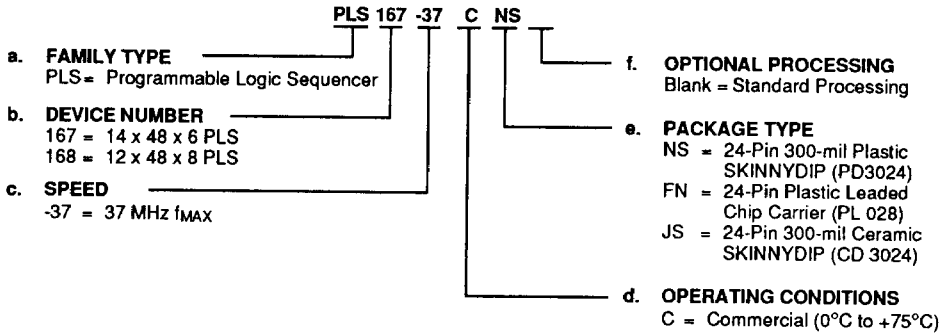
PIN DESIGNATIONS

CLK	Output/state register clock
GND	Ground
I	Inputs to AND array
P	Programmable output/state register
P/$\overline{OE}$	Programmable asynchronous function pin; default is active-high Preset (all registers go HIGH), programmed is active-low Output Enable
Q	Output register outputs
V_{CC}	Supply Voltage

ORDERING INFORMATION
Commercial Products (Bipolar Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Device Number**
c. **Speed**
d. **Operating Conditions**
e. **Package Type**
f. **Optional Processing**



Valid Combinations	
PLS167-37	CNS, CFN, CJS
PLS168-37	

Valid Combinations

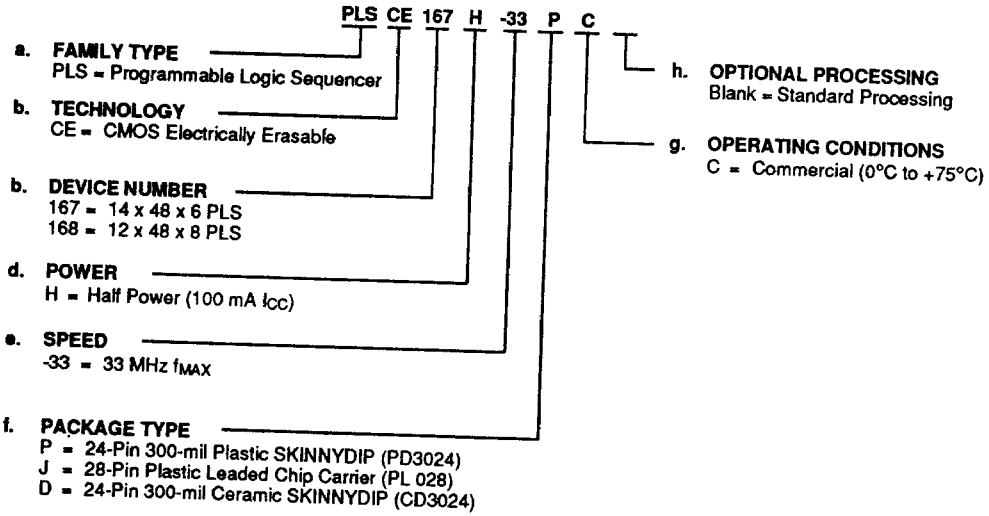
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with MMI logo.

ORDERING INFORMATION
Commercial Products (CMOS Only)

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

a. **Family Type**
b. **Technology**
c. **Device Number**
d. **Power**
e. **Speed**
f. **Package Type**
g. **Operating Conditions**
h. **Optional Processing**



Valid Combinations	
PLSCE167H-33	PC, JC, DC
PLSCE168H-33	

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

FUNCTIONAL DESCRIPTION

State Machine Implementation

State machines contain conditional input logic, state memory and output generation logic. The PLS device is built around a programmable AND/OR logic array which serves as both conditional input and output generation logic. Forty-eight product or transition terms are found in the AND array. The AND array is driven from several sources: there are twelve to fourteen external inputs, six internal feedback signals from the buried state registers, two to four progammable registers, and the complement term.

The OR array drives the output registers, programmable registers, buried state registers, and the complement array term. The PLS device offers six to eight output registers and six buried state registers.

Architectural Details

Part Number	Pins	Inputs	Flip-Flops	Outputs
PLS167	24	14	12	6
PLS168	24	12	14	8

State and Output Registers

The state and output registers are both implemented with edge-triggered S-R type flip-flops. If neither input is active, the flip-flop will retain its contents when clocked. This free "hold" state saves product terms. The registers may change only on the LOW-to-HIGH transition of the clock pulse. There are four output registers, two output/buried registers and six buried state registers on the PLS167 device, and two additional output/buried registers on the PLS168 device.

Logic Implementation

All transition terms can include True, False, or Don't Care states of the controlling variables. The OR array merges one or more product terms to generate the desired user logic functions for the output and next-state registers. This sharing of OR-terms minimizes the overall logic required to implement complicated control functions.

Complement Array Term

An internal variable (C) known as the complement array term directly implements the "else" logic clause at any state. This often reduces the number of product terms required for a conditional "else" transition . The complement array can also be used for illegal state recovery and designing modulo counters.

Initialization

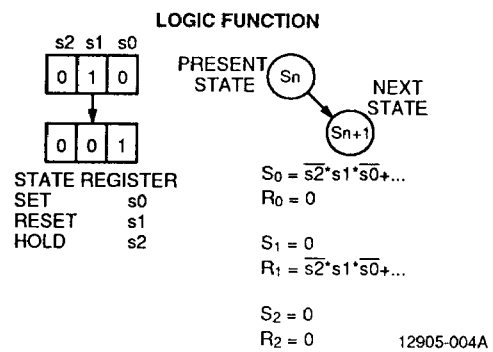
Starting the state machine in a known state is facilitated by power-up preset circuitry which unconditionally loads a "1" into each flip-flop during power-up or by using the asynchronous Preset function. Synchronous transitions to the initial state can be made by having an input be an OR term on all the state register S inputs, and ANDing its complement with all of the R logic terms. Whenever this input is active the machine will synchronously change to the state with all outputs high.

Output Enable

The Preset input can be converted to a three-state Output Enable function by an architecture bit. Expansion to larger control functions can be accommodated by connecting several PLS devices to a control bus and selectively enabling them to each handle a segment of the control algorithm. This user-programmable option is specified as an auxiliary equation in the design file or optionally by use of a keyword.

Typical Operation

The details of device operation may be illustrated by the simple state transition indicated. The state register initially contains 010 and will become 001 after the next clock. For this to occur, state bit 0 must be set, state bit 1 must be reset and state bit 2 must hold its value. The transition term fragments listed produce this result. The S_0 and R_1 product terms detect the bit pattern for the current state (010) and produce a logic one. All other terms evaluate to a zero, producing the transition to state 001.



Typical State Transition

Security Bit

A security bit is provided on the PLS167/8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback of the programmed pattern by a device programmer, securing proprietary designs from competitors.

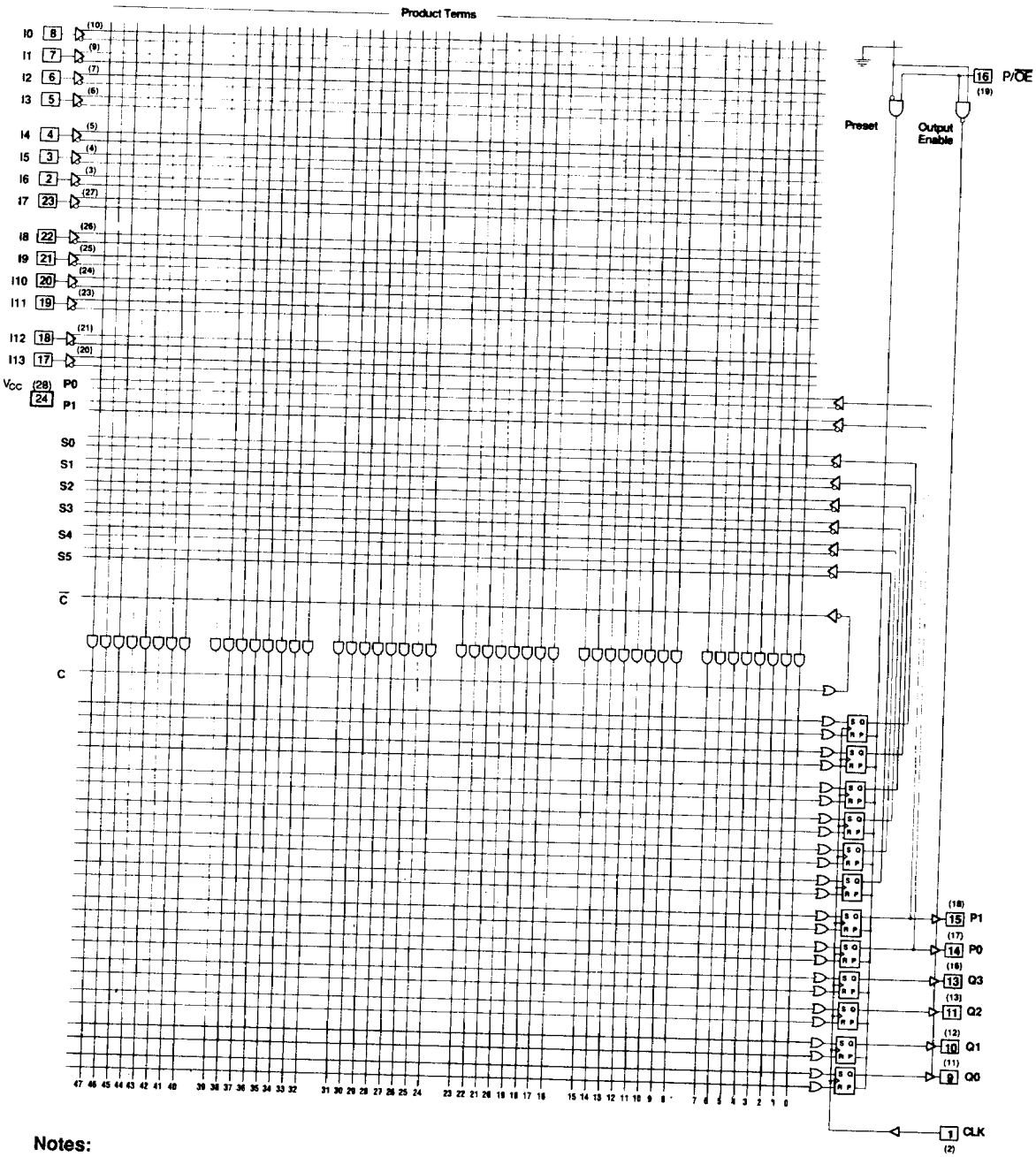
On the PLSCE167/8, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during an erase cycle. The security bit also prevents preload and observability.

Programming and Erasing

The PLS167/8 can be programmed on standard logic programmers. Approved programmers are listed in the Programmer Reference Guide.

The PLSCE167/8 may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

PLS167 LOGIC DIAGRAM
DIP (PLCC) Pinout



Notes:

1. All disconnected AND gate inputs float to a logic "1."
2. All disconnected OR gate inputs float to a logic "0."

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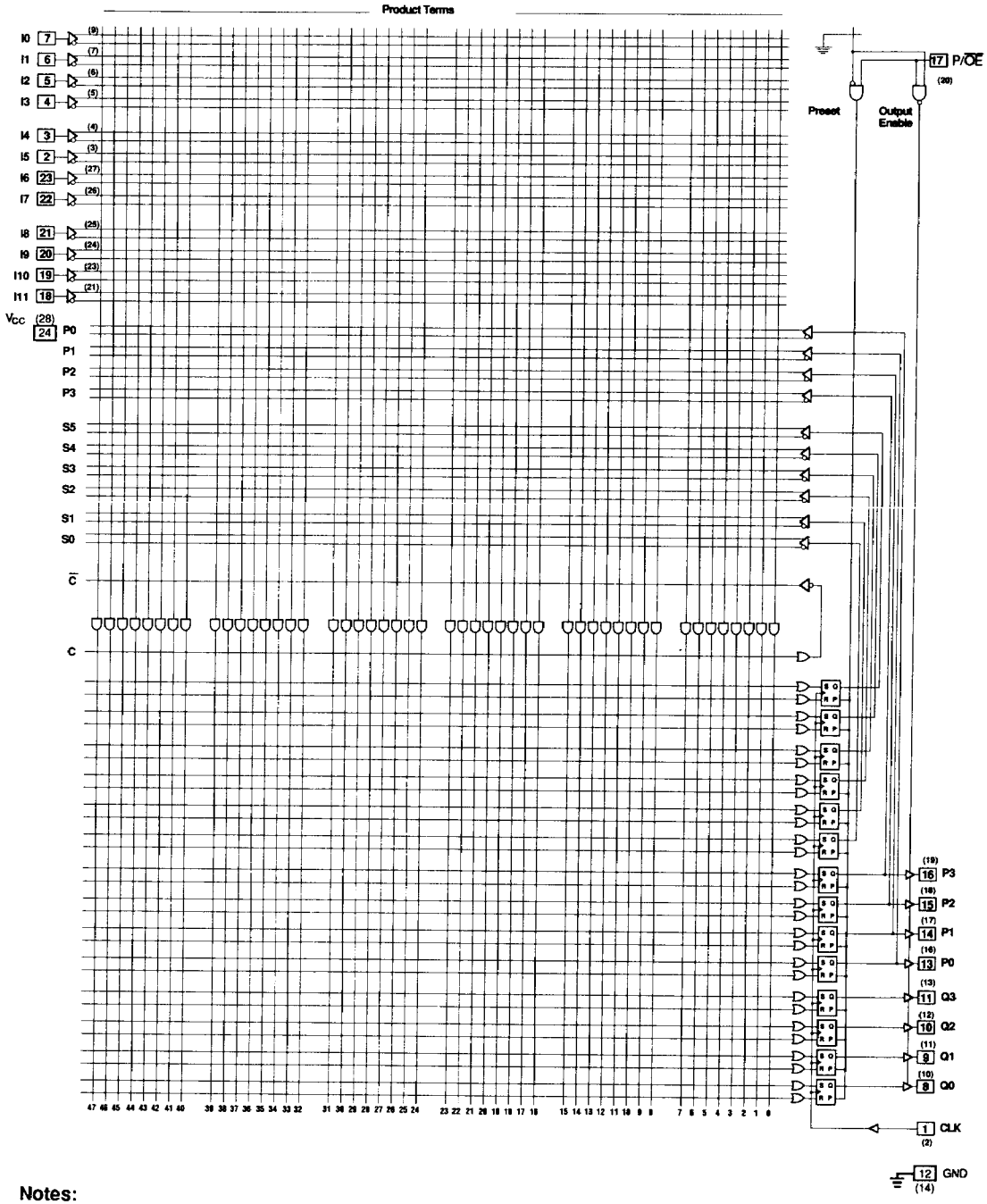
PLS168 LOGIC DIAGRAM
DIP (PLCC) Pinout



Notes:

1. All disconnected AND gate inputs float to a logic "1."
2. All disconnected OR gate inputs float to a logic "0."

14081-007A

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +5.5 V
DC Output or I/O Pin Voltage	–0.5 V to +5.5 V
DC Output Current	+16 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL} V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0	5.5	V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
V_I	Input Clamp Voltage	I_{IN} = –18 mA, V_{CC} = Min.		–1.2	V
I_{IH}	Input HIGH Current	V_{IN} = 2.4 V, V_{CC} = Max. (Note 2)		20	µA
I_{IL}	Input LOW Current	V_{IN} = 0.4 V, V_{CC} = Max. (Note 2)		–250	µA
I_I	Maximum Input Current	V_{IN} = 5.5 V, V_{CC} = Max.		25	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 2.7 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)		20	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0.4 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)		–20	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		160	mA

Notes:

1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = +25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_S	Setup Time from Input or Feedback to Clock		Without Complement Array		17		ns
t_{SC}	Setup Time from Input or Feedback to Clock		With Complement Array		30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output or Feedback					13	ns
t_{AP}	Asynchronous Preset to Output					15	ns
t_{APW}	Asynchronous Preset Width				10		ns
t_{APR}	Asynchronous Preset Recovery Time				8		ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 3)	External Feedback	Without Complement Array	1/(ts + tco)	33		MHz
f_{MAXC}		External Feedback	With Complement Array	1/(tsc + tco)	23		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					12	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	–0.5 V to +7.0 V
DC Output or I/O Pin Voltage	–0.5 V to +7.0 V
Static Discharge Voltage	2001 V
Latchup Current (T_A = 0°C to +75°C)	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air	0°C to +75°C
Supply Voltage (V_{CC}) with Respect to Ground	+4.75 V to +5.25 V

Operating Ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –3.2 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 24 mA V_{IN} = V_{IH} or V_{IL}, V_{CC} = Min.		0.5	V
V_{IH}	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
V_{IL}	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
I_{IH}	Input HIGH Leakage Current	V_{IN} = 5.25 V, V_{CC} = Max. (Note 2)		10	µA
I_{IL}	Input LOW Leakage Current	V_{IN} = 0 V, V_{CC} = Max. (Note 2)		–10	µA
I_{OZH}	Off-State Output Leakage Current HIGH	V_{OUT} = 5.25 V, V_{CC} = Max., V_{IN} = V_{IL} or V_{IH} (Note 2)		10	µA
I_{OZL}	Off-State Output Leakage Current LOW	V_{OUT} = 0 V, V_{CC} = Max. V_{IN} = V_{IL} or V_{IH} (Note 2)		–10	µA
I_{SC}	Output Short-Circuit Current	V_{OUT} = 0.5 V, V_{CC} = Max. (Note 3)	–30	–130	mA
I_{CC}	Supply Current	V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) V_{CC} = Max.		100	mA

Notes:

1. These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
3. Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. V_{OUT} = 0.5V has been chosen to avoid test problems caused by tester ground degradation.

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C_{IN}	Input Capacitance	V_{IN} = 2.0 V	V_{CC} = 5.0 V, T_A = 25°C, f = 1 MHz	5	pF
C_{OUT}	Output Capacitance	V_{OUT} = 2.0 V		8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

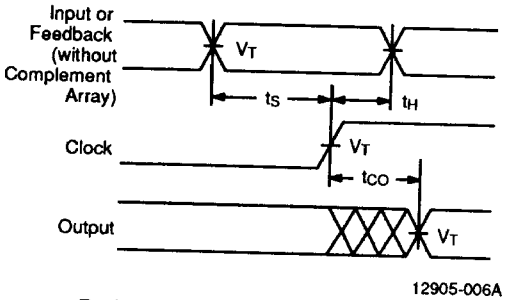
SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description				Min.	Max.	Unit
t_S	Setup Time from Input or Feedback to Clock		Without Complement Array		17		ns
t_{SC}	Setup Time from Input or Feedback to Clock		With Complement Array		30		ns
t_H	Hold Time				0		ns
t_{CO}	Clock to Output					13	ns
t_{CF}	Clock to Feedback (Note 3)					10	ns
t_{AP}	Asynchronous Preset to Output					15	ns
t_{APW}	Asynchronous Preset Width				10		ns
t_{APR}	Asynchronous Preset Recovery Time				8		ns
t_{WL}	Clock Width	LOW			10		ns
t_{WH}		HIGH			10		ns
f_{MAX}	Maximum Frequency (Note 4)	External Feedback	Without Complement Array	$1/(t_S + t_{CO})$	33		MHz
		Internal Feedback		$1/(t_S + t_{CF})$	37		MHz
f_{MAXC}		External Feedback	With Complement Array	$1/(t_{SC} + t_{CO})$	23		MHz
		Internal Feedback		$1/(t_{SC} + t_{CF})$	25		MHz
t_{PZX}	$\overline{OE}$ to Output Enable					12	ns
t_{PXZ}	$\overline{OE}$ to Output Disable					10	ns

Notes:

2. See Switching Test Circuit for test conditions.
3. Calculated from measured f_{MAX} internal.
4. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

SWITCHING WAVEFORMS



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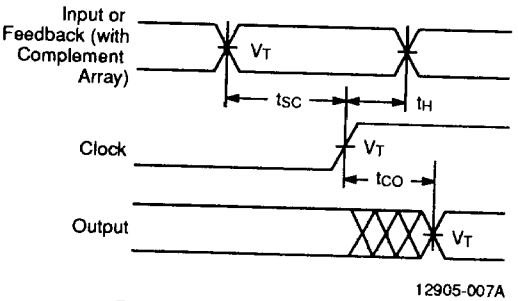
Registered Output (without Complement Array)



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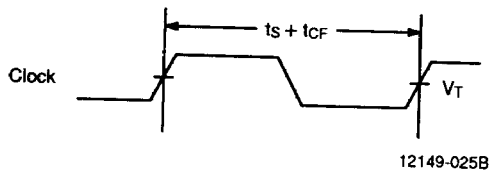
Registered Output (with Complement Array)



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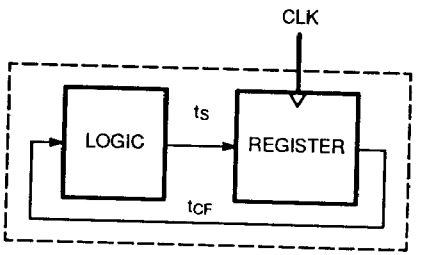
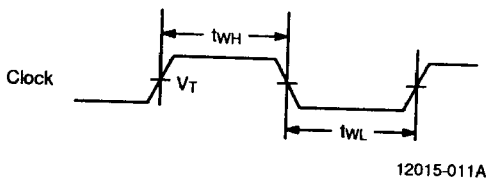
Clock to Feedback (f_{MAX} Internal)
See Path at Right

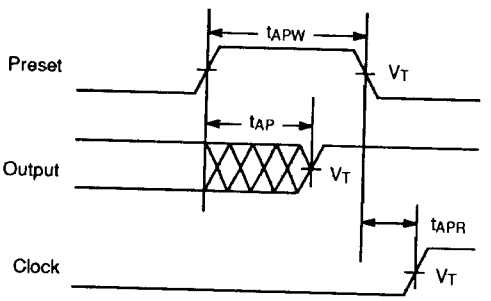


12015-021A



12015-011A

Clock Width



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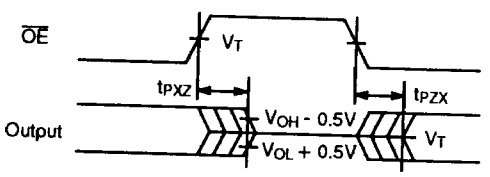
Asynchronous Preset



12905-008A

$\overline{OE}$ to Output Disable/Enable

Notes:

1. V_T = 1.5 V
2. Input pulse amplitude 0 V to 3.0 V.
3. Input rise and fall times 2–5 ns typical.

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

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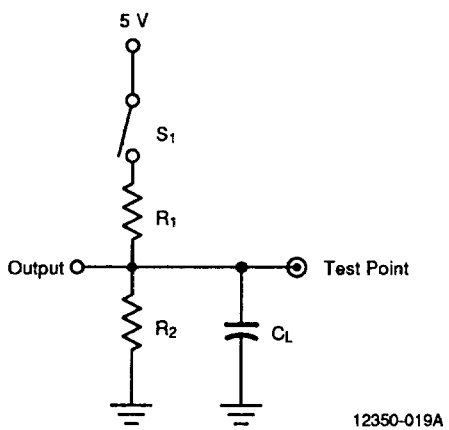
SWITCHING TEST CIRCUIT



12350-019A

Specification	S_1	C_L	R_1	R_2	Measured Output Value
t_{CO}, t_{CF}	Closed	50 pF	200 Ω	390 Ω	1.5 V
t_{PZX}	Z → H: Open Z → L: Closed				1.5 V
t_{PXZ}	H → Z: Open L → Z: Closed	5 pF			H → Z: V_{OH} −0.5 V L → Z: V_{OL} +0.5 V

ENDURANCE CHARACTERISTICS

The PLSCE167/8 is manufactured using AMD's advanced electrically erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed – a feature which allows 100% testing at the factory.

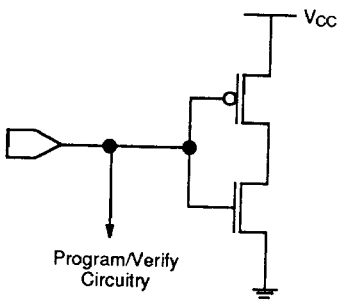
Endurance Characteristics

Symbol	Parameter	Min.	Units	Test Conditions
t_{DR}	Min. Pattern Data Retention Time	10	Years	Max. Storage Temperature
		20	Years	Max. Operating Temperature (125°C)
N	Min. Reprogramming Cycles	100	Cycles	Normal Programming Conditions

INPUT/OUTPUT EQUIVALENT SCHEMATICS

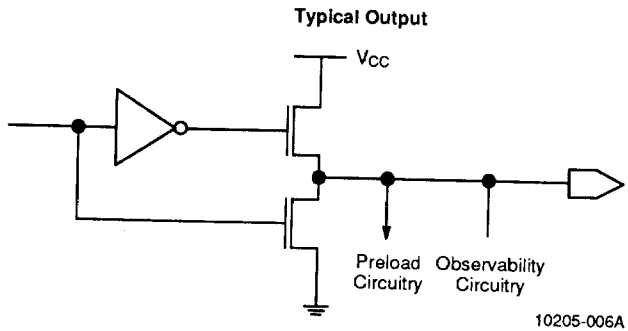
CMOS

Typical Input



10205-012A

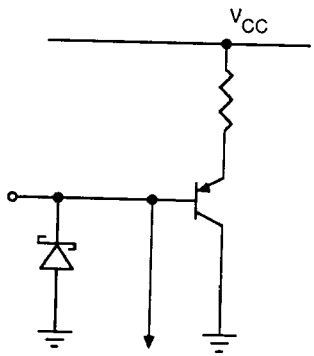
Typical Output



10205-006A

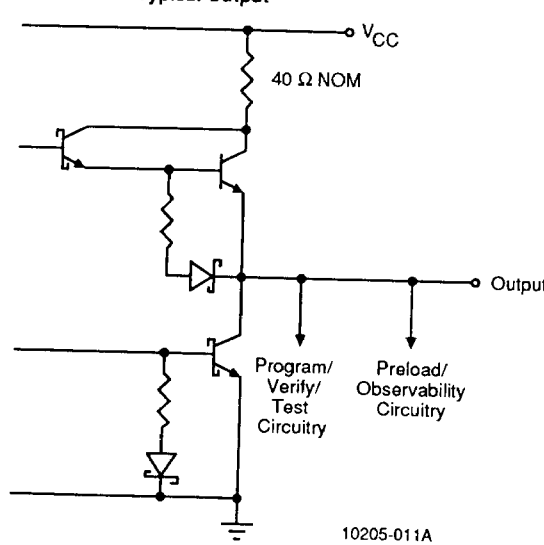
BIPOLAR

Typical Input



10205-010A

Typical Output



10205-011A

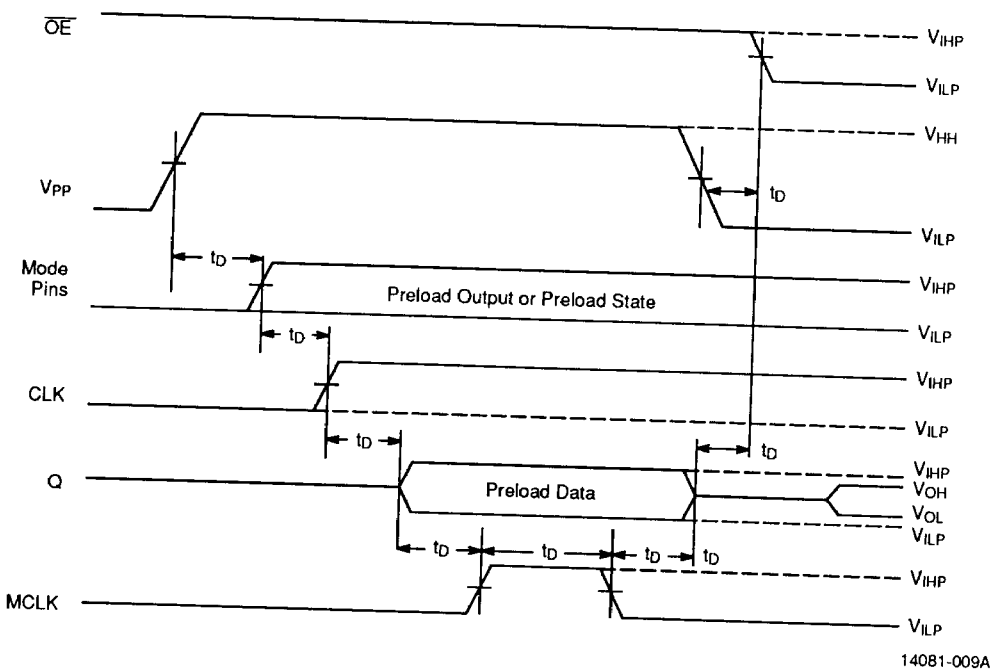
OUTPUT REGISTER PRELOAD (CMOS Only)

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

1. Set $\overline{OE}$ to V_{IHP} to disable outputs.
2. With Mode pins LOW raise V_{PP} to V_{HH}.
3. Use Mode pins to select Preload Output or Preload State.
4. Raise CLK to V_{IHP}.
5. Apply either V_{IHP} or V_{ILP} to all outputs. Use V_{IHP} to preload a LOW in the flip-flop; use V_{ILP} to preload a HIGH in the flop-flop.
6. Pulse MCLK from V_{ILP} to V_{IHP} to V_{ILP}.
7. Remove preload data from outputs.
8. Lower V_{PP} to V_{ILP}.
9. Lower $\overline{OE}$ to V_{ILP} to enable the outputs.
10. Verify V_{OL}/V_{OH} at all outputs. To verify state registers, use the observability mode.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	13.25	13.5	13.75	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	4.0	5.0	$V_{CC}+1$	V
t_D	Delay time	1			µs
dV_r/dt	V_{HH} Rise Time Slew Rate	10		100	V/µs
dV_f/dt	V_{HH} Fall Time Slew Rate		2.0	3.0	V/µs

Mode Select Pins			
MD_0	MD_1	MD_2	MD_3
0	1	1	0
1	1	1	0



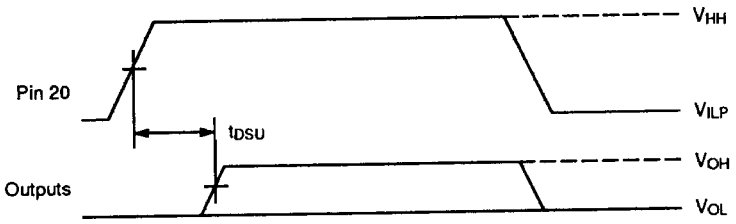
Output Register Preload Waveform

OBSERVABILITY (Bipolar Only)

The observability function allows the state register to be sent to the output pins. This feature aids functional testing of sequential designs by allowing direct observation of the buried state register. The procedure for observability follows.

1. Apply V_{HH} to pin 20.
2. Observe S_0–S_5 on pins Q_0–Q_3, P_0–P_1 (167) or Q_2–Q_3, P_0–P_3 (168).

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{HH}	Super-level input voltage	11.5	12	12.5	V
t_{DSU}	Delay time	250			ns



14081-010A

Observability Waveforms

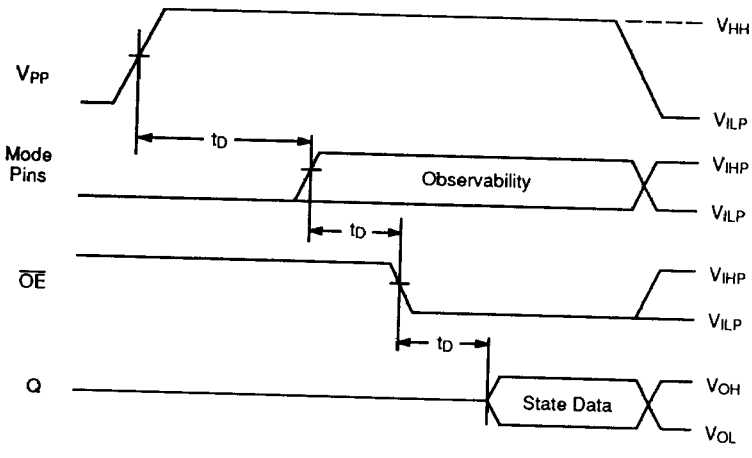
3

OBSERVABILITY (CMOS Only)

The observability function allows the state register to be sent to the output pins. This feature aids functional testing of sequential designs by allowing direct observation of the buried state register. The procedure for observability follows.

1. Set $\overline{OE}$ to V_{IHP} to disable outputs.
2. With Mode pins LOW raise V_{PP} to V_{HH}.
3. Use Mode pins to select Observability.
4. Lower $\overline{OE}$ to V_{ILP} to enable the state data to the outputs.
5. Lower V_{PP} to V_{ILP}.

Mode Select Pins			
MD_0	MD_1	MD_2	MD_3
0	0	0	1



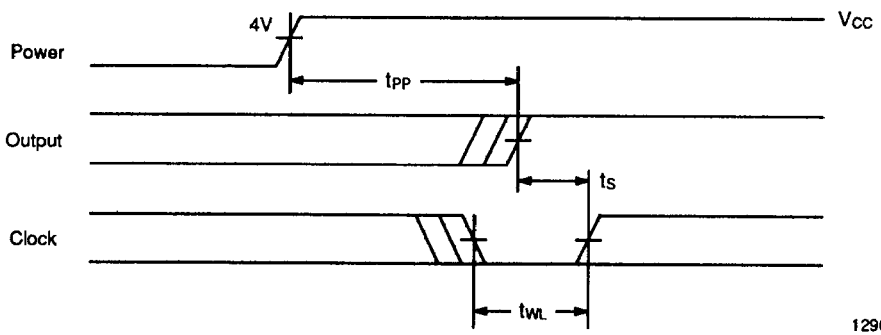
Observability Waveforms

POWER-UP PRESET

The power-up preset feature ensures that all flip-flops will be preset to HIGH after the device has been powered up. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up preset and the wide range of ways V_{CC} can rise to its steady state, two conditions are required to ensure a valid power-up preset. These conditions are:

1. The V_{CC} rise must be monotonic.
2. Following preset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
t_{PP}	Power-up Preset Time	1000	ns
t_S	Input or Feedback Setup Time	See Switching Characteristics	
t_{WL}	Clock Width LOW		



Power-Up Preset Waveform

1. Raise V_{CC} to 5.0 V ± 0.5 V.
2. Raise pin 19 to V_{IHH}.
3. Disable output pins by raising P/$\overline{OE}$ pin to V_{IHP}.
4. Apply V_{IHP}/V_{ILP} as desired to all output pins.
7. Enable output pins by lowering P/$\overline{OE}$ pin to V_{ILP}.
8. Lower pin 19 to V_{ILP}.

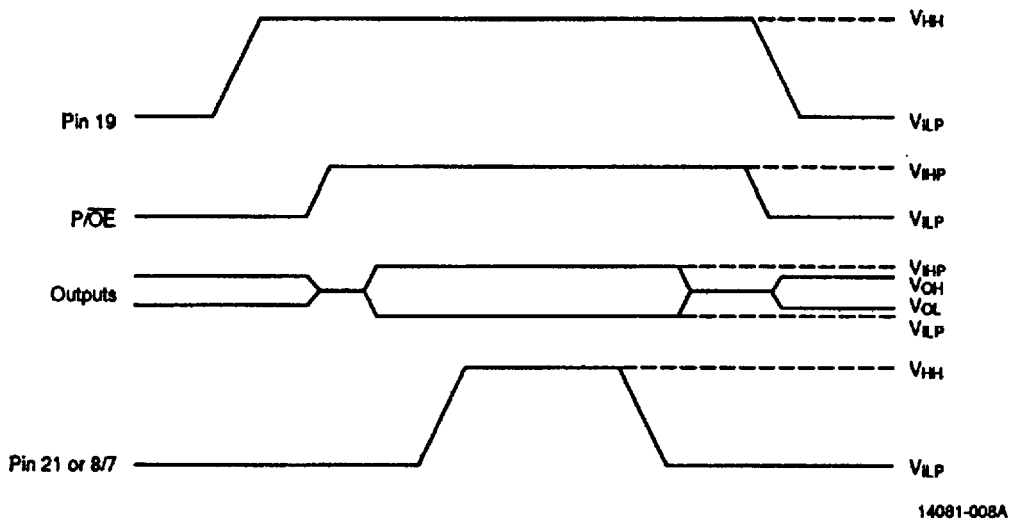
Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
V_{IHH}	Super-level input voltage	11.5	12	12.5	V
V_{ILP}	Low-level input voltage	0	0	0.5	V
V_{IHP}	High-level input voltage	2.4	5.0	5.5	V
t_D	Delay time	1			µs
dV_r/dt	V_{IHH} Rise Time Slew Rate	10		100	V/µs
dV_f/dt	V_{IHH} Fall Time Slew Rate		2.0	3.0	V/µs

PLS167

Preload Data	Pulse	Preloaded Register
Q_0–Q_3, P_0–P_1		
D_0–D_5	Pin 21	Q_0–Q_3, P_0–P_1
D_0–D_5	Pin 8	S_0–S_5

PLS168

Preload Data	Pulse	Preloaded Register
Q_0–Q_3, P_0–P_3		
D_0–D_7	Pin 21	Q_0–Q_3, P_0–P_3
X, X, D_2–D_7	Pin 7	S_0–S_5



14081-008A

Output Register Preload Waveform