

April 1997

16 x 16-Bit CMOS Parallel Multiplier

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- 16 x 16-Bit Parallel Multiplier with Full 32-Bit Product
- High-Speed (45ns) Clocked Multiply Time
- Low Power CMOS Operation
 - $I_{CCSB} = 500\mu A$ Maximum
 - $I_{CCOP} = 7.0mA$ Maximum at 1MHz
- HMU16/883 is Compatible with the AM29516, LMU16, IDT7216, and the CY7C516
- Supports Two's Complement, Unsigned Magnitude and Mixed Mode Multiplication
- TTL Compatible Inputs/Outputs
- Three-State Outputs

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HMU16GM-45/883	-55 to 125	68 Ld CPGA	N68.95
HMU16GM-60/883	-55 to 125	68 Ld CPGA	N68.95

Description

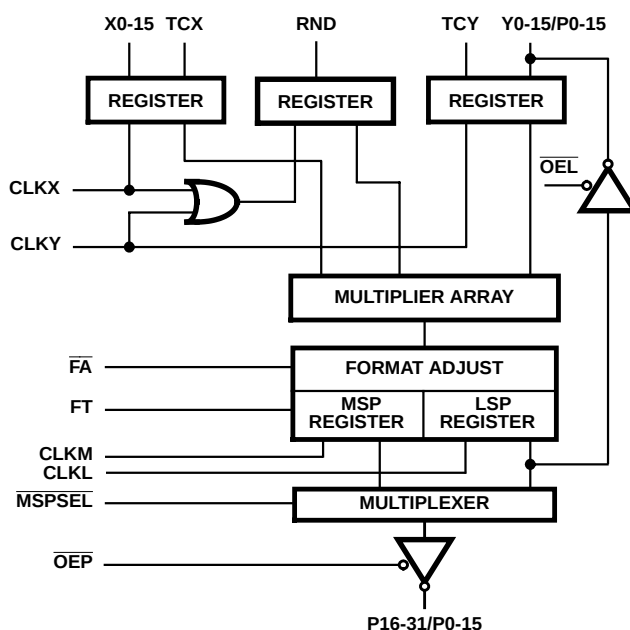
The HMU16/883 is a high speed, low power CMOS 16 x 16-bit parallel multiplier ideal for fast, real time digital signal processing applications. The 16-bit X and Y operands may be independently specified as either two's complement or unsigned magnitude format, thereby, allowing mixed mode multiplication operations.

Additional inputs are provided to accommodate format adjustment and rounding of the 32-bit product. The Format Adjust control allows the user to select a 31-bit product with the sign bit replicated in the LSP. The round control provides for rounding the most significant portion of the result by adding one to the most significant bit of the LSP.

Two 16-bit Output Registers (MSP and LSP) are provided to hold the most and least significant portions of the result, respectively. These registers may be made transparent for asynchronous operation through the use of the Feedthrough Control (FT). The two halves of the product may be routed to a single 16-bit three-state output port via the output multiplexer control, and in addition, the LSP is connected to the Y-input port through a separate three-state buffer.

The HMU16/883 utilizes independent clock signals (CLKX, CLKY, CLKL, CLKM) to latch the input operands and output Product Registers. This configuration maximizes throughput and simplifies bus interfacing. All outputs of the HMU16/883 also offer three-state control for multiplexing onto multi-use system busses.

Functional Diagram



Absolute Maximum Ratings

Supply Voltage +8.0V
 Input or Output Voltage Applied GND -0.5V to $V_{CC} + 0.5V$
 ESD Classification Class 1

Operating Conditions

Voltage Range +4.5V to +5.5V
 Temperature Range -55°C to 125°C

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (°C/W) θ_{JC} (°C/W)
 CPGA Package 42.69 10.0
 Maximum Junction Temperature 175°C
 Maximum Storage Temperature Range -65°C to 150°C
 Maximum Lead Temperature (Soldering 10s) 300°C

Die Characteristics

Gate Count 4500 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

TABLE 1. HMU16/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	TEST CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	$V_{CC} = 5.5V$	1, 2, 3	$-55 \leq T_A \leq 125$	2.2	-	V
Logical Zero Input Voltage	V_{IL}	$V_{CC} = 4.5V$	1, 2, 3	$-55 \leq T_A \leq 125$	-	0.8	V
Output HIGH Voltage	V_{OH}	$I_{OH} = -400\mu A$ $V_{CC} = 4.5V$ (Note 2)	1, 2, 3	$-55 \leq T_A \leq 125$	2.6	-	V
Output LOW Voltage	V_{OL}	$I_{OL} = +4.0mA$ $V_{CC} = 4.5V$ (Note 2)	1, 2, 3	$-55 \leq T_A \leq 125$	-	0.4	V
Input Leakage Current	I_I	$V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$	1, 2, 3	$-55 \leq T_A \leq 125$	-10	+10	mA
Output or I/O Leakage Current	I_O	$V_{OUT} = V_{CC}$ or GND $V_{CC} = 5.5V$	1, 2, 3	$-55 \leq T_A \leq 125$	-10	+10	mA
Standby Power Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$ or GND, $V_{CC} = 5.5V$, Outputs Open	1, 2, 3	$-55 \leq T_A \leq 125$	-	500	mA
Operating Power Supply Current	I_{CCOP}	$f = 1.0MHz$, $V_{IN} = V_{CC}$ or GND $V_{CC} = 5.5V$ (Note 3)	1, 2, 3	$-55 \leq T_A \leq 125$	-	7.0	mA
Functional Test	FT	(Note 4)	7, 8	$-55 \leq T_A \leq 125$	-	-	

NOTES:

2. Interchanging of force and sense conditions is permitted.
3. Operating supply current is proportional to frequency, typical rating is 5mA/MHz.
4. Tested as follows: $f = 1MHz$, V_{IH} (clock inputs) = 3.0, V_{IH} (all other inputs) = 2.6, $V_{IL} = 0.4$, $V_{OH} \geq 1.5V$, and $V_{OL} \leq 1.5V$.

TABLE 2. HMU16/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 5) TEST CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE (°C)	-45		-60		UNITS
					MIN	MAX	MIN	MAX	
Unclocked Multiply Time	t_{MUC}		9, 10, 11	$-55 \leq T_A \leq 125$	-	70	-	90	ns
Clocked Multiply Time	t_{MC}		9, 10, 11	$-55 \leq T_A \leq 125$	-	45	-	60	ns
X, Y, RND Setup Time	t_S		9, 10, 11	$-55 \leq T_A \leq 125$	18	-	20	-	ns
Clock HIGH Pulse Width	t_{PWH}		9, 10, 11	$-55 \leq T_A \leq 125$	15	-	20	-	ns
Clock LOW Pulse Width	t_{PWL}		9, 10, 11	$-55 \leq T_A \leq 125$	15	-	20	-	ns
MSPSEL to Product Out	t_{PDSEL}		9, 10, 11	$-55 \leq T_A \leq 125$	-	25	-	30	ns
Output Clock to P	t_{PDP}		9, 10, 11	$-55 \leq T_A \leq 125$	-	25	-	30	ns
Output Clock to Y	t_{PDY}		9, 10, 11	$-55 \leq T_A \leq 125$	-	25	-	30	ns
Three-State Enable Time	t_{ENA}	(Note 6)	9, 10, 11	$-55 \leq T_A \leq 125$	-	25	-	30	ns
Clock Low Hold Time CLKXY Relative to CLKML	t_{HCL}	(Note 7)	9, 10, 11	$-55 \leq T_A \leq 125$	0	-	0	-	ns

NOTES:

- AC Testing as follows: $V_{CC} = 4.5V$ and $5.5V$. Input levels $0V$ and $3.0V$; timing reference levels = $1.5V$; output load per test load circuit, with $V_1 = 4V$, $R_1 = 500\Omega$ and $C_L = 40pF$.
- Transition is measured at $\pm 200mV$ from steady state voltage; output loading per test load circuit with $V_1 = 1.5V$, $R_1 = 500\Omega$ and $C_L = 40pF$.
- To ensure the correct product is entered in the Output Registers; new data may not be entered into the Input Registers before the Output Registers have been clocked.

TABLE 3. HMU16/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTES	TEMPERATURE (°C)	-45		-60		UNITS
					MIN	MAX	MIN	MAX	
Input Capacitance	C _{IN}	V _{CC} = Open, f = 1MHz All Measurements are referenced to device GND.	1	T _A = 25	-	15	-	15	pF
Output Capacitance	C _{OUT}		1	T _A = 25	-	10	-	10	pF
I/O Capacitance	C _{I/O}		1	T _A = 25	-	10	-	10	pF
X, Y, RND Hold Time	t _H		1, 2	-55 ≤ T _A ≤ 125	3	-	3	-	ns
Three-State Disable Time	t _{DIS}		1, 2, 3	-55 ≤ T _A ≤ 125	-	25	-	30	ns
Output Rise Time	t _r	From 0.8V to 2.0V	1, 2, 4	-55 ≤ T _A ≤ 125	-	10	-	10	ns
Output Fall Time	t _f	From 2.0V to 0.8V	1, 2, 4	-55 ≤ T _A ≤ 125	-	10	-	10	ns

NOTES:

8. The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major process and/or design changes.
9. Guaranteed, but not 100% tested.
10. Transition is measured at 1200mV from steady state voltage; output loading per test load circuit with V₁ = 1.5V, R₁ = 500Ω and C_L = 40pF.
11. Loading is as specified in the test load circuit, with V₁ = 2.4V, R₁ = 500Ω and C_L = 40pF.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	-
PDA	100%	1
Final Test	100%	2, 3, 8A, 8B, 10, 11
Group A	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C and D	Samples/5005	1, 7, 9

Burn-In Circuit

68 LEAD CPGA
TOP VIEW

11		N/C	X13	X15	RND	TCY	V _{CC}	GND	FT	$\overline{OE\overline{P}}$	
10	X11	X12	X14	CLKX	TCX	V _{CC}	GND	$\overline{MSP}$ SEL	$\overline{FA}$	CLKM	N/C
9	X9	X10								P30/ P14	P31/ P15
8	X7	X8								P28/ P12	P29/ P13
7	X5	X6								P26/ P10	P27/ P11
6	X3	X4								P24/P8	P25/P9
5	X1	X2								P22/P6	P23/P7
4	$\overline{OE\overline{L}}$	X0								P20/P4	P21/P5
3	CLKY	CLKL								P18/P2	P19/P3
2	N/C	Y0/P0	Y2/P2	Y4/P4	Y6/P6	Y8/P8	Y10/ P10	Y12/ P12	Y14/ P14	P16/P0	P17/P1
1		Y1/P1	Y3/P3	Y5/P5	Y7/P7	Y9/P9	Y11/ P11	Y13/ P13	Y15/ P15	N/C	
	A	B	C	D	E	F	G	H	J	K	L

CPGA PIN	PIN NAME	BURN-IN SIGNAL
B6	X4	F6
A6	X3	F5
B5	X2	F4
A5	X1	F3
B4	X0	F2
A4	$\overline{OE\overline{L}}$	V _{CC}
B3	CLKL	F0
A3	CLKY	F0
B2	Y0/P0	F2
B1	Y1/P1	F3
C2	Y2/P2	F4
C1	Y3/P3	F5
D2	Y4/P4	F6
D1	Y5/P5	F7
E2	Y6/P6	F8
E1	Y7/P7	F9
F2	Y8/P8	F10
F1	Y9/P9	F11
G2	Y10/P10	F12

CPGA PIN	PIN NAME	BURN-IN SIGNAL
G1	Y11/P11	F13
H2	Y12/P12	F14
H1	Y13/P13	F15
J2	Y14/P14	F4
J1	Y15/P15	F5
K2	P0/P16	V _{CC} /2
L2	P1/P17	V _{CC} /2
K3	P2/P18	V _{CC} /2
L3	P3/P19	V _{CC} /2
K4	P4/P20	V _{CC} /2
L4	P5/P21	V _{CC} /2
K5	P6/P22	V _{CC} /2
L5	P7/P23	V _{CC} /2
K6	P8/P24	V _{CC} /2
L6	P9/P25	V _{CC} /2
K7	P10/P26	V _{CC} /2
L7	P11/P27	V _{CC} /2
K8	P12/P28	V _{CC} /2
L8	P13/P29	V _{CC} /2

CPGA PIN	PIN NAME	BURN-IN SIGNAL
K9	P14/P30	$V_{CC}/2$
L9	P15/P31	$V_{CC}/2$
K10	CLKM	F0
K11	$\overline{OE}$	F1
J10	$\overline{FA}$	F14
J11	FT	F15
H10	$\overline{MSPSEL}$	F14
H11	GND	GND
G10	GND	GND
G11	V_{CC}	V_{CC}
F10	V_{CC}	V_{CC}
F11	TCY	F15
E10	TCX	F15
E11	RND	F1
D10	CLKX	F0
D11	X15	F3
C10	X14	F2
C11	X13	F15
B10	X12	F14
A10	X11	F13
B9	X10	F12
A9	X9	F11
B8	X8	F10
A8	X7	F9
B7	X6	F8
A7	X5	F7
A2	N.C.	NONE
K1	N.C.	NONE
L10	N.C.	NONE
B11	N.C.	NONE

NOTES:

12. $V_{CC} = 5.5V + 0.5V/-0.0V$ with $0.1\mu F$ decoupling capacitor to GND.
13. $F0 = 100kHz$, $F1 = F0/2$, $F2 = F1/2$,
14. $V_{IH} = V_{CC} - 1V \pm 0.5V$ (Min), $V_{IL} = 0.8V$ (Max).
15. $47k\Omega$ Load Resistors used on all pins except V_{CC} and GND (Pin-Grid identifiers F10, G10, G11 and H11).

Die Characteristics

DIE DIMENSIONS:

179 x 169 x 19 ± 1mils

METALLIZATION:

Type: Si - Al or Si-Al-Cu

Thickness: 8kÅ

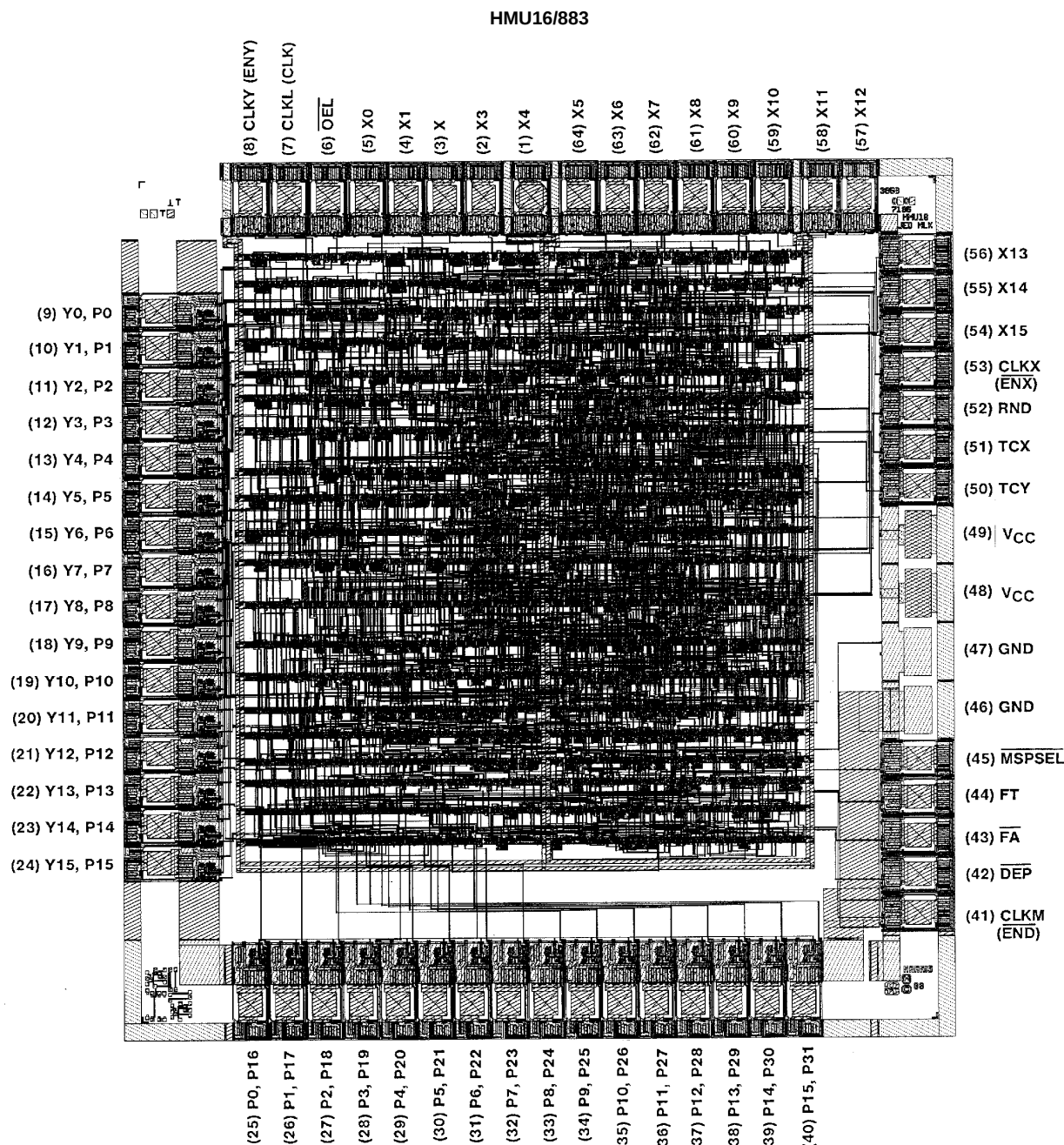
GLASSIVATION:

Type: Nitrox

Thickness: 10kÅ

WORST CASE CURRENT DENSITY: $1.2 \times 10^5 \text{A/cm}^2$

Metallization Mask Layout



All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site <http://www.intersil.com>