SPICE Model Tutorial of the RSLIC18™ AC Loop

Application Note | October 1998 | AN9824

The AC loop of the RSLIC18 refers to the voice band path which provides full duplex signal communication and impedance synthesis. The circuit operation is described here in as well as the macromodel used to simulate the AC performance of the device. The architecture is the same for all part numbers available in the RSLIC18 family of ringing subscriber line interface circuits.

The information in this document applies to all part numbers of the RSLIC18 family: HC55180, HC55181, HC55182, HC55183 and HC55184.

Architectural Description

The complete AC response of the device is determined by a the dominant AC loop and a low frequency DC loop. The DC loop provides the loop current limit function and contributes to the AC characteristics below 400Hz. The operation of the DC loop will not be discussed in detail, however the effects of this loop are included in the macromodel.

Voltage Feed Current Sense

The AC loop is designed around a voltage feed current sense architecture. The AC loop current is sensed across a pair of low value resistors which are in series with the Tip and Ring amplifier outputs. These sense resistors are placed within the feedback loop of each amplifier, compensating for voltage loss. All internal resistors use ratio relationships providing superb matching, temperature stability and gain accuracies.

The voltage across each resistor is measured using a differential amplifier, referred to as the sense amplifier (SA). The sense amplifier is configured as a dual differential amplifier. The sense connections to the amplifier are “flipped” resulting in addition of metallic signals (AC voice and DC loop current) and cancellation of longitudinal currents.

The output of the sense amplifier drives an inverting amplifier referred to as the transmit amplifier (TA). The gain of the transmit amplifier is set by the external component RS, which sets the synthesized impedance for the device. The output of the transmit amplifier provides the 4-wire output of the device as well as the feedback required for impedance synthesis. The feedback signal for impedance matching is inverted with respect to the incoming voice signal at the receive input VRX.

The receiver represents a unity gain current summing node. The voice signal at the VRX input and the feedback signal at the VTX output each drive internal resistors. The currents formed by the respective voltages and resistors are summed by a high impedance current summing junction. The sum of the currents are mirrored and drive the inverting terminal of the Tip and Ring amplifiers. The mirrored output of the receiver sources Tip current and sinks Ring current, providing the differential 2-wire output for the device.

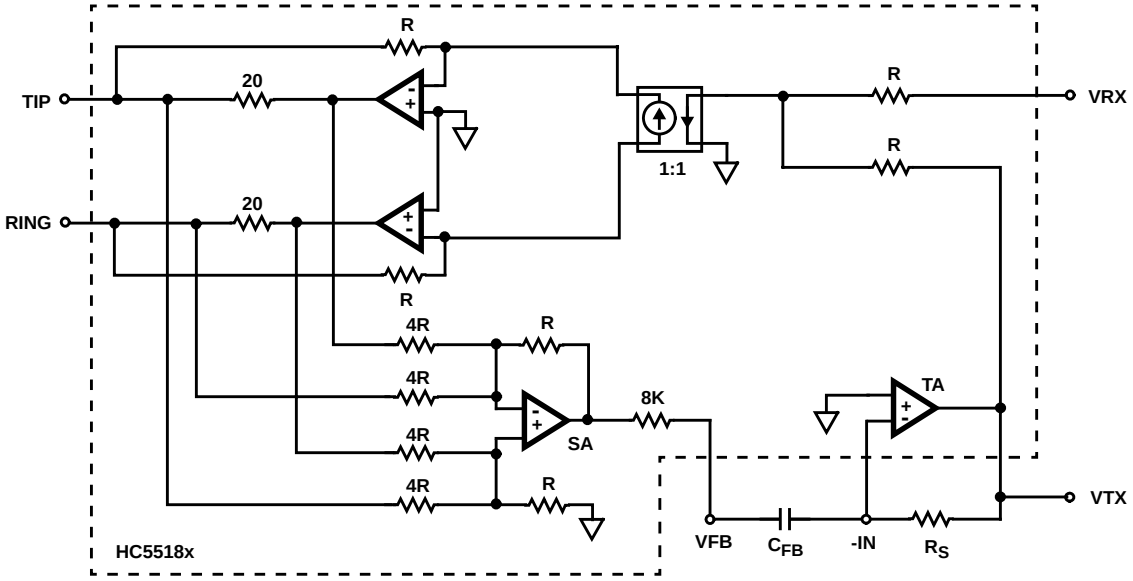

FIGURE 1. RSLIC18 AC SIGNAL TRANSMISSION SIGNAL PATH

Functional Description

The functional blocks of the AC loop are the receiver, tip and ring amplifiers, sense amplifier and transmit amplifier.

Receiver

The receiver provides the current summing node for the voice signals from the CODEC (VRX) and the impedance matching feedback (VTX). The current generated by each voltage signal and internal 200kΩ resistor is summed and mirrored to the Tip and Ring amplifier inverting inputs. Positive voltages at the receive input (VRX) will source current to the Tip amp and sink current from the Ring amp.

Tip and Ring Amplifiers

Both amplifiers are of voltage feedback design with a 200kΩ feedback resistor. The voltage and current relationships of the receiver to Tip and Ring amplifier outputs is shown in Figure 2.

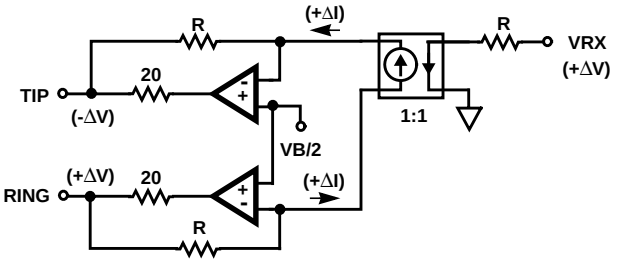

FIGURE 2. RECEIVE INTERFACE

The 20Ω resistors are the sense resistors which provide the loop current information to the sense amplifier. The sense resistor voltage drops are compensated by the feedback loop of each amplifier.

Sense Amplifier

The sense amplifier is configured as a 4 input differential amplifier with a voltage gain of 1/4. The differential input pairs are connected across the internal 20Ω sense resistors. Current flowing out of Tip and into Ring is the convention for positive loop current (I_L) flow. The sense connections across the sense resistors form an inverting relationship between the loop current flow and the output voltage of the sense amp. Figure 3 shows the sense amplifier with connections to the sense resistors.

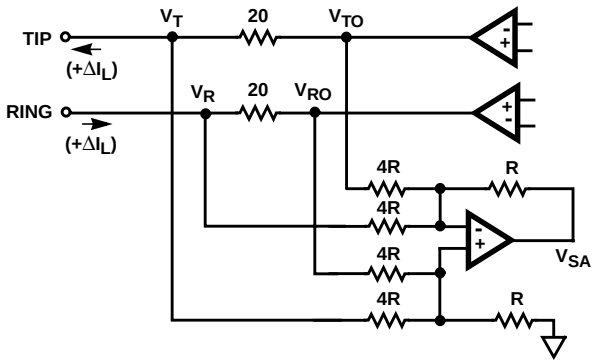

FIGURE 3. SENSE AMPLIFIER SENSING CONNECTIONS

The sense amplifier output voltage as a function of the Tip sense connections can be found by applying superposition to the circuit of Figure 3.

$$V_{SA(T)} = V_T\left(\frac{R \parallel 4R}{4R + R \parallel 4R}\right)\left(1 + \frac{R}{4R}\right) - V_{TO}\left(\frac{R}{4R}\right) \quad \text{(EQ. 1)}$$

Simplifying the terms in parenthesis leads to the Tip sense differential relationship of Equation 2.

$$V_{SA(T)} = \frac{1}{4}(V_T - V_{TO}) \quad \text{(EQ. 2)}$$

The voltage across the Tip sense resistor is the loop current multiplied by the sense resistor as shown in Equation 3.

$$V_{TO} - V_T = 20I_L \quad \text{(EQ. 3)}$$

The voltage at the Tip amplifier output (V_{TO}) is more positive than the Tip sense connection voltage (V_T) as defined by the loop current flow convention of Figure 3. Substituting the loop current term of Equation 3 into the sense amplifier output expression of Equation 2 yields:

$$V_{SA(T)} = \frac{1}{4}(V_T - V_{TO}) = \frac{1}{4}(-20I_L) = -5I_L \quad \text{(EQ. 4)}$$

Applying the same superposition analysis to the Ring sense connections results in the complete sense amplifier output expression of Equation 5.

$$V_{SA} = V_{SA(T)} + V_{SA(R)} = (-5I_L) + (-5I_L) = -10I_L \quad \text{(EQ. 5)}$$

The final step in defining the sense amplifier functionality is to express the loop current in terms of the load impedance. Since the loop from Tip to Ring represents a closed system the loop current out of Tip equals the loop current into Ring. Therefore the voltage across any impedance in the loop will provide the loop current information. The loop impedance between Tip and Ring (V_T and V_R) is the protection resistors ($2R_P$) and the load impedance (Z_L). Using this voltage and impedance relationship, the sense amplifier output voltage is rewritten as shown in Equation 6. The last term of Equation 6 represent the voltage gain relationship of the sense amp.

$$I_L = \frac{V_T - V_R}{Z_L + 2R_P} \Longrightarrow V_{SA} = (V_T - V_R)\frac{-10}{Z_L + 2R_P} \quad \text{(EQ. 6)}$$

Transmit Amplifier

The transmit amplifier is a voltage feedback design with the noninverting terminal referenced to ground. It amplifies the sense amplifier output to achieve impedance synthesis. The output equation for the transmit amplifier is provided below.

$$V_{TA} = V_{SA}\left(\frac{-R_S}{8000}\right) = V_{SA}\left(\frac{-400Z_O}{8000}\right) \quad \text{(EQ. 7)}$$

The term RS is the external resistor used to program the synthesized impedance of the device. The value of RS is equal to 400 x Z_O. In addition to impedance matching, the transmit amplifier drives the CODEC transmit interface.

SPICE Macromodel Analysis

The SPICE macromodel represents entire the AC loop of the device. Of the five functional blocks only the receiver is not modeled. The receiver does not contribute significantly to the device bandwidth and is modeled as an ideal current mirror. The four core amplifiers of the design are modeled by two or three pole circuits using voltage controlled voltage sources. Low frequency effects of the loop current limit function are included in the model but will not be discussed in detail. The SPICE net list included at the end of the document should be compatible with any SPICE compatible simulation software.

Model Diagram

The macromodel diagram of Figure 6 is very similar to the functional diagram of Figure 1. The only differences are the addition of the DC loop current limit function and generic blocks representing the amplifiers. The current mirror is modeled using a generic current controlled current source.

AMPLIFIER MODELS

The primary amplifier blocks of the architecture are the tip, ring, sense and transmit amplifiers. Each amplifier will be discussed separately followed by simulation examples using the model.

Tip Amplifier

The Tip amplifier is modeled with a three pole circuit. The open loop gain is 49740 or 94dB and the open loop 3dB bandwidth is 13Hz. An internal compensation capacitor of 5.2pF in parallel with the feedback resistor of 200kΩ forms a zero in the amplifier response at 153kHz. The model for the Tip amplifier is shown below. The non inverting input is indicated by (+), the inverting input by (-) and the output by (o).

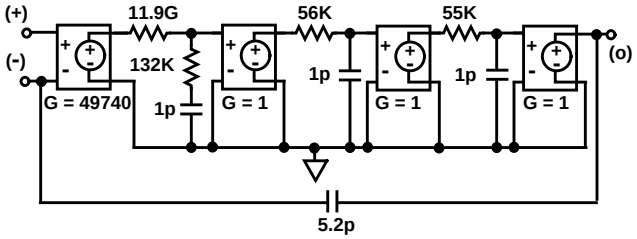

FIGURE 4. TIP AMPLIFIER 3-POLE MODEL

Ring Amplifier

The Ring amplifier is modeled with a three pole circuit. The open loop gain is 59420 or 95dB and the open loop 3dB bandwidth is 12Hz. An internal compensation capacitor of 8pF in parallel with the feedback resistor of 200kΩ forms a zero in the amplifier response at 100kHz. The model for the Ring amplifier is shown below. The non inverting input is indicated by (+), the inverting input by (-) and the output by (o).

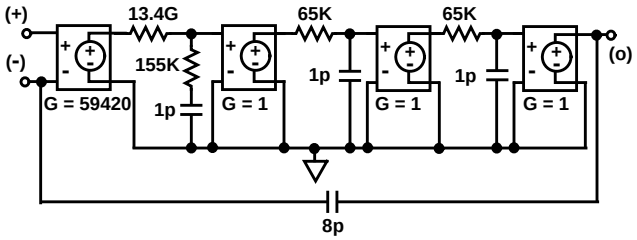

FIGURE 5. RING AMPLIFIER 3-POLE MODEL

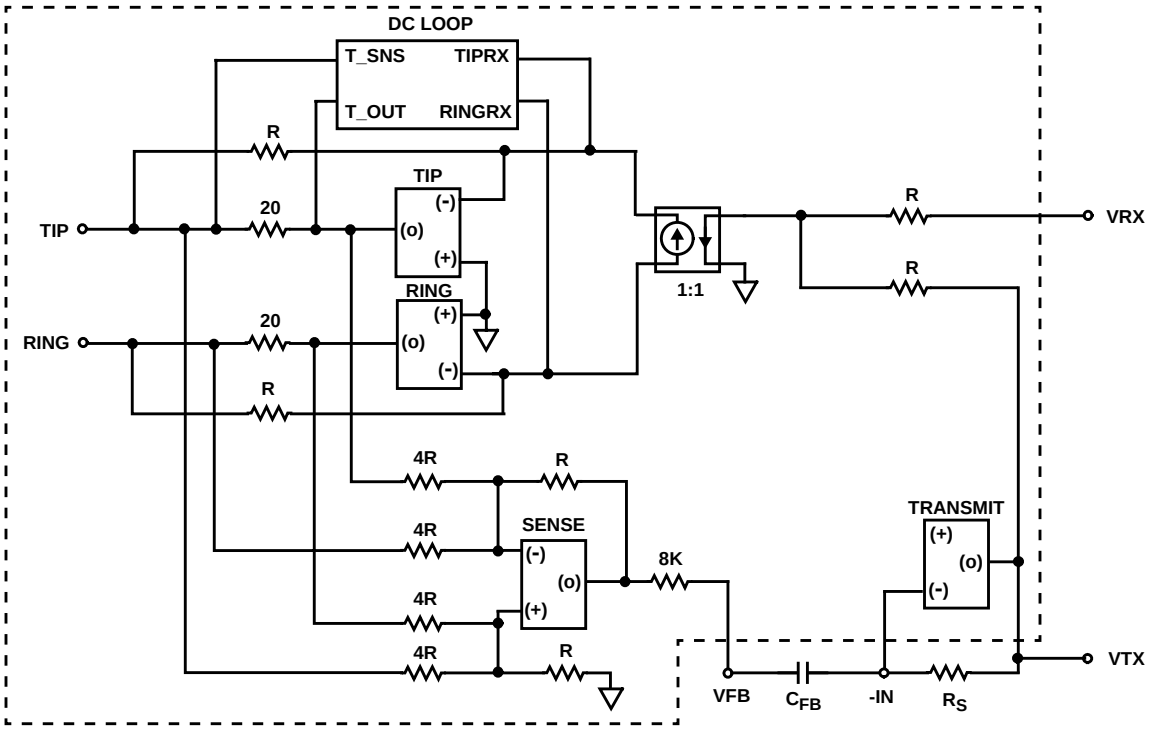

FIGURE 6. AC LOOP MACROMODEL DIAGRAM

Sense Amplifier

The Sense amplifier is modeled with a two pole circuit. The open loop gain is 4716 or 73dB and the open loop 3dB bandwidth is 260Hz. The model for the Sense amplifier is shown below. The non inverting input is indicated by (+), the inverting input by (-) and the output by (o).

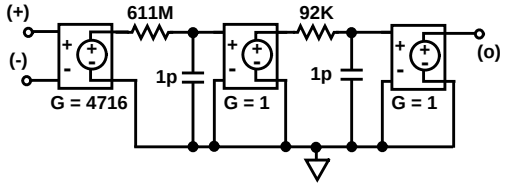

FIGURE 7. SENSE AMPLIFIER 2-POLE MODEL

Transmit Amplifier

The Transmit amplifier is modeled with a two pole circuit. The open loop gain is 4151 or 72dB and the open loop 3dB bandwidth is 127Hz. The model for the Transmit amplifier is shown below. The non inverting input is indicated by (+), the inverting input by (-) and the output by (o).

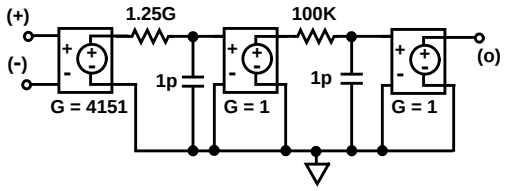

FIGURE 8. TRANSMIT AMPLIFIER 2-POLE MODEL

The gains and component values used in the models were matched to the actual device level simulations of each amplifier. Lab measurements may vary due to component tolerances and process variations.

Simulation Example - Resistive Load

Resistive matching is a misnomer, since the impedance being matched is in the voice band. However, resistive matching is the case when the device synthesizes an impedance to match a purely resistive load. This example will match the device to a 600Ω load impedance, which is the reference impedance for most North American telephony AC transmission specifications.

Device Impedance Synthesis

The device synthesized impedance (Z_O) is defined as the difference between the load impedance (Z_L) and the sum of the protection resistance (R_P).

$$Z_O = Z_L - 2R_P = 600\Omega - 2(35\Omega) = 530\Omega \quad \text{(EQ. 8)}$$

Typically the load impedance represents a combination of loop length and phone impedance, therefore a separate term for the loop length (ohms/foot) is not required.

The external resistor, R_S, which programs the synthesized impedance is calculated from the equation shown below.

$$R_S = 400 \times Z_O = 400 \times 530\Omega = 212k\Omega \quad \text{(EQ. 9)}$$

The resistor value used in the application circuit will be the standard component value nearest to the calculated value.

G_{42} Simulation

The G_{42} frequency response of the device is simulated using the circuit of Figure 9.

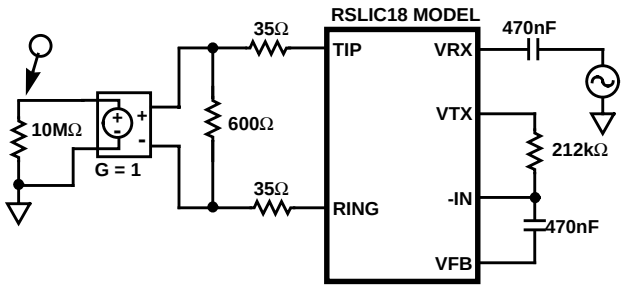

FIGURE 9. G_{42} RESISTIVE LOAD SIMULATION CIRCUIT

The VRX input of the model is driven by an AC voltage source. The differential voltage across the 600Ω load is converted to single ended by the voltage controlled voltage source with a gain of 1. A dB voltage probe was used to measure the magnitude and a phase voltage probe was used to measure the phase of the frequency response.

EXPECTED RESULTS

The G_{42} results are predicted using the voltage divider relationship shown below.

$$G_{42} = \frac{-2Z_L}{Z_L + 2R_P + Z_O} = \frac{-2(600)}{600 + 2(35) + 530} = -1 \quad \text{(EQ. 10)}$$

The magnitude of the frequency response in the voice band, 300Hz to 3400Hz, should be approximately 0dB and the phase should be nearly 180 degrees.

G_{24} Simulation

The G_{24} frequency response of the device is simulated using the circuit of Figure 10.

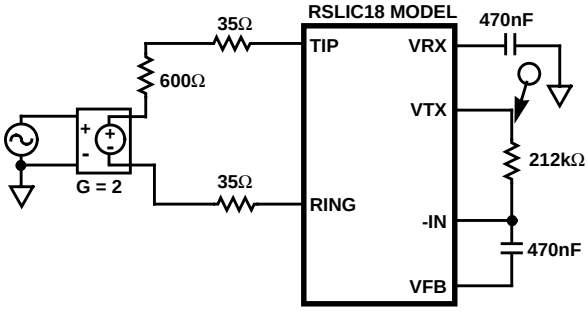

FIGURE 10. G_{24} RESISTIVE LOAD SIMULATION CIRCUIT

The voltage controlled voltage source converts the single ended AC voltage source to a differential driver for the 2-wire interface. The 4-wire output voltage is measured at the transmit output, VTX, of the device. A dB voltage probe was used to measure the magnitude and a phase voltage probe was used to measure the phase of the frequency response.

EXPECTED RESULTS

The G_{24} results are predicted using the voltage divider relationship shown below.

$$G_{24} = \frac{-Z_O}{Z_L + 2R_P + Z_O} = \frac{-530}{600 + 2(35) + 530} = -0.441 \quad \text{(EQ. 11)}$$

The magnitude of the frequency response in the voice band, 300Hz to 3400Hz, should be approximately -7.1dB and the phase should be nearly 180 degrees.

G_{44} Simulation

The G_{44} frequency response of the device is simulated using the circuit of Figure 11.

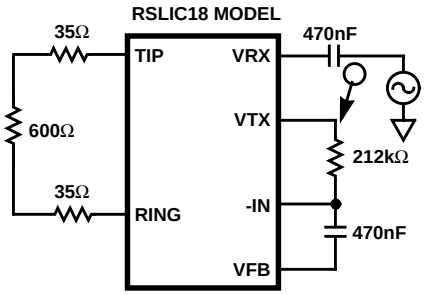

FIGURE 11. G_{44} RESISTIVE LOAD SIMULATION CIRCUIT

The VRX input of the mode is driven by an AC voltage source. The 4-wire output voltage is measured at the transmit output, VTX, of the device. A dB voltage probe was used to measure the magnitude and a phase voltage probe was used to measure the phase of the frequency response.

EXPECTED RESULTS

The G_{44} results are predicted using the voltage divider relationship shown below.

$$G_{44} = \frac{-Z_O}{Z_L + 2R_P + Z_O} = \frac{-530}{600 + 2(35) + 530} = -0.441 \quad \text{(EQ. 12)}$$

The magnitude of the frequency response in the voice band, 300Hz to 3400Hz, should be approximately -7.1dB and the phase should be nearly 180 degrees.

Simulation Example - Complex Load

Most international telephony transmission requirements are defined around a complex 2-wire impedance. The most widely recognized form of the complex network is shown below as well as the device synthesis network to match the impedance.

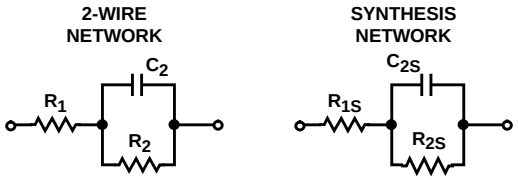

FIGURE 12. TYPICAL COMPLEX IMPEDANCE NETWORK

This simulation example will use the 2-wire complex network for China which is defined as $R_1 = 200\Omega$, $R_2 = 680\Omega$ and $C_2 = 100nF$.

Device Impedance Synthesis

When matching the device to a complex load the sum of the protection resistance is subtracted from the series resistor R_1. The other components remain unchanged. The general form of the design equation is shown below.

$$Z_O = Z_L - 2R_P = (R_1 + R_2 \| C_2) - 2(R_P) \quad \text{(EQ. 13)}$$

Substituting actual component values results in the complex network to be synthesized by the device.

$$Z_O = (200 + 680 \| 100n) - 2(35) = 130 + 680 \| 100n \quad \text{(EQ. 14)}$$

Typically the load impedance represents a combination of loop length and phone impedance, therefore a separate term for the loop length (ohms/foot) is not required.

The external resistor, R_S, which programs the synthesized impedance now takes the form of the complex network defined by R_{1S}, R_{2S} and C_{2S}.

$$R_{1S} = 400(R_1 - 2R_P) = 400(130) = 52k\Omega \quad \text{(EQ. 15)}$$

$$R_{2S} = 400(R_2) = 400(680) = 272k\Omega \quad \text{(EQ. 16)}$$

$$C_{2S} = \frac{C_2}{400} = \frac{100n}{400} = 250pF \quad \text{(EQ. 17)}$$

The resistor value used in the application circuit will be the standard component value nearest to the calculated value.

G_{42} Simulation

The G_{42} frequency response of the device can be simulated using the circuit of Figure 13.

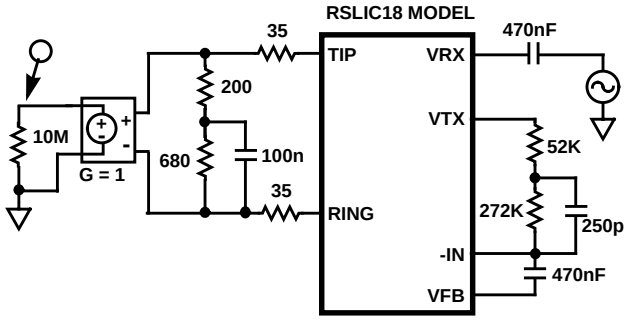

FIGURE 13. G_{42} COMPLEX LOAD SIMULATION CIRCUIT

EXPECTED RESULTS

Though slightly cumbersome, the voltage divider relationship also applies to the complex matching gain.

$$G_{42} = \frac{-2Z_L}{Z_L + 2R_P + Z_O} \quad \text{(EQ. 18)}$$

where: $Z_L = R_1 + R_2 // C_2$

$R_P = R_P$

$Z_O = (R_1 + R_2 // C_2) - (2R_P)$

Substituting the above terms into Equation 19, the G_{42} gain equation for complex matching is formed.

$$G_{42} = \frac{-2(R_1 + R_2 \| C_2)}{(R_1 + R_2 \| C_2) + 2R_P + (R_1 + R_2 \| C_2) - 2(R_P)} \quad \text{(EQ. 19)}$$

Cancelling the protection resistor terms in the denominator reduces the gain equation into the following simplified form.

$$G_{42} = \frac{-2(R_1 + R_2 \| C_2)}{(R_1 + R_2 \| C_2) + (R_1 + R_2 \| C_2)} = -1 \quad \text{(EQ. 20)}$$

Therefore for either resistive or complex matching the G_{42} voltage gain will always be unity and the phase will be nearly 180 degrees.

G_{24} Simulation

The G_{24} frequency response of the device can be simulated using the circuit of Figure 14.

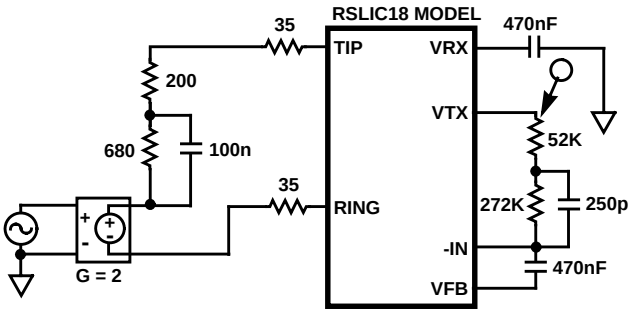

FIGURE 14. G_{24} COMPLEX LOAD SIMULATION CIRCUIT

EXPECTED RESULTS

The G_{24} results for complex matching are predicted using the voltage divider relationship shown below.

$$G_{24} = \frac{-Z_O}{Z_L + 2R_P + Z_O} \quad \text{(EQ. 21)}$$

where: $Z_L = R_1 + R_2 // C_2$

$R_P = R_P$

$Z_O = (R_1 + R_2 // C_2) - (2R_P)$

Substituting the above terms into Equation 22, the G_{24} gain equation for complex matching is formed.

$$G_{24} = \frac{-((R_1 + R_2 \| C_2) - 2(R_P))}{(R_1 + R_2 \| C_2) + 2R_P + (R_1 + R_2 \| C_2) - 2(R_P)} \quad \text{(EQ. 22)}$$

Cancelling the protection resistor terms in the denominator and substituting terms reduces the gain equation to the frequency dependent form shown below.

$$G_{42(\omega)} = \frac{-\left[(R_1 - 2R_P) + \dfrac{R_2}{1 + j\omega C_2 R_2}\right]}{2\left[R_1 + \dfrac{R_2}{1 + j\omega C_2 R_2}\right]} \quad \text{(EQ. 23)}$$

Until now, all relationships have simplified to scalar terms and have not contained frequency dependent components. Evaluating the gain at 1kHz, results in a voltage gain of 0.459 and a phase of 178 degrees. Simulation results will vary slightly due to device bandwidth.

G_{44} Simulation

The G_{44} frequency response of the device can be simulated using the circuit of Figure 15.

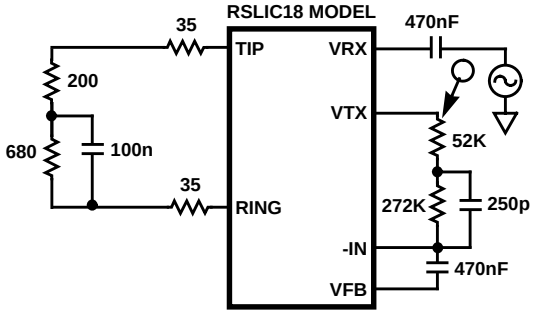

FIGURE 15. G_{44} COMPLEX LOAD SIMULATION CIRCUIT

EXPECTED RESULTS

The G_{44} results for complex matching are predicted using the voltage divider relationship shown below.

$$G_{44} = \frac{-Z_O}{Z_L + 2R_P + Z_O} \quad \text{(EQ. 24)}$$

where: $Z_L = R_1 + R_2 // C_2$

$R_P = R_P$

$Z_O = (R_1 + R_2 // C_2) - (2R_P)$

Since the G_{44} gain has the same mathematical expression as the G_{24} gain, the same frequency dependent gain equation applies to both. Evaluating the gain at 1kHz, results in a voltage gain of 0.459 and a phase of 178 degrees. Simulation results will vary slightly due to device bandwidth.

Simulation Results

The following pages contain results for both simulation examples. The magnitude and phase response of each gain path is plotted from 10Hz to 10kHz. The model will accurately predict device frequency response up to 1MHz. In addition to the graphs, numerical data is also provided for reference. Performing the above simulations is suggested when first using the model. The results obtained should agree with those provided herein.

Resistive Matching Simulation Results

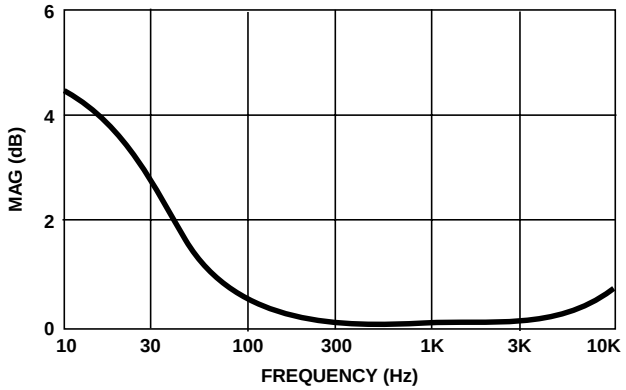

FIGURE 16. G_{42} RESISTIVE MATCHING MAGNITUDE RESPONSE

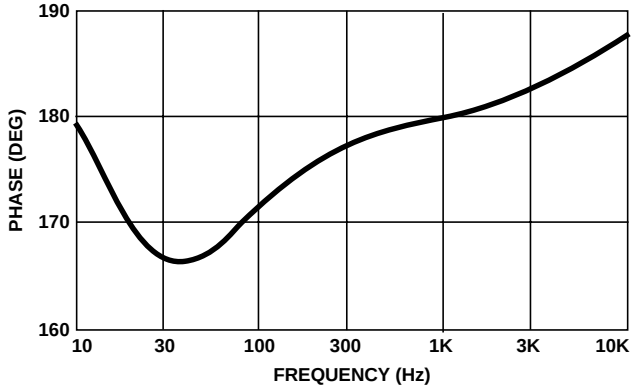

FIGURE 17. G_{42} RESISTIVE MATCHING PHASE RESPONSE

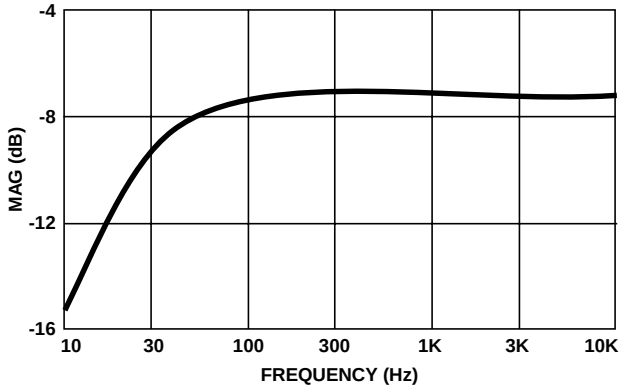

FIGURE 18. G_{24} RESISTIVE MATCHING MAGNITUDE RESPONSE

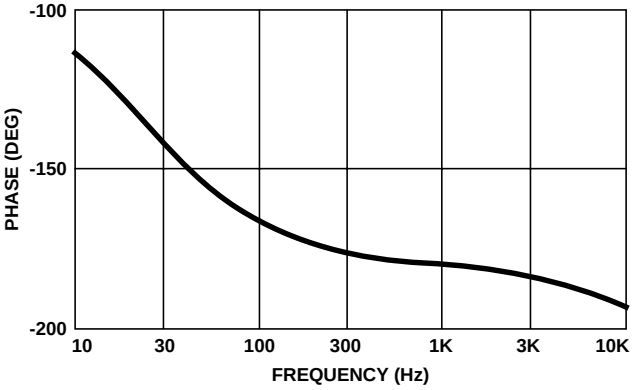

FIGURE 19. G_{24} RESISTIVE MATCHING PHASE RESPONSE

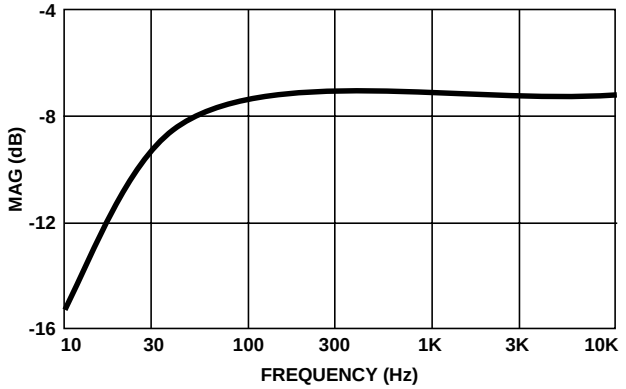

FIGURE 20. G_{44} RESISTIVE MATCHING MAGNITUDE RESPONSE

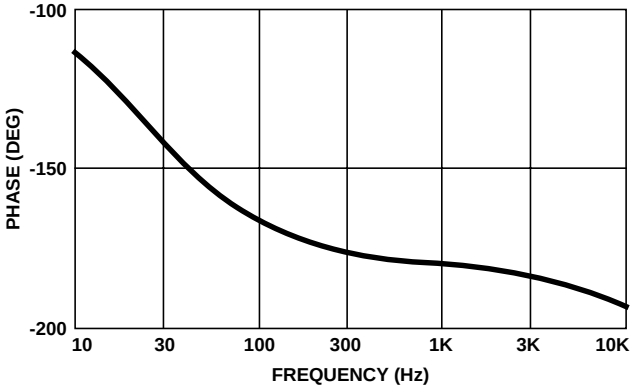

FIGURE 21. G_{44} RESISTIVE MATCHING PHASE RESPONSE

TABLE 1. RESISTIVE MATCHING NUMERICAL RESULTS

FREQUENCY	G_{42}		G_{24}		G_{44}	
	MAGNITUDE (dB)	PHASE (DEG)	MAGNITUDE (dB)	PHASE (DEG)	MAGNITUDE (dB)	PHASE (DEG)
10	4.46	179.9	-15.29	-113.0	-15.29	-113.0
30	2.64	166.8	-9.21	-141.9	-9.21	-141.9
100	0.48	171.5	-7.37	-166.9	-7.37	-166.9
300	0.06	177.1	-7.16	-175.9	-7.16	-175.9
1K	0.02	180.0	-7.14	-180.1	-7.14	-180.1
3K	0.08	182.5	-7.15	-183.8	-7.15	-183.8
10K	0.77	187.7	-7.34	-194.0	-7.34	-194.0

Complex Matching Simulation Results

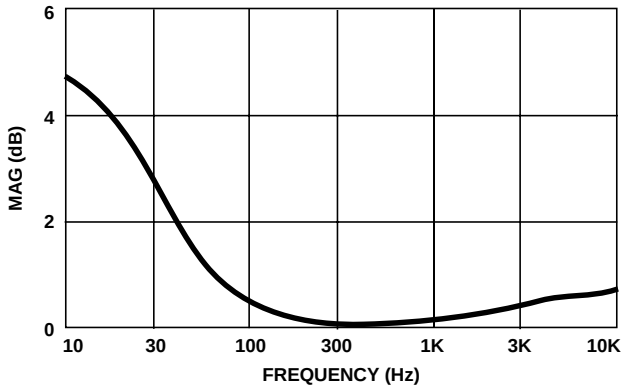

FIGURE 22. G_{42} COMPLEX MATCH MAGNITUDE RESPONSE

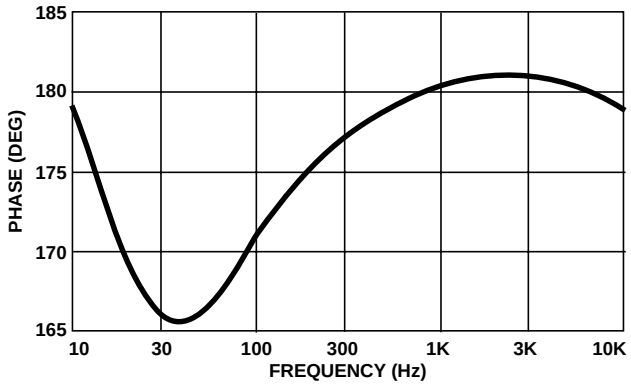

FIGURE 23. G_{42} COMPLEX MATCH PHASE RESPONSE

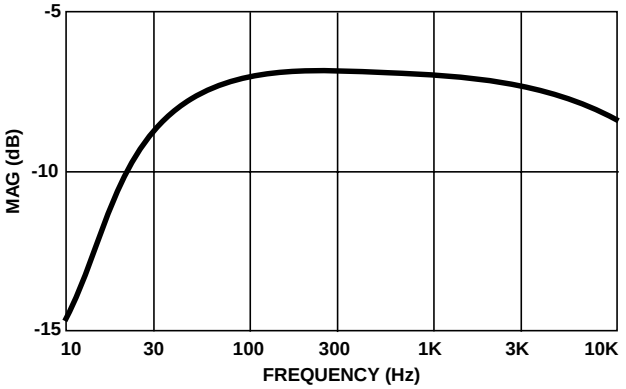

FIGURE 24. G_{24} COMPLEX MATCH MAGNITUDE RESPONSE

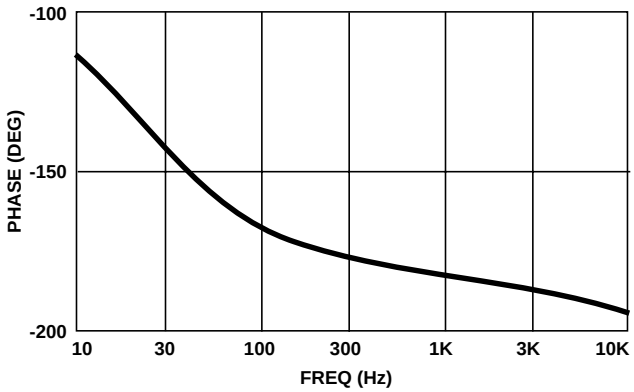

FIGURE 25. G_{24} COMPLEX MATCH PHASE RESPONSE

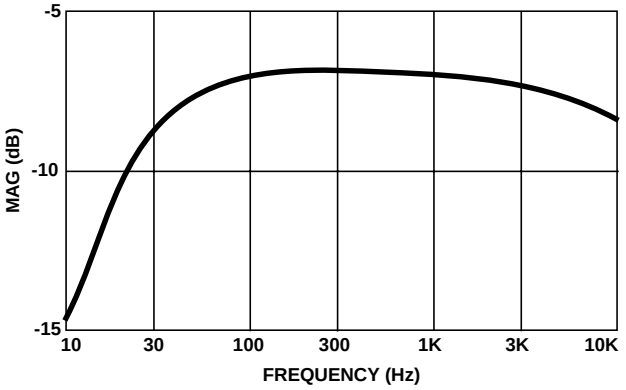

FIGURE 26. G_{44} COMPLEX MATCH MAGNITUDE RESPONSE

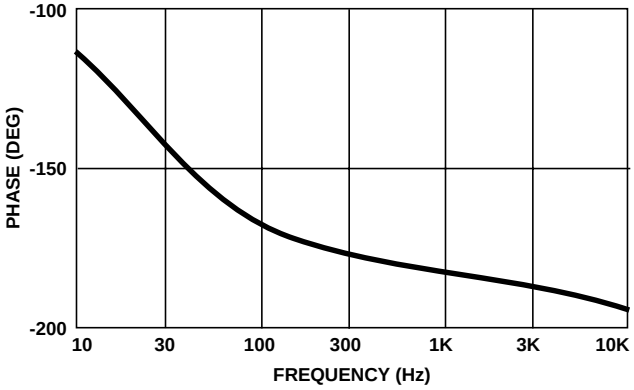

FIGURE 27. G_{44} COMPLEX MATCH PHASE RESPONSE

TABLE 2. COMPLEX MATCH NUMERICAL RESULTS

	G_{42}		G_{24}		G_{44}	
FREQUENCY	MAGNITUDE (dB)	PHASE (DEG)	MAGNITUDE (dB)	PHASE (DEG)	MAGNITUDE (dB)	PHASE (DEG)
10	4.70	179.2	-14.7	-113.8	-14.7	-113.8
30	2.74	165.9	-8.76	-143.0	-8.76	-143.0
100	0.49	171.1	-7.02	-167.6	-7.02	-167.6
300	0.07	177.2	-6.84	-176.8	-6.84	-176.8
1K	0.12	180.4	-6.92	-182.1	-6.92	-182.1
3K	0.42	181.0	-7.34	-187.1	-7.34	-187.1
10K	0.69	178.5	-8.50	-194.0	-8.50	-194.0

SPICE Net List

The following is the complete net list for the macromodel. Notations have been added to the listing to assist in decoding the net list.

SPICE Net list

Components At Amplifier Block Interconnect Level

```
R_U1_R1        $N_0002 $N_0001  200k
R_U1_R2        $N_0002 $N_0027  200k
R_U1_R3        $N_0035 $N_0043  200k
R_U1_R4        $N_0035 $N_0036  20
R_U1_R5        $N_0003 $N_0044  200k
R_U1_R6        $N_0003 $N_0010  20
R_U1_R7        $N_0036 $N_0029  600k
R_U1_R8        $N_0003 $N_0029  600k
R_U1_R9        $N_0010 $N_0028  600k
R_U1_R10       $N_0035 $N_0028  600k
R_U1_R11       $N_0028 0  150k
R_U1_R12       $N_0029 $N_0034  150k
R_U1_R13       $N_0034 $N_0004  8k
F_U1_F4        $N_0043 $N_0044 VF_U1_F4 -1
VF_U1_F4       $N_0002 $N_0005 0V
R_U1_R23       0 $N_0005  1
V_U1_V1        $N_0014 0 -12V
```

Ring Amplifier Model Components

```
E_U1_HS1_E8        $N_0006 0 $N_0014 $N_0044 59420
E_U1_HS1_E9        $N_0008 0 $N_0007 0 1
E_U1_HS1_E10       $N_0010 0 $N_0009 0 1
R_U1_HS1_R24       $N_0006 $N_0007  13.4G
R_U1_HS1_R25       $N_0011 $N_0009  65k
C_U1_HS1_C2        0 $N_0012  1p
C_U1_HS1_C3        0 $N_0009  1p
R_U1_HS1_R27       $N_0008 $N_0013  65k
C_U1_HS1_C5        0 $N_0013  1p
E_U1_HS1_E12       $N_0011 0 $N_0013 0 1
R_U1_HS1_R29       $N_0012 $N_0007  155k
C_U1_HS1_C6        $N_0010 $N_0044  8p
```

Tip Amplifier Model Components

```
E_U1_HS2_E8        $N_0015 0 $N_0014 $N_0043 49740
E_U1_HS2_E9        $N_0017 0 $N_0016 0 1
E_U1_HS2_E10       $N_0036 0 $N_0018 0 1
R_U1_HS2_R24       $N_0015 $N_0016  11.9G
R_U1_HS2_R25       $N_0019 $N_0018  55k
C_U1_HS2_C2        0 $N_0020  1p
C_U1_HS2_C3        0 $N_0018  1p
R_U1_HS2_R27       $N_0017 $N_0021  56k
C_U1_HS2_C5        0 $N_0021  1p
E_U1_HS2_E12       $N_0019 0 $N_0021 0 1
R_U1_HS2_R29       $N_0020 $N_0016  132k
C_U1_HS2_C6        $N_0036 $N_0043  5.2p
```

Transmit Amplifier Model Components

```
E_U1_HS3_E8        $N_0023 0 0 $N_0022 4151
E_U1_HS3_E9        $N_0025 0 $N_0024 0 1
E_U1_HS3_E10       $N_0027 0 $N_0026 0 1
R_U1_HS3_R24       $N_0023 $N_0024  1.25G
R_U1_HS3_R25       $N_0025 $N_0026  100k
C_U1_HS3_C2        0 $N_0024  1p
C_U1_HS3_C3        0 $N_0026  1p
```

Sense Amplifier Model Components

```
E_U1_HS4_E8        $N_0030 0 $N_0028 $N_0029 4716
E_U1_HS4_E9        $N_0032 0 $N_0031 0 1
E_U1_HS4_E10       $N_0034 0 $N_0033 0 1
R_U1_HS4_R24       $N_0030 $N_0031  611M
R_U1_HS4_R25       $N_0032 $N_0033  92k
C_U1_HS4_C2        0 $N_0031  1p
C_U1_HS4_C3        0 $N_0033  1p
```

DC Loop Current Model Components

```
G_U1_U4_G1         $N_0037 0 $N_0035 $N_0036 69.4e-6
I_U1_U4_I1         $N_0038 0 DC 34.375e-6
R_U1_U4_R1         $N_0039 0  17k
R_U1_U4_R2         $N_0041 $N_0040  100k
C_U1_U4_C2         0 $N_0039  4.7u
G_U1_U4_G2         $N_0042 0 $N_0036 $N_0035 69.4e-6
R_U1_U4_R6         0 $N_0042  10e6
R_U1_U4_R7         0 $N_0038  10e6
R_U1_U4_R8         0 $N_0037  10e6
D_U1_U4_D6         $N_0042 $N_0038 Dbreak
D_U1_U4_D8         $N_0037 $N_0038 Dbreak
G_U1_U4_G6         $N_0043 $N_0044 $N_0039 0 58.823e-6
G_U1_U4_G8         $N_0039 0 $N_0040 0 4e-3
D_U1_U4_D10        $N_0038 $N_0045 Dbreak
R_U1_U4_R33        0 $N_0045  50k
E_U1_U4_E3         $N_0041 0 $N_0045 0 1
I_U1_U4_I17        $N_0039 0 DC 20u
G_U1_U4_G10        $N_0039 0 $N_0046 0 2.5e-6
V_U1_U4_V16        $N_0046 0 -24
R_U1_U4_R40        0 $N_0040  100e15
V_U1_V1        $N_0014 0 -12V
```

*End of Subcircuit

The files required to load the model in MicroSim Pspice are located on our website at: www.intersil.com.