# FAST CMOS BUFFER/CLOCK DRIVER

**IDT49FCT805BT/CT**

## FEATURES:

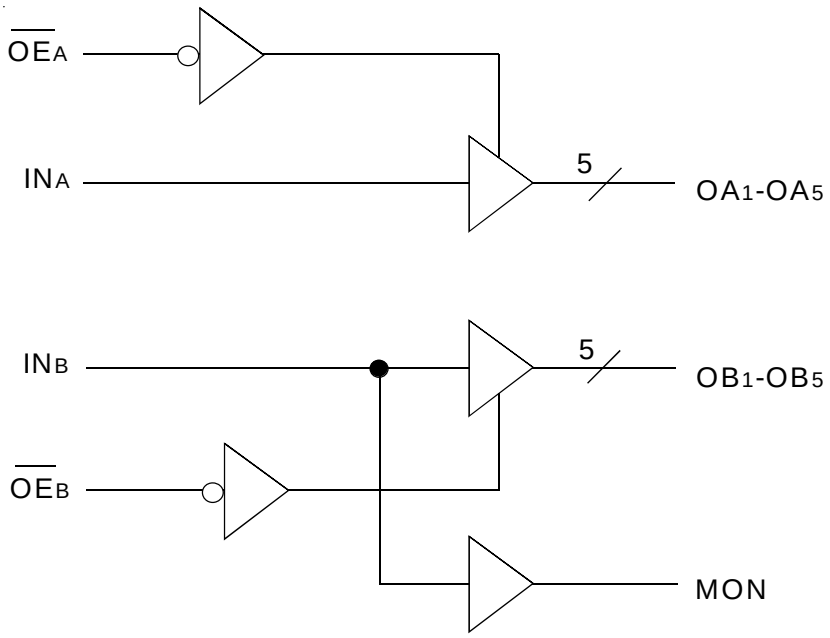
- **0.5 MICRON CMOS Technology**
- **Guaranteed low skew < 500ps (max.)**
- **Very low duty cycle distortion < 600ps (max.)**
- **Low CMOS power levels**
- **TTL compatible inputs and outputs**
- **TTL level output voltage swings**
- **High drive: -32mA $I_{OH}$, +48mA $I_{OL}$**
- **Two independent output banks with 3-state control**
- **1:5 fanout per bank**
- **"Heartbeat" monitor output**
- **ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)**
- **Available in the following packages:**
  - *Commercial: QSOP, SOIC, SSOP*
  - *Military: CERDIP, LCC*

## DESCRIPTION:

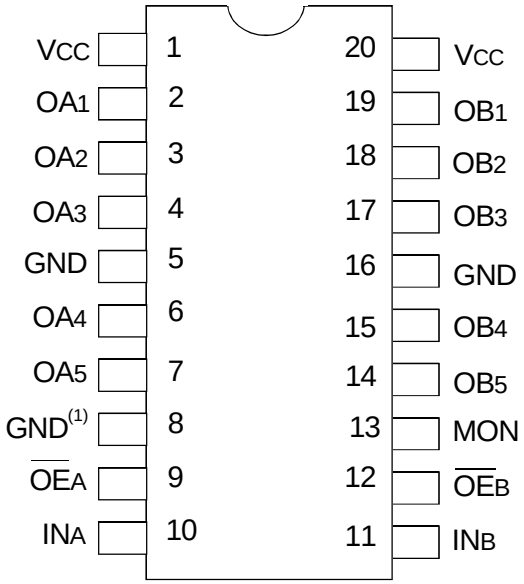
This buffer/clock driver is built using advanced dual metal CMOS technology. The FCT805T is a non-inverting clock driver consisting of two banks of drivers. Each bank drives five output buffers from a standard TTL compatible input. This part has extremely low output skew, pulse skew, and package skew. The device has a "heart-beat" monitor for diagnostics and PLL driving. The monitor output is identical to all other outputs and complies with the output specifications in this document.

The FCT805T is designed for fast, clean edge rates to provide accurate clock distribution in high speed systems.

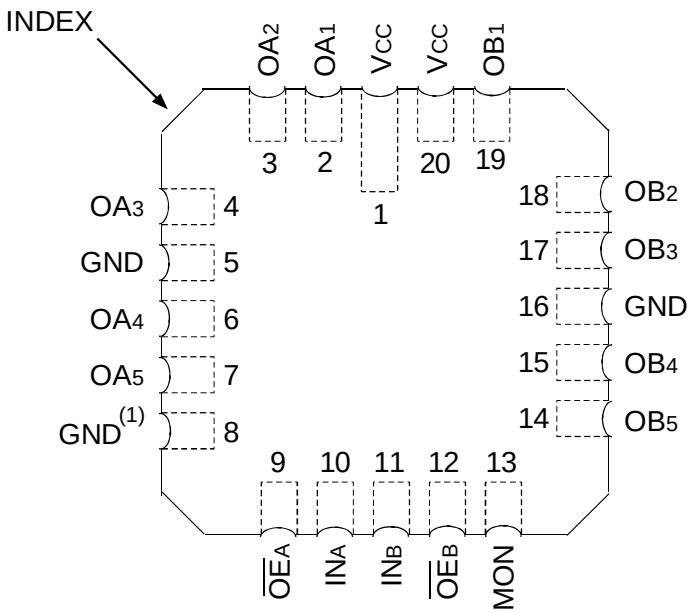
## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**QSOP/ SOIC/ SSOP/ CERDIP**
**TOP VIEW**




**LCC**
**TOP VIEW**

**NOTE:**
1. Pin 8 is internally connected to GND. To insure compatibility with all products, pin 8 should be connected to GND at the board level.

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max | Unit |
|---|---|---|---|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | –0.5 to +7 | V |
| $T_{STG}$ | Storage Temperature | –65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | –60 to +120 | mA |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## CAPACITANCE ($T_A$ = +25°C, f = 1.0MHz)

| Symbol | Parameter(1) | Conditions | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 0V | 4.5 | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 0V | 5.5 | 8 | pF |

**NOTE:**
1. This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

| Pin Names | Description |
|---|---|
| $\overline{OE}_A$, $\overline{OE}_B$ | 3-State Output Enable Inputs (Active LOW) |
| $IN_A$, $IN_B$ | Clock Inputs |
| OAx, OBx | Clock Outputs |
| MON | Monitor Output |

## FUNCTION TABLE(1)

| Inputs | | Outputs | |
|---|---|---|---|
| $\overline{OE}_A$, $\overline{OE}_B$ | $IN_A$, $IN_B$ | OAx, OBx | MON |
| L | L | L | L |
| L | H | H | H |
| H | L | Z | L |
| H | H | Z | H |

**NOTE:**
1. H = HIGH
L = LOW
Z = High-Impedance

# DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Commercial: $T_A$ = 0°C to +70°C, Military: $T_A$ = -55°C to +125°C, $V_{CC}$ = 5V ± 10%

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Level | Guaranteed Logic HIGH Level | | 2 | — | — | V |
| $V_{IL}$ | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| $I_{IH}$ | Input HIGH Current[5] | $V_{CC}$ = Max. | $V_I$ = 2.7V | — | — | ±1 | µA |
| $I_{IL}$ | Input LOW Current[5] | $V_{CC}$ = Max. | $V_I$ = 0.5V | — | — | ±1 | µA |
| $I_{OZH}$ | High Impedance Output Current | $V_{CC}$ = Max. | $V_O$ = 2.7V | — | — | ±1 | µA |
| $I_{OZL}$ | (3-State Output Pins) | | $V_O$ = 0.5V | — | — | ±1 | |
| $I_I$ | Input HIGH Current | $V_{CC}$ = Max., $V_I$ = $V_{CC}$ (Max.) | | — | — | ±1 | µA |
| $V_{IK}$ | Clamp Diode Voltage | $V_{CC}$ = Min., $I_{IN}$ = –18mA | | — | –0.7 | –1.2 | V |
| $I_{OS}$ | Short Circuit Current | $V_{CC}$ = Max., $V_O$ = GND[3] | | –60 | –120 | –255 | mA |
| $V_{OH}$ | Output HIGH Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OH}$ = –12mA MIL<br>$I_{OH}$ = –15mA COM'L | 2.4 | 3.3 | — | V |
| | | | $I_{OH}$ = –24mA MIL<br>$I_{OH}$ = –32mA COM'L[4] | 2 | 3 | — | V |
| $V_{OL}$ | Output LOW Voltage | $V_{CC}$ = Min.<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ | $I_{OL}$ = 32mA MIL<br>$I_{OL}$ = 48mA COM'L | — | 0.3 | 0.55 | V |
| $I_{OFF}$ | Input/Output Power Off Leakage[5] | $V_{CC}$ = 0V, $V_{IN}$ or $V_O \leq$ 4.5V | | — | — | ±1 | µA |
| $V_H$ | Input Hysteresis for all inputs | — | | — | 150 | — | mV |
| $I_{CCL}$<br>$I_{CCH}$<br>$I_{CCZ}$ | Quiescent Power Supply Current | $V_{CC}$ = Max., $V_{IN}$ = GND or $V_{CC}$ | | — | 5 | 500 | µA |

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Duration of the condition should not exceed one second.
5. The test limit for this parameter is ±5µA at $T_A$ = -55°C.

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions[1] | | Min. | Typ.[2] | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $\Delta I_{CC}$ | Quiescent Power Supply Current<br>TTL Inputs HIGH | $V_{CC}$ = Max.<br>$V_{IN}$ = 3.4V[3] | | — | 1 | 2 | mA |
| $I_{CCD}$ | Dynamic Power Supply Current[4] | $V_{CC}$ = Max.<br>Outputs Open<br>$\overline{OE}_A$ = $\overline{OE}_B$ = GND<br>50% Duty Cycle | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 60 | 100 | µA/MHz |
| $I_C$ | Total Power Supply Current[6] | $V_{CC}$ = Max.<br>Outputs Open<br>fo = 25MHz<br>50% Duty Cycle<br>$\overline{OE}_A$ = $\overline{OE}_B$ = $V_{CC}$<br>Mon. Output Toggling | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 1.5 | 3 | mA |
| | | | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 1.8 | 4 | |
| | | $V_{CC}$ = Max.<br>Outputs Open<br>fo = 50MHz<br>50% Duty Cycle<br>$\overline{OE}_A$ = $\overline{OE}_B$ = GND<br>Eleven Outputs Toggling | $V_{IN}$ = $V_{CC}$<br>$V_{IN}$ = GND | — | 33 | 55.5[5] | |
| | | | $V_{IN}$ = 3.4V<br>$V_{IN}$ = GND | — | 33.5 | 57.5[5] | |

**NOTES:**

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC}$ = 5V, +25°C ambient.
3. Per TTL driven input ($V_{IN}$ = 3.4V); all other inputs at $V_{CC}$ or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
5. Values for these conditions are examples of the $I_C$ formula. These limits are guaranteed but not tested.
6. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_O N_O)$
   $I_{CC}$ = Quiescent Current ($I_{CCL}$, $I_{CCH}$ and $I_{CCZ}$)
   $\Delta I_{CC}$ = Power Supply Current for a TTL High Input ($V_{IN}$ = 3.4V)
   $D_H$ = Duty Cycle for TTL Inputs High
   $N_T$ = Number of TTL Inputs at $D_H$
   $I_{CCD}$ = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   $f_O$ = Output Frequency
   $N_O$ = Number of Outputs at $f_O$
   All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY(1,2)

| Symbol | Parameter | Conditions(3) | FCT805BT | | FCT805CT | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min.(4) | Max. | Min.(4) | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$IN_A$ to $OA_x$, $IN_B$ to $OB_x$ | $C_L$ = 50pF<br>$R_L$ = 500Ω | 1.5 | 5.7 | 1.5 | 5.2 | ns |
| $t_R$ | Output Rise Time | | — | 2 | — | 2 | ns |
| $t_F$ | Output Fall Time | | — | 1.5 | — | 1.5 | ns |
| $t_{SK(O)}$ | Output skew: skew between outputs of all banks of same package (inputs tied together) | | — | 0.9 | — | 0.7 | ns |
| $t_{SK(P)}$ | Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$) | | — | 0.9 | — | 0.8 | ns |
| $t_{SK(PP)}$ | Part-to-part skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade | | — | 1.5 | — | 1.2 | ns |
| $t_{PZL}$<br>$t_{PZH}$ | Output Enable Time<br>$\overline{OE}_A$ to $OA_x$, $\overline{OE}_B$ to $OB_x$ | | 1.5 | 6.5 | 1.5 | 6 | ns |
| $t_{PLZ}$<br>$t_{PHZ}$ | Output Disable Time<br>$\overline{OE}_A$ to $OA_x$, $\overline{OE}_B$ to $OB_x$ | | 1.5 | 6.5 | 1.5 | 6 | ns |

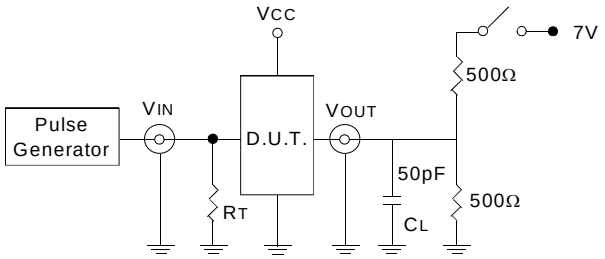
**NOTES:**
1. $t_{PLH}$, $t_{PHL}$, and $t_{SK}(pp)$ are production tested. All other parameters are guaranteed but not production tested.
2. Propagation delay range indicated by Min. and Max. limit is dues to Vcc, operating temperature, and process parameters. These propagation delay limits do not imply skew.
3. See Test Circuits and Waveforms.
4. Minimum limits are guaranteed but not tested on Propagation Delays.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL(1,2)

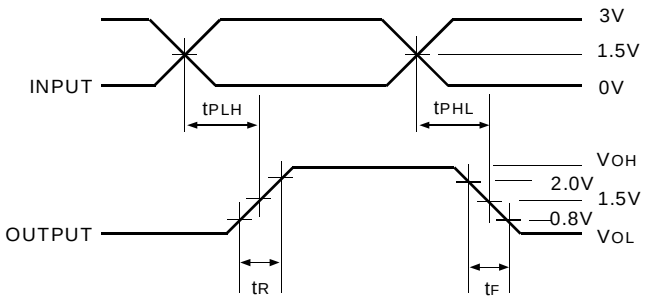
| Symbol | Parameter | Conditions(3) | FCT805BT | | FCT805CT | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min.(4) | Max. | Min.(4) | Max. | |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>$IN_A$ to $OA_x$, $IN_B$ to $OB_x$ | $C_L$ = 50pF<br>$R_L$ = 500Ω | 1.5 | 5 | 1.5 | 4.5 | ns |
| $t_R$ | Output Rise Time | | — | 1.5 | — | 1.5 | ns |
| $t_F$ | Output Fall Time | | — | 1.5 | — | 1.5 | ns |
| $t_{SK(O)}$ | Output skew: skew between outputs of all banks of same package (inputs tied together) | | — | 0.7 | — | 0.5 | ns |
| $t_{SK(P)}$ | Pulse skew: skew between opposite transitions of same output ($\|t_{PHL} - t_{PLH}\|$) | | — | 0.7 | — | 0.6 | ns |
| $t_{SK(PP)}$ | Part-to-part skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade | | — | 1.2 | — | 1 | ns |
| $t_{PZL}$<br>$t_{PZH}$ | Output Enable Time<br>$\overline{OE}_A$ to $OA_x$, $\overline{OE}_B$ to $OB_x$ | | 1.5 | 6 | 1.5 | 5 | ns |
| $t_{PLZ}$<br>$t_{PHZ}$ | Output Disable Time<br>$\overline{OE}_A$ to $OA_x$, $\overline{OE}_B$ to $OB_x$ | | 1.5 | 6 | 1.5 | 5 | ns |

**NOTES:**
1. $t_{PLH}$, $t_{PHL}$, and $t_{SK}(pp)$ are production tested. All other parameters are guaranteed but not production tested.
2. Propagation delay range indicated by Min. and Max. limit is dues to Vcc, operating temperature, and process parameters. These propagation delay limits do not imply skew.
3. See Test Circuits and Waveforms.
4. Minimum limits are guaranteed but not tested on Propagation Delays.

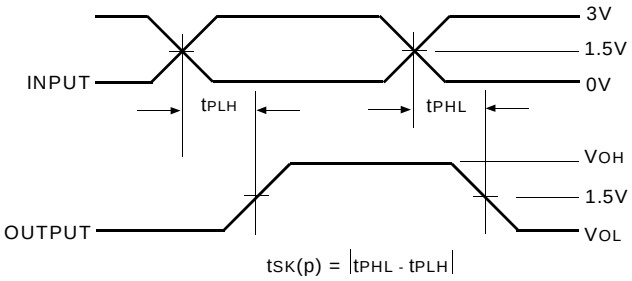
# TEST CIRCUITS AND WAVEFORMS




***Test Circuits for All Outputs***

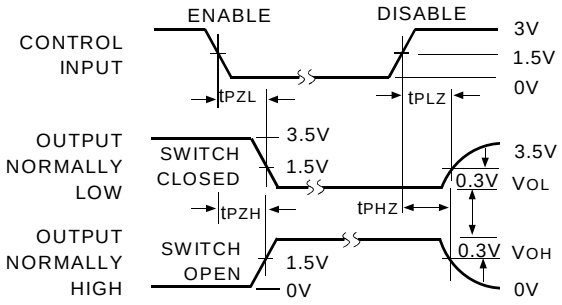



***Package Delay***




$t_{SK(p)} = |t_{PHL} - t_{PLH}|$

***Pulse Skew - $t_{SK(P)}$***



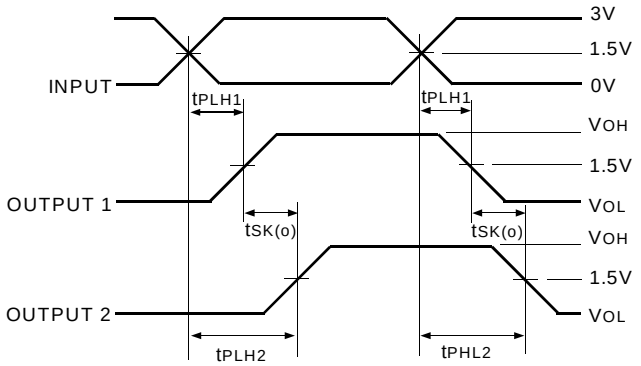

***Enable and Disable Times***

**NOTES:**
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; $t_F$ ≤ 2.5ns; $t_R$ ≤ 2.5ns

# SWITCH POSITION

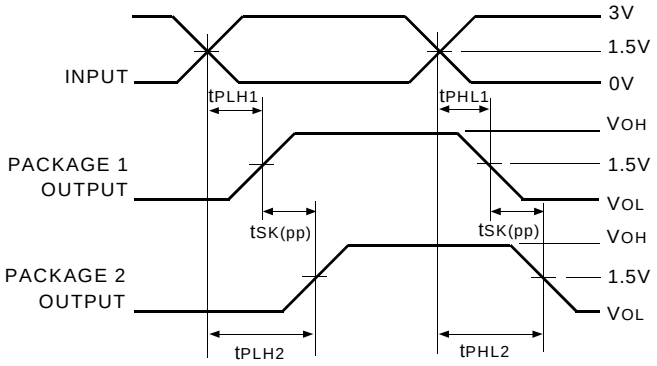
| Test | Switch |
|---|---|
| Disable LOW<br>Enable LOW | Closed |
| Disable HIGH<br>Enable HIGH | GND |

**DEFINITIONS:**
$C_L$ = Load capacitance: includes jig and probe capacitance.
$R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator.




$t_{SK(o)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

***Output Skew***




$t_{SK(pp)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

***Part-to-Part Skew - $t_{SK(PP)}$***

**NOTE:**
1. Package 1 and Package 2 are same device type and speed grade.

## ORDERING INFORMATION

IDT49FCT XXXX (Device Type) XX (Package) X (Process)

**Process**

| | |
|---|---|
| Blank | Commercial (0°C to +70°C) |
| B | MIL-STD-883, Class B (– 55°C to +125°C) |

**Package**

Commercial Options

| | |
|---|---|
| SO | Small Outline IC |
| Q | Quarter-size Small Outline Package |
| PY | Shrink Small Outline Package |

Military Options

| | |
|---|---|
| D | CERDIP |
| L | Leadless Chip Carrier |

**Device Type**

| | |
|---|---|
| 805BT | Fast CMOS Buffer/Clock Driver |
| 805CT | |

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