Hitachi Flash Cards

User's Manual

HITACHI

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Hitachi semiconductor

Notice

Contents

Section 1 Hitachi Flash Cards

1.1 Introduction

Hitachi flash cards are designed to (1) replace hard disks and (2) be embedded to various equipment. This manual is intended for those using Hitachi flash cards for these applications for the first time. For this reason, each item is not described in detail. Refer to the data sheet or other related documents for detailed information. Internal card configuration, operating mode, data transfer protocol and formatting at shipment are explained in the following chapters.

1.2 Hitachi PC-ATA Card

PC cards are used to extend the functions of memories, modems, LANs, and various equipment like laptop- and notebook-type computers are equipped with sockets for PC cards. Such PC-card standards as the physical, electrical and interface specifications have been developed in cooperation with JEIDA (Japan Electronic Industry Development Association) and PCMCIA (Personal Computer Memory Card International Association). Although both these organizations previously issued standards separately, they were unified into the PC Card Standard in 1995 and issued jointly issui.

PC cards are classified into the following two types.

(1) Memory cards: Flash memory card, SRAM card, ROM card, etc.
(2) I/O cards: Flash ATA card, HDD card, modem card, LAN card, etc.

Memory card is used as ordinary memories in order to extend memory capacity and I/O cards as peripherals for extending functions.

Hitachi's PC-ATA flash card is classified as an I/O card. The built-in controller is designed to precisely control data writing into the flash memory, achieving the same interface as a hard disk. Thanks to this function, the minimum data reading and writing unit is one sector (1 sector = 512 bytes) and not one byte (8 bits) like memory.

Unlike hard disks, this card has no driving system such as disks or heads, and features (1) low power consumption, (2) high-speed operation and (3) vibration resistance.

The flash memory card mentioned here refers to one that is not designed to internally control data writing into the built-in flash memory but to achieve an interface as the memory, while the HDD card refers to one having a small rotating magnetic hard disk.

The physical specifications of Hitachi PC-ATA card (e.g. card dimensions and connector shapes) are in accordance with the PC Card Standard. The device like notebook (laptop) type computer, which controls the cards, is called “the host”, and the following is the two types of specifications for the interface between the host and the card:

(1) PC card ATA specification
(2) True-IDE specification

PC card ATA specification is regulated by the PC Card Standard. Simply inserting the card in the socket enables information written onto it to be read by the host and the card to be recognized as a flash ATA card. The host then writes data onto the card to set the card operating mode.

The True-IDE specification does not follow the PC Card Standard. They were specified by changing the IDE hard disk interface specifications for card application and for handling cards as hard disks. While PC card ATA specification requires cards to be recognized and operating mode to be set, the True-IDE specification does not, thereby reducing the load on the host.

1.3 Hitachi CompactFlash™

Because PC cards are too large for small, lightweight equipment like digital cameras and hand-held PCs, several types of small memory cards are available. The CompactFlash™ small memory card standard was proposed by SanDisk Corporation of the U.S., on which Hitachi CompactFlash™ is based. The host interface is compatible with PC card ATA or True-IDE specification, the same as Hitachi PC-ATA card.

Hitachi flash cards refer to the above PC-ATA card and CompactFlash™.

1.4 JEIDA and PCMCIA

PC card-related standard has been established by JEIDA (Japan Electronic Industry Development Association) and PCMCIA (Personal Computer Memory Card International Association) since JEIDA started establishing standard for memory cards like SRAMs in 1985.

In 1989, PC manufacturers in the U.S. established PCMCIA. Although PCMCIA and JEIDA cooperated in establishing JEIDA Ver 4.0/PCMCIA 1.0 in 1990, to covered only memory cards. Since I/O card specifications were specified by PCMCIA 2.0 established in 1991, such cards as modem and LAN cards have been widely used to extend the memories and functions of notebook PCs.

JEIDA Ver 4.2/PCMCIA 2.1 established in 1993 specified software for using PC cards. And in 1995, the standards were unified into the PC Card Standard, to which several more standards have been, and will continue to be added.

JEIDA and PCMCIA can be contacted at:

Japan Electronic Industry Development Association
Personal Computer Operation Committee and
IC Memory Card Applied Technology Special Committee,
3-5-8 Shiba-koen, Minato-ku, Tokyo, Japan
Tel: 03-3433-1923

Personal Computer Memory Card International Association
2635 North First Street, Suite 209
San Jose, CA 95134 USA

1.5 CFA

The CompactFlash™ small flash memory card standard was proposed by SanDisk Corporation of the U.S., which is promoted by CFA (CompactFlash Association). CompactFlash™, a trademark of SanDisk Corporation of the U.S., is licensed to CFA. The size of the CompactFlash™ is approximately one third of that of a PC card. Its electrical and interface specifications comply with PC card ATA and True-IDE specifications.

CFA can be contacted at:

CompactFlash Association
PO. Box 51537
Palo Alto, CA 94303
http:www.compactflash.org

Section 2 Hitachi Flash Cards Overview

2.1 Comparison of PC-ATA Card and CompactFlash™

The sizes of PC cards are classified into three types by thickness. Type I to Type III and PC-ATA cards are classified as Type II (overall dimensions: $54.0 \times 85.6 \times 5.0$ (mm)). The size of the CompactFlash™ is approximately one third of PC cards (overall dimensions: $42.8 \times 36.4 \times 3.3$ (mm)). Figures 2.1 and 2.2 show their overall dimensions.

Tables 2.1 and 2.2 show the pin assignments for the PC-ATA Card and CompactFlash™. Since the functions of some pins vary depending on the card mode (refer to Chapter 3), the tables show the signal names in each mode. While only 50 of the 68 pins of the PC-ATA card slot are used, all 50 pins are used for the CompactFlash™.

Because the electrical and interface specifications of Hitachi PC-ATA Card and CompactFlash™ are standardized (refer to the data sheet, for detailed specifications since differences exist between generations), PC-ATA Card and CompactFlash™ are not differentiated between in the descriptions below. Note that CompactFlash™ can also be used in the PC-ATA card slot by mounting them in a PC card adapter.

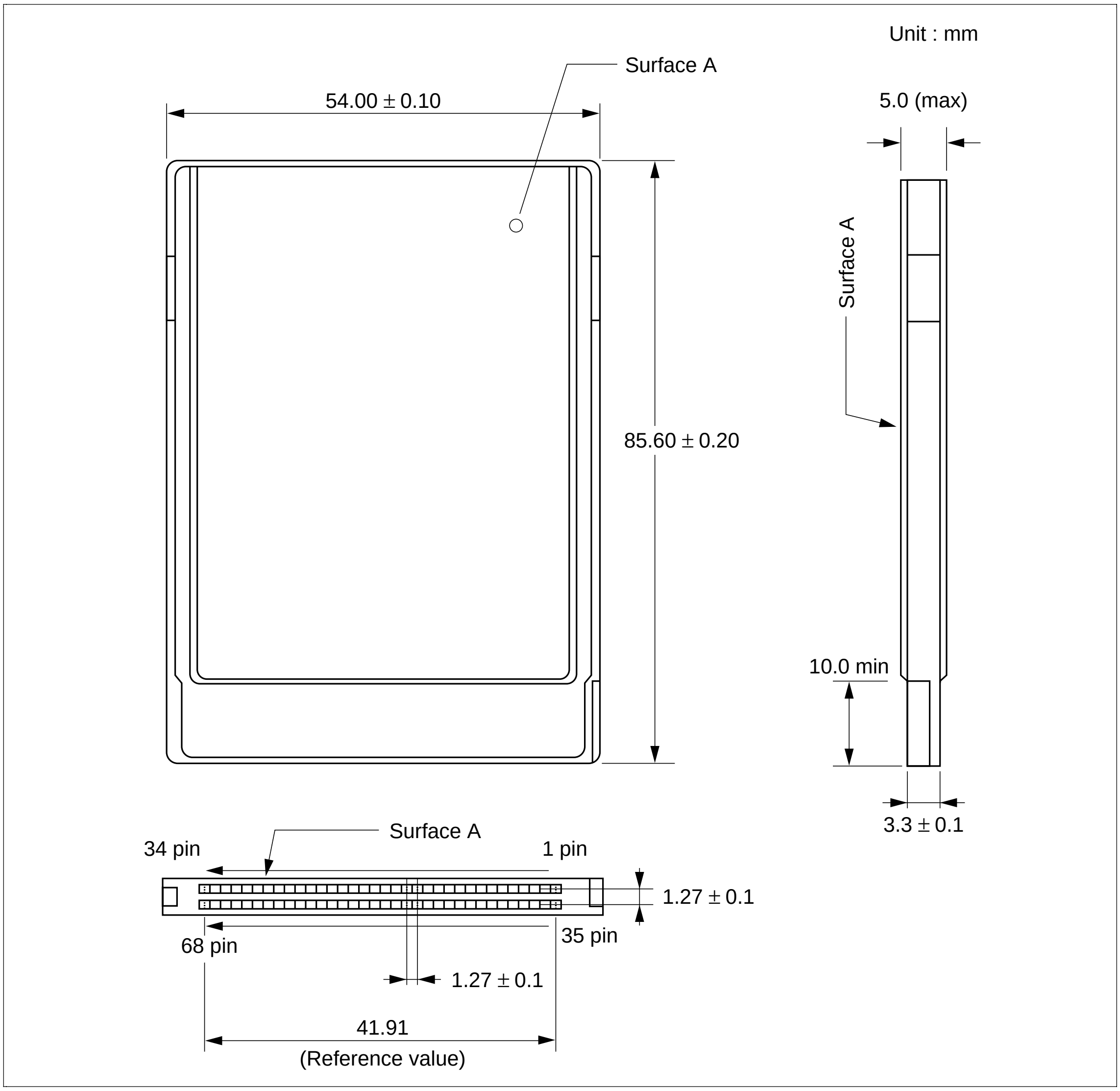


Figure 2.1 Overall Dimensions of PC-ATA Card

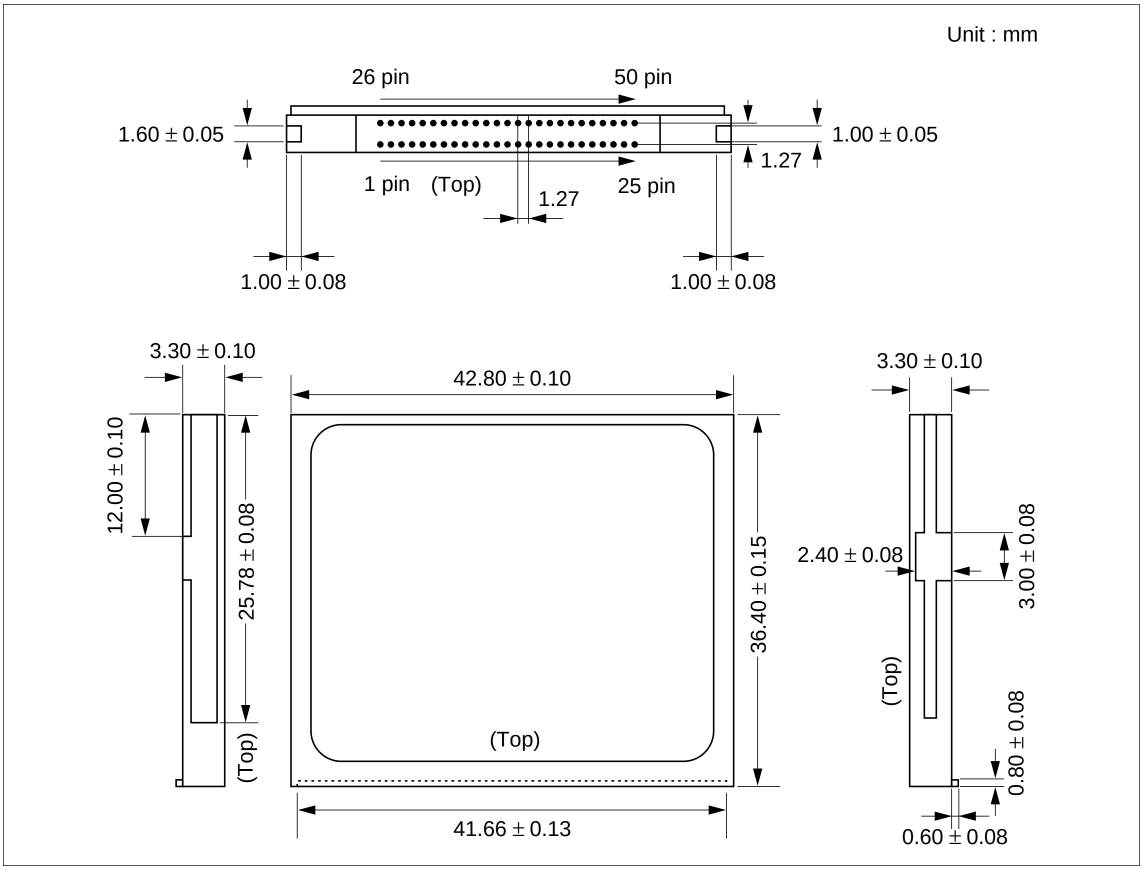


Figure 2.2 Overall Dimensions of CompactFlash™

Table 2.1 PC-ATA Card Pin Assignment

	Memory card mode		I/O card mode		True-IDE mode	
Pin No.	Signal	Input (I) /Output (O)	Signal	Input (I) /Output (O)	Signal	Input (I) /Output (O)
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CE1	I
8	A10	I	A10	I	A10	I
9	-OE	I	-OE	I	-ATASEL	I
10	—	—	—	—	—	—
11	A9	I	A9	I	A9	I
12	A8	I	A8	I	A8	I
13	—	—	—	—	—	—
14	—	—	—	—	—	—
15	-WE	I	-WE	I	-WE	I
16	RDY/-BSY	O	-IREQ	O	INTRQ	O
17	VCC	—	VCC	—	VCC	—
18	—	—	—	—	—	—
19	—	—	—	—	—	—
20	—	—	—	—	—	—
21	—	—	—	—	—	—
22	A7	I	A7	I	A7	I
23	A6	I	A6	I	A6	I
24	A5	I	A5	I	A5	I
25	A4	I	A4	I	A4	I
26	A3	I	A3	I	A3	I
27	A2	I	A2	I	A2	I
28	A1	I	A1	I	A1	I
29	A0	I	A0	I	A0	I
30	D0	I/O	D0	I/O	D0	I/O

Table 2.1 PC-ATA Card Pin Assignment (cont.)

	Memory card mode		I/O card mode		True-IDE mode	
Pin No.	**Signal**	**Input (I) /Output (O)**	**Signal**	**Input (I) /Output (O)**	**Signal**	**Input (I) /Output (O)**
31	D1	I/O	D1	I/O	D1	I/O
32	D2	I/O	D2	I/O	D2	I/O
33	WP	O	-IOIS16	O	-IOIS16	O
34	GND	—	GND	—	GND	—
35	GND	—	GND	—	GND	—
36	-CD1	O	-CD1	O	-CD1	O
37	D11	I/O	D11	I/O	D11	I/O
38	D12	I/O	D12	I/O	D12	I/O
39	D13	I/O	D13	I/O	D13	I/O
40	D14	I/O	D14	I/O	D14	I/O
41	D15	I/O	D15	I/O	D15	I/O
42	-CE2	I	-CE2	I	-CE2	I
43	-VS1	O	-VS1	O	-VS1	O
44	-IORD	I	-IORD	I	-IORD	I
45	-IOWR	I	-IOWR	I	-IOWR	I
46	—	—	—	—	—	—
47	—	—	—	—	—	—
48	—	—	—	—	—	—
49	—	—	—	—	—	—
50	—	—	—	—	—	—
51	VCC	—	VCC	—	VCC	—
52	—	—	—	—	—	—
53	—	—	—	—	—	—
54	—	—	—	—	—	—
55	—	—	—	—	—	—
56	-CSEL	I	-CSEL	I	-CSEL	I
57	-VS2	O	-VS2	O	-VS2	O
58	RESET	I	RESET	I	-RESET	I
59	-WAIT	O	-WAIT	O	IORDY	O
60	-INPACK	O	-INPACK	O	-INPACK	O

Table 2.1 PC-ATA Card Pin Assignment (cont.)

	Memory card mode		I/O card mode		True-IDE mode	
Pin No.	**Signal**	**Input (I) /Output (O)**	**Signal**	**Input (I) /Output (O)**	**Signal**	**Input (I) /Output (O)**
61	-REG	I	-REG	I	-REG	I
62	BVD2	I/O	-SPKR	I/O	-DASP	I/O
63	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O
64	D8	I/O	D8	I/O	D8	I/O
65	D9	I/O	D9	I/O	D9	I/O
66	D10	I/O	D10	I/O	D10	I/O
67	-CD2	O	-CD2	O	-CD2	O
68	GND	—	GND	—	GND	—

Table 2.2 CompactFlash™ Pin Assignment

	Memory card mode		I/O card mode		True-IDE mode	
Pin No.	**Signal**	**Input (I) /Output (O)**	**Signal**	**Input (I) /Output (O)**	**Signal**	**Input (I) /Output (O)**
1	GND	—	GND	—	GND	—
2	D3	I/O	D3	I/O	D3	I/O
3	D4	I/O	D4	I/O	D4	I/O
4	D5	I/O	D5	I/O	D5	I/O
5	D6	I/O	D6	I/O	D6	I/O
6	D7	I/O	D7	I/O	D7	I/O
7	-CE1	I	-CE1	I	-CE1	I
8	A10	I	A10	I	A10	I
9	-OE	I	-OE	I	-ATASEL	I
10	A9	I	A9	I	A9	I
11	A8	I	A8	I	A8	I
12	A7	I	A7	I	A7	I
13	VCC	—	VCC	—	VCC	—
14	A6	I	A6	I	A6	I
15	A5	I	A5	I	A5	I
16	A4	I	A4	I	A4	I
17	A3	I	A3	I	A3	I

Table 2.2 CompactFlash™ Pin Assignment (cont.)

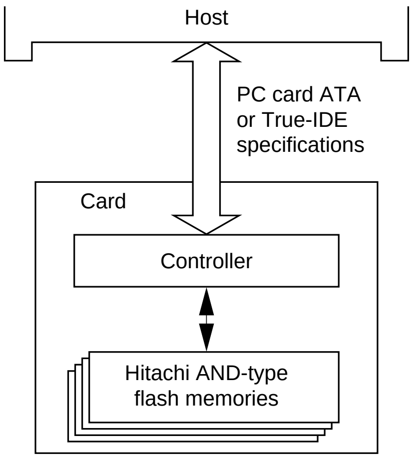
	Memory card mode		I/O card mode		True-IDE mode	
Pin No.	**Signal**	**Input (I) /Output (O)**	**Signal**	**Input (I) /Output (O)**	**Signal**	**Input (I) /Output (O)**
18	A2	I	A2	I	A2	I
19	A1	I	A1	I	A1	I
20	A0	I	A0	I	A0	I
21	D0	I/O	D0	I/O	D0	I/O
22	D1	I/O	D1	I/O	D1	I/O
23	D2	I/O	D2	I/O	D2	I/O
24	WP	O	-IOIS16	O	-IOIS16	O
25	-CD2	O	-CD2	O	-CD2	O
26	-CD1	O	-CD1	O	-CD1	O
27	D11	I/O	D11	I/O	D11	I/O
28	D12	I/O	D12	I/O	D12	I/O
29	D13	I/O	D13	I/O	D13	I/O
30	D14	I/O	D14	I/O	D14	I/O
31	D15	I/O	D15	I/O	D15	I/O
32	-CE2	I	-CE2	I	-CE2	I
33	-VS1	O	-VS1	O	-VS1	O
34	-IORD	I	-IORD	I	-IORD	I
35	-IOWR	I	-IOWR	I	-IOWR	I
36	-WE	I	-WE	I	-WE	I
37	RDY/-BSY	O	-IREQ	O	INTRQ	O
38	VCC	—	VCC	—	VCC	—
39	-CSEL	I	-CSEL	I	-CSEL	I
40	-VS2	O	-VS2	O	-VS2	O
41	RESET	I	RESET	I	-RESET	I
42	-WAIT	O	-WAIT	O	IORDY	O
43	-INPACK	O	-INPACK	O	-INPACK	O
44	-REG	I	-REG	I	-REG	I
45	BVD2	I/O	-SPKR	I/O	-DASP	I/O
46	BVD1	I/O	-STSCHG	I/O	-PDIAG	I/O

Table 2.2 CompactFlash™ Pin Assignment (cont.)

	Memory card mode		I/O card mode		True-IDE mode	
Pin No.	**Signal**	**Input (I) /Output (O)**	**Signal**	**Input (I) /Output (O)**	**Signal**	**Input (I) /Output (O)**
47	D8	I/O	D8	I/O	D8	I/O
48	D9	I/O	D9	I/O	D9	I/O
49	D10	I/O	D10	I/O	D10	I/O
50	GND	—	GND	—	GND	—

2.2 Interface Specifications

Hitachi flash cards are equipped with Hitachi AND-type flash memories, which are controlled by built-in controllers. For the interface between the controller and the host, you can select either PC card ATA or True-IDE specifications. When turning the power on, set the -OE (-ATASEL) pin at level "H" to select the PC card ATA specification or at GND to select the True-IDE specification (see figure 2.3).



PC card ATA specifications selected when the -OE (-ATASEL) pin is set at "H" level at power-on. As specified by the PC Card Standard, the host recognizes the card and sets the operating mode.

True-IDE specifications selected when the -OE (-ATASEL) pin is set at GND at power-on. The card is handled as a hard disk in accordance with modified IDE specification for card. IDE specification is one of hard disk interface specification.

Figure 2.3 Interface Specifications

2.3 Address Space

With the PC card ATA specification interface, the memory and I/O address spaces can be seen from the host as shown in figure 2.4. Writing and reading are controlled by the -OE and -WE signals in the memory address space and by the -IORD and -IOWR signals in the I/O address space.

The memory address space is further divided into attribute and common memory areas. The attribute memory area includes a configuration registers used for setting the card operating mode and card information structure (CIS) describing information for recognizing the card type. The common memory area can contain a task file registers for communicating data with the host. Use the -REG signal to switch between the attribute and common memory areas. Set this signal at level “L” to access the attribute memory area or at level “H” for the common memory area.

Task file registers can also be assigned to the I/O address space. Whether it is assigned to the I/O address space or the common memory area is determined by the host.

The True-ID specification only has an I/O address space, so no memory address space is available (figure 2.5). The task file registers are assigned to the I/O address space and the configuration registers and card information structure (CIS) cannot be seen from the host.

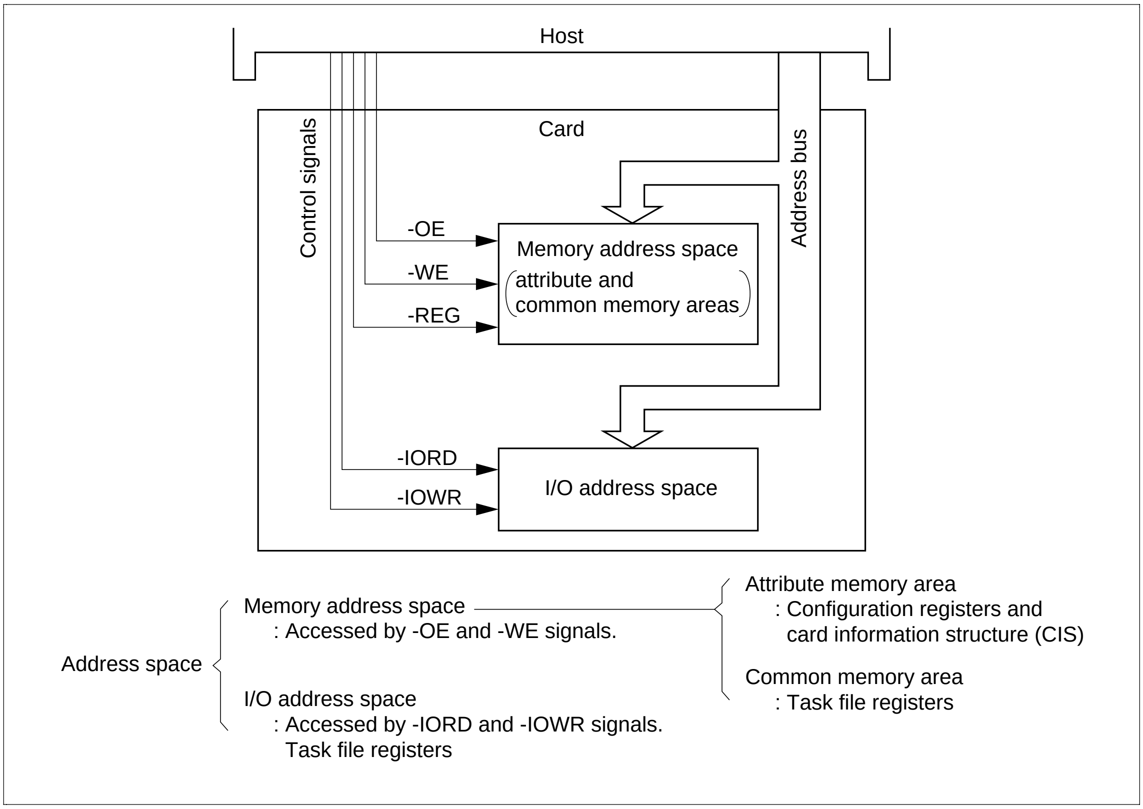


Figure 2.4 PC card ATA Specification Address Space

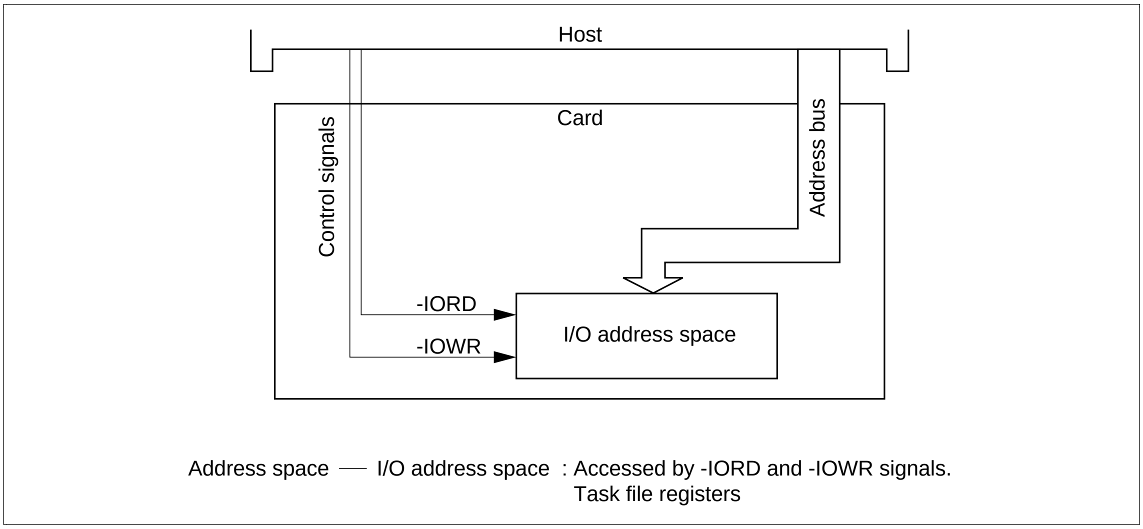


Figure 2.5 True-IDE Specification Address Space

2.4 Card Mode

Reading from or writing to the host is executed by transmitting ATA commands to the task file register (see figure 2.6). The data in the data area is also transmitted via the task file register. The host cannot directly communicate data with the card data area. This method is common to both PC card ATA and True-IDE specifications.

With the PC card ATA specification, the task file registers are assigned to the common memory area or the I/O address space. The memory card mode refers to the status when it is assigned to the common memory area and the I/O card mode the status when it is assigned to the I/O address space. The I/O card mode is further divided into three mapping modes (contiguous I/O, primary I/O and secondary I/O mapping modes) depending on which address the task file registers are assigned to.

True-IDE specification only has I/O address space, to which the task file registers are assigned. This card mode is called the "True-IDE mode", which has only one mapping mode. Table 2.3 summarizes the relationship between the above card modes and task file registers assignment.

Chapter 3 explains (1) configuration registers, (2) card information structure (CIS), (3) task file registers and (4) card mode in detail. Chapter 4 explains (5) power up sequence after inserting the card in the slot and (6) data transfer protocol, and Chapter 5 explains (7) default format.

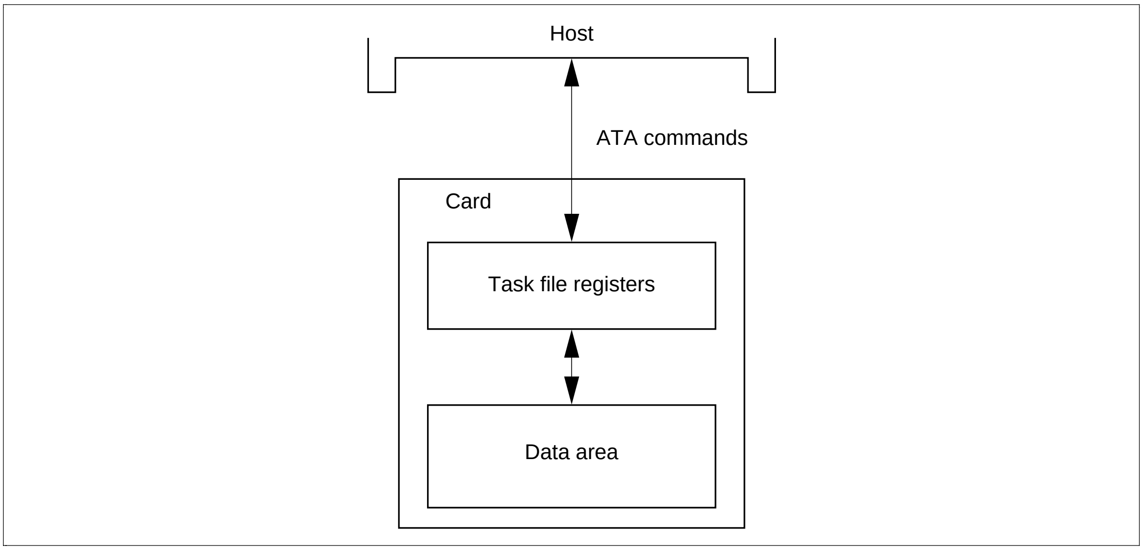


Figure 2.6 Task File Registers

Table 2.3 Card Mode

Interface specification	Card mode	Task file registers space (mapping mode)
PC card ATA specification	Memory card mode	Common memory area (memory map)
	I/O card mode	I/O address space (contiguous I/O map) (primary I/O map) (secondary I/O map)
True-IDE specification	True-IDE mode	I/O address space (True-IDE mode I/O map)

Section 3 Internal Card Configuration and Card Mode

3.1 Configuration Registers

The host is designed to set the PC card operatign environment according to its own configuration after the PC card is inserted. Hitachi flash cards have the following four configuration registers.

1) Configuration option register
2) Configuration status register
3) Pin replacement register
4) Socket copy register

The sizes of these registers, assigned at even addresses to the attribute memory area, are 1 byte. These addresses are specified by the base address written in TPCC_RADR in CIS and each register is allocated starting from base address "200H" to the next two added addresses (202H, 204H, ...). Figure 3.1 shows the configuration registers assignment.

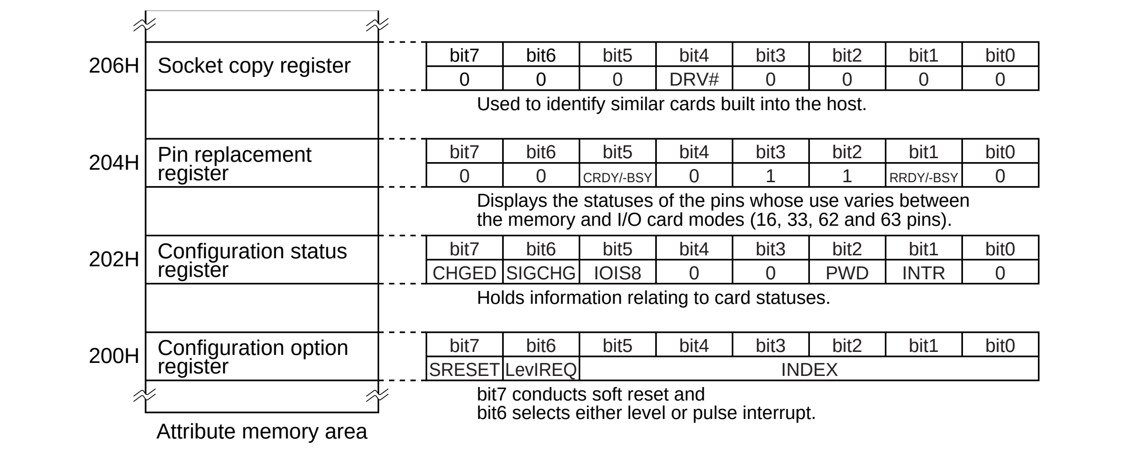


Figure 3.1 Configuration Registers

The configuration option register has three independent functions. The INDEX function indicated by bit5 to bit0 is explained here. "Configuration" refers to setting the operating environment for such modes as card and mapping. Either mode is selected after the host writes a value in INDEX. The card status corresponding to each INDEX value is described in the configuration entry tuple in CIS. For this purpose, the host needs to read CIS before configuration. Table 3.1 shows card and mapping modes corresponding to INDEX values. Refer to "3.3 Task File Registers" for mapping mode.

For other configuration functions, refer to the data sheet.

Table 3.1 Correspondence Between INDEX and Card Mode

INDEX							
bit5	**bit4**	**bit3**	**bit2**	**bit1**	**bit0**	**Card mode**	**Mapping mode**
0	0	0	0	0	0	Memory card mode	memory map
0	0	0	0	0	1	I/O card mode	contiguous I/O map
0	0	0	0	1	0	I/O card mode	primary I/O map
0	0	0	0	1	1	I/O card mode	seconday I/O map

3.2 Card Information Structure (CIS)

Card Information structure (CIS) is assigned at even addresses to the attribute memory area the same as for configuration register. CIS forms information unit called a “tuple” and the first tuple starts from address “000H”. Each tuple holds data indicating the position of the next tuple (pointer to the next tuple) and is configured in chains. The last tuple is called the “End of list tuple”, indicating that there are no more tuples to follow.

As shown in figure 3.2, each tuple starts from the tuple ID and next tuple pointer data, followed by unique data.

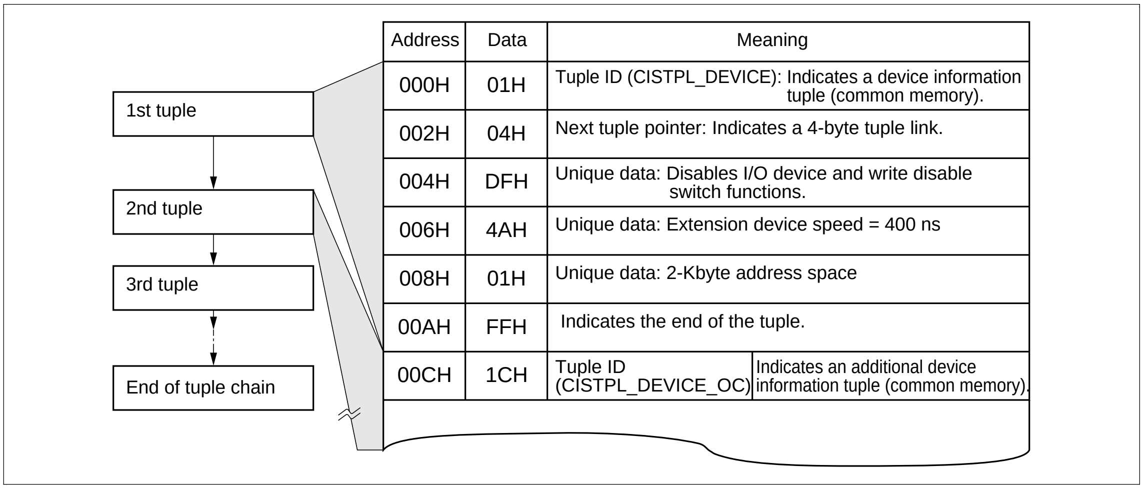


Figure 3.2 CIS Configuration and Tuple Format

CIS information is required when the host recognizes or configures card. Table 3.2 shows the following typical tuples.

1) Device information tuple: Describes device speed, type and capacity.
2) Function class ID tuple: Information relating to card manufacturer.
3) Level 1 version/product information tuple: Contains information on manufacturer, etc.
4) Function class ID tuple: Describes card function information.
5) Configuration tuple: Describes the position and contents of the configuration register.
6) Configuration entry tuple: Describes card configuration and its variation.

The INDEX value of TPCE_INDEX in the configuration entry tuple corresponds to the value to be written in INDEX of the configuration optional register. The configuration of the card when writing this value is described in the configuration entry tuple. Table 3.2 shows a typical configuration entry tuple in the memory card mode at a power supply voltage of 5 V. There are other tuples in the memory card mode at a power supply voltage of 3.3 V and in the I/O card mode at a power supply voltage of 5 V or 3.3 V.

Table 3.2 Typical CISs

Address	Tuple	Contents		Description
000H to	Device information	TPL_CODE = 01H		Tuple ID = 01H
00AH	tuple	TPL_LINK = 04H		Next tuple pointer = 04H
	(common memory) CISTPL_DEVICE	Device ID = DFH	Device type = DH	I/O device
			WPS = 1H	Write disable switch function disabled
			Device speed = 7H	Extension device speed enabled
		Extended speed = 4AH		Extension device speed = 400 ns
		Device size = 01H		2-Kbyte address space
		List end marker = FFH		End of tuple
020H to	Manufacture ID tuple	TPL_CODE = 20H		Tuple ID = 20H
02AH	CISTPL_MANFID	TPL_LINK = 04H		Next tuple pointer = 04H
		TPLMID_MANF = 0007H		Manufacture ID cord = 0007H (Hitachi)
		TPLMID_CARD = 0000H		Manufacture information = 0000H

Table 3.2 Typical CISs (cont.)

Address	Tuple	Contents		Description
02CH to 058H	Level 1 version/ product information tuple	TPL_CODE = 15H		Tuple ID = 15H
		TPL_LINK = 15H		Next tuple pointer = 15H
		TPLLV1_MAJOR = 04H		Basic compatible layer (layer 1) complies with the PCMCIA2.0/ JEIDA4.1 standards.
	CISTRPL_VERS_1	TPLLV1_MINOR = 01H		
		Manufacturer name string = "HITACHI"		Indicates the third-generation Hitachi flash card.
		Product name string = "FLASH"		
		Additional info = "3.0"		
		List end marker = FFH		End of tuple
05AH to 060H	Function class ID tuple	TPL_CODE = 21H		Tuple ID = 21H
		TPL_LINK = 02H		Next tuple pointer = 02H
	CISTPL_FUNCID	TPLFID_FUNTION = 04H		PC card ATA
		System initialization byte = 01H	Reserve = 0H	Reserved
			R = 0H	No BIOS ROM
			P = 1H	Configuration processed at power-on self test
074H to 080H	Configuration tuple	TPL_CODE = 1AH		Tuple ID = 1AH
	CISTPL_CONF	TPL_LINK = 05H		Next tuple pointer = 05H
		TPCC_SZ = 01H	TPCC_RFSZ = 0H	Reserved
			TPCC_RMSZ = 0H	This value + 1 is equal to byte count of TPCC_RSVD field.
			TPCC_RASZ = 1H	This value + 1 is equal to byte count of TPCC_RADR field.
		TPCC_LAST = 03H		Last index No. = 03H
		TPCC_RADR = 0200H		Configuration register base address = 0200H
		TPCC_RMSK = 0FH		4 configuration registers exist.

Table 3.2 Typical CISs (cont.)

Address	Tuple	Contents		Description
082H to 094H	Configuration entry tuple CISTPL_CFTABLE_ENTRY	TPL_CODE = 1BH		Tuple ID = 1BH
		TPL_LINK = 08H		Next tuple pointer = 08H
		TPCE_INDX = C0H	I = 1H	Followed by interface description field
			D = 1H	Default setting
			INDEX = 00H	Memory card INDEX
		TPCE_IF = C0H	W = 0H	WAIT signal not used
			R = 1H	Ready/busy signal enabled
			P = 0H	WP signal not used
			B = 0H	BVD1 and BVD2 signals not used
			IF type = 0H	Memory interface
		TPCE_FS = A1H	M = 1H	Other function information remains.
			MS = 1H	Memory address space mapping specified by 2 bytes
			IR = 0H	Interrupt not used
			IO = 0H	IO space not used
			T = 0H	No timing-related setting
			P = 1H	Only information describing VCC conditions exists.
		TPCE_PD = 01H	NV = 1H, other = 0	Parameter selecting byte of standard operating power supply voltage
		VCC normal value = 55H		Standard operating power supply voltage = 5 V
		TPCE_MS = 0008H		Memory space window size = 2 Kbyte
		TPCE_MI = 20H	X = 0H	End of extension byte
			R = 0H	Reserved
			P = 1H	Supports power-down mode.
			RO = 0H	No read-only
			A = 0H	Audio function not used
			T = 0H	Only one card can be set the same.

3.3 Task File Registers

Data is transferred between the host and the card and the transfer controlled via the task file registers. The task file registers refer to the following series of registers.

1) Data register
2) Error register
3) Feature register
4) Sector count register
5) Sector number register
6) Cylinder low register
7) Cylinder high register
8) Drive head register
9) Status register
10) Alternate status register
11) Command register
12) Device control register
13) Drive address register

These registers are divided into five mapping modes ((1) memory mapping, (2) primary I/O mapping, (3) secondary I/O mapping, (4) contiguous I/O mapping and (5) True-IDE mode I/O mapping) according to the address spaces to which these registers are assigned. The mapping mode is selected after the host writes a value in INDEX of the configuration optional register. Each mapping mode is explained below.

In the memory mapping mode, the task file registers are assigned to the common memory area (see figure 3.3 below). As described in CIS (TPCE_FA and TPCE_MS of the configuration entry tuple), the memory window size is set at 2 Kbyte and the card base address at “0H”. This window can be mapped to any address in the memory address space of the host. The position of the task file registers is determined by the offset address from the card base address. The 1-Kbyte memory window from offset “400H” to “7FFH” is secured for the host to access the data register during block transfer from memory to memory. Since this 1-Kbyte memory window accesses FIFO, data cannot be accessed randomly.

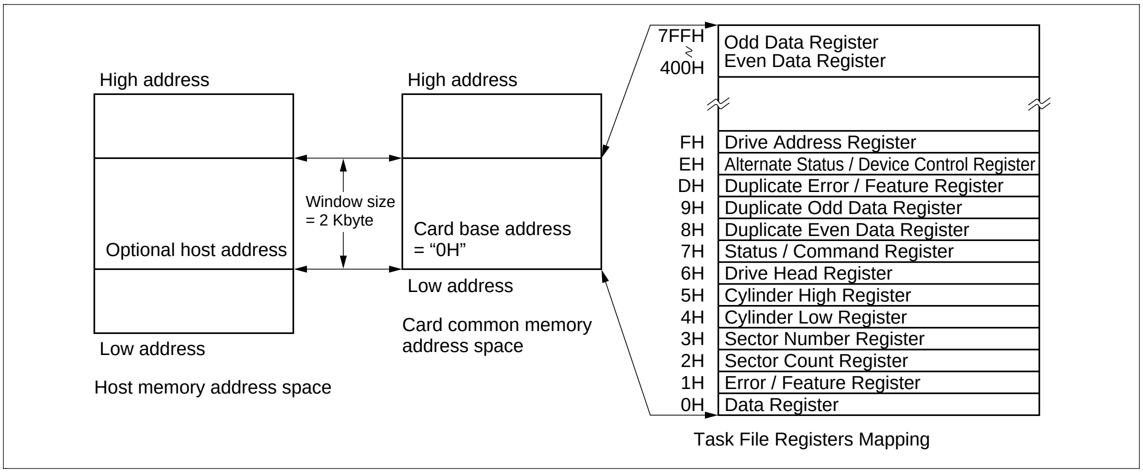


Figure 3.3 Memory Mapping Mode

In the primary or secondary I/O mapping mode, the register functions as the I/O card to be accessed via "1F0H" to "1F7H" and "3F6H " to "3F7H" (primary) or "170H " to "177H" and "376H" to "377H" (secondary) in the standard I/O address space. Address signals of A9 to A0 are used for access and A10 neglected.

In the contiguous I/O mapping mode, only four address signals of A3 to A0 in the I/O address space are decoded. Thanks to this function, those other than A3 to A0 can be accessed via any address although host operation is required.

Table 3.3 shows task file registers mapping in the I/O card mode. The contiguous I/O mapping mode has the data and error/feature registers as well as the duplicate even data, duplicate odd data and duplicate error/feature registers. The data register can be accessed as 16-bit data combining 8-bit data indicated by an even address and 8-bit data indicated by an odd address. Since the data register overlaps the error/feature register when handled as 16-bit data, registers duplicating them are equipped.

Table 3.3 Task File Registers Mapping at I/O Card Mode

Primary I/O map A9 to A0	Secondary I/O map A9 to A0	Contiguous I/O map A3 to A0	Task file register
1F0H	170H	0H	Data register
1F1H	171H	1H	Error/feature register
1F2H	172H	2H	Sector count register
1F3H	173H	3H	Sector number register
1F4H	174H	4H	Cylinder low register
1F5H	175H	5H	Cylinder high register
1F6H	176H	6H	Drive head register
1F7H	177H	7H	Status/command register
—	—	8H	Duplicate even data register
—	—	9H	Duplicate odd data register
—	—	DH	Duplicate error/feature register
3F6H	376H	EH	Alternate status/device control register
3F7H	377H	FH	Drive address register

In the True-IDE mode I/O mapping mode, only three address signals of A2 to A0 in the I/O address space are decoded as shown in table 3.4, and the -CE2 signal is used to select the alternate status/device control or drive address register and the -CE1 to select other task file registers.

Table 3.4 Task File Registers Mapping at True-IDE Mode

-CE2	-CE1	True-IDE Mode I/O map A2 to A0	Task file register
1	0	0H	Data register
1	0	1H	Error/feature register
1	0	2H	Sector count register
1	0	3H	Sector number register
1	0	4H	Cylinder low register
1	0	5H	Cylinder high register
1	0	6H	Drive head register
1	0	7H	Status/command register
0	1	6H	Alternate status/device control register
0	1	7H	Drive address register

3.4 Card Mode

Table 3.5 summarizes card modes. In the memory card mode, the host configures the card using CIS and the configuration registers and communication between the host and the card are conducted by the task file registers mapped in the 2-Kbyte window in the memory address space.

In the I/O card mode, configuration is conducted in the same way as in the memory card mode and the task file registers are mapped to the I/O address space.

The True-IDE mode does not have configuration function and the task file registers are mapped in the I/O address space selected by address signal A2 to A0, -CE2 and -CE1.

Table 3.5 Card Mode

Card mode	Configuration registers and CIS	Task file registers
Memory card mode	Exists in the attribute area in the memory address space.	Exists in the common memory area in the memory address space.
I/O card mode	Exists in the attribute area in the memory address space.	Exists in the I/O address space.
True-IDE mode	None	Exists in the I/O address space.

Section 4 Power Up Sequence and ATA Commands

4.1 Power up Sequence

Figure 4.1 shows the flow overview from inserting the card to determining the card mode. Since hot insertion is supported in the memory or I/O card mode, the card can be inserted after the host power is turned on. In the True-IDE mode, the host power should be turned on after the card is inserted. In either mode, power-on is reset by the reset signal first generated by the reset IC built into the card. During card default processing after the above operation, the ATA select (-OE(-ATASEL)) pin level is detected and interface specification determined (PC card ATA or True-IDE specification).

There are three types of the card pin lengths in order to support hot insertion in PC card ATA specification (see table 4.1). After inserting the card in the slot, the power source and the ground pin reconnected first and the card detection pins (-CD1 and-CD2) last. Since -CD1 and -CD2 are connected to the ground inside the card, the host can detect card insertion.

When the card is set in PC card ATA specification, the host reads CIS from the card. At this time, power source voltage information is supplied to the host by the voltage sense pins (-VS1 and -VS2). In order to indicate that CIS can be read both at 5 V and 3.3 V, -VS1 is connected to the ground inside the card and -VS2 kept open.

The host is designed to recognize and configure the card based on the CIS information read. Recognizing the card means determining the type, manufacturer, system resource to be used (I/O address, IRQ signal and memory window) and the kind of card. The host adjusts and assigns the system resource to be used so as not to compete with other devices and sets an appropriate value in the configuration registers (card configuration). The card mode is determined by the value to be set in INDEX of the configuration optional register.

In the True-IDE specification, two connections, namely, the master and slave drives, are allowed. The drive is identified using the card select (-CSEL) pin level, followed by default processing. In this way, the True-IDE mode is determined only by the states of the -OE(-ATASEL) and -CSEL pins.

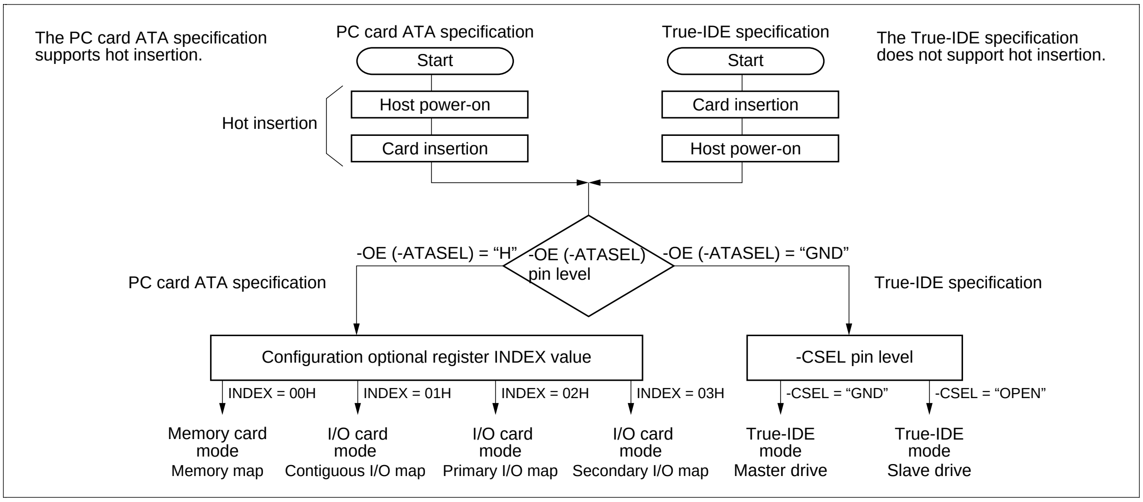


Figure 4.1 Power up Sequence and Card Mode

Table 4.1 Pin Length

Pin type	Pin length
Power and ground pins (VCC and GND)	5.00 ± 0.10 mm
Card detection pins (-CD1 and -CD2)	3.50 ± 0.10 mm
Other signal pins	4.25 ± 0.10 mm

Figure 4.2 shows the timing chart at power-on. Card insertion is detected when the -CD1 and -CD2 pins are turned to level "L", starting power (VCC) supply. If VCC has already been supplied before detected card, there is possibility that mode setting is disabled. In order to set the card mode, the -OE(-ATASEL) pin level has to be set before supplying VCC until resetting is completed. Setting the pin at level "H" sets the memory or I/O card mode and at "GND", the True-IDE mode.

In the True-IDE mode, the master and slave drives are identified by the -CSEL pin which is pulled up inside the card. The level of this pin must also be set before supplying VCC until resetting is completed the same as for the -OE(-ATASEL) pin. Setting it at level "L" sets the master drive and opening it sets the slave drive.

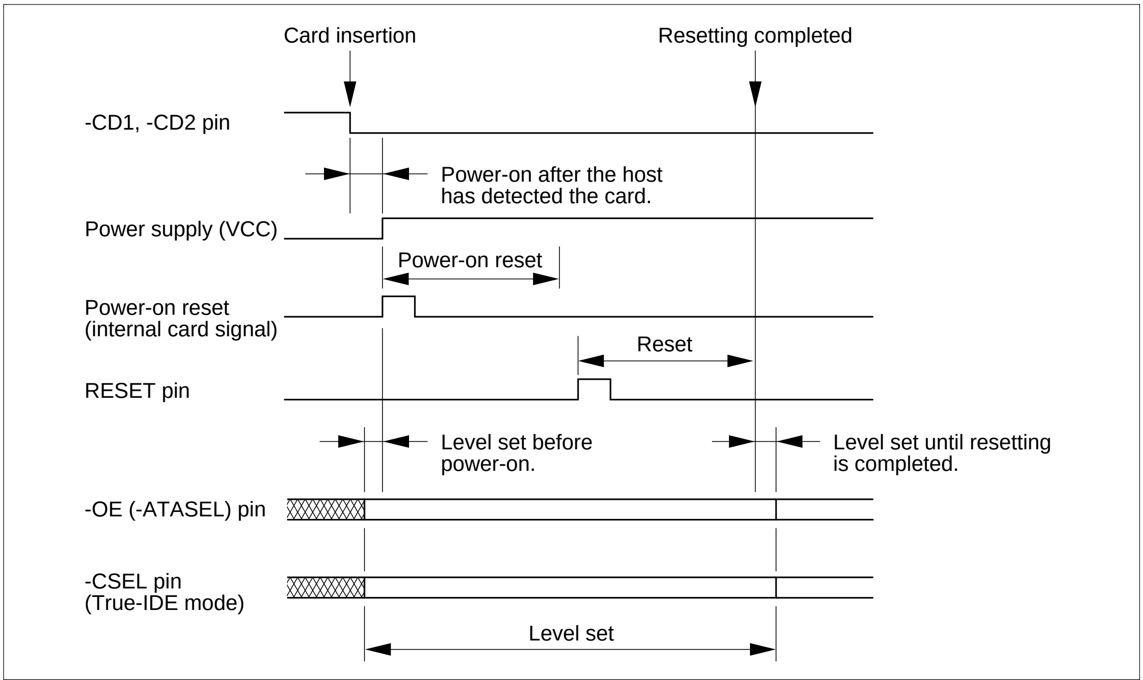


Figure 4.2 Timing Chart at Power-on

4.2 Host Configuration

Figure 4.3 (a) shows the host configuration in the memory or I/O card mode. The card inserted in the slot is connected to the PCMCIA controller (PCIC). The socket service provides the card service with an interface which is not dependent on PCIC. The card service has host system resource control functions and configures the card. The card service client driver corresponds to the device driver. After configuring the card, the operating system controls the card via this driver. The ATA commands used here are explained in the next section. The operating system provides the application program with general file operating functions.

In the True-IDE mode, no software corresponding to the socket and card services is available since there is no card recognition or configuration (figure 4.3 (b)). The card is also controlled using ATA commands in this mode as in the memory or I/O card mode.

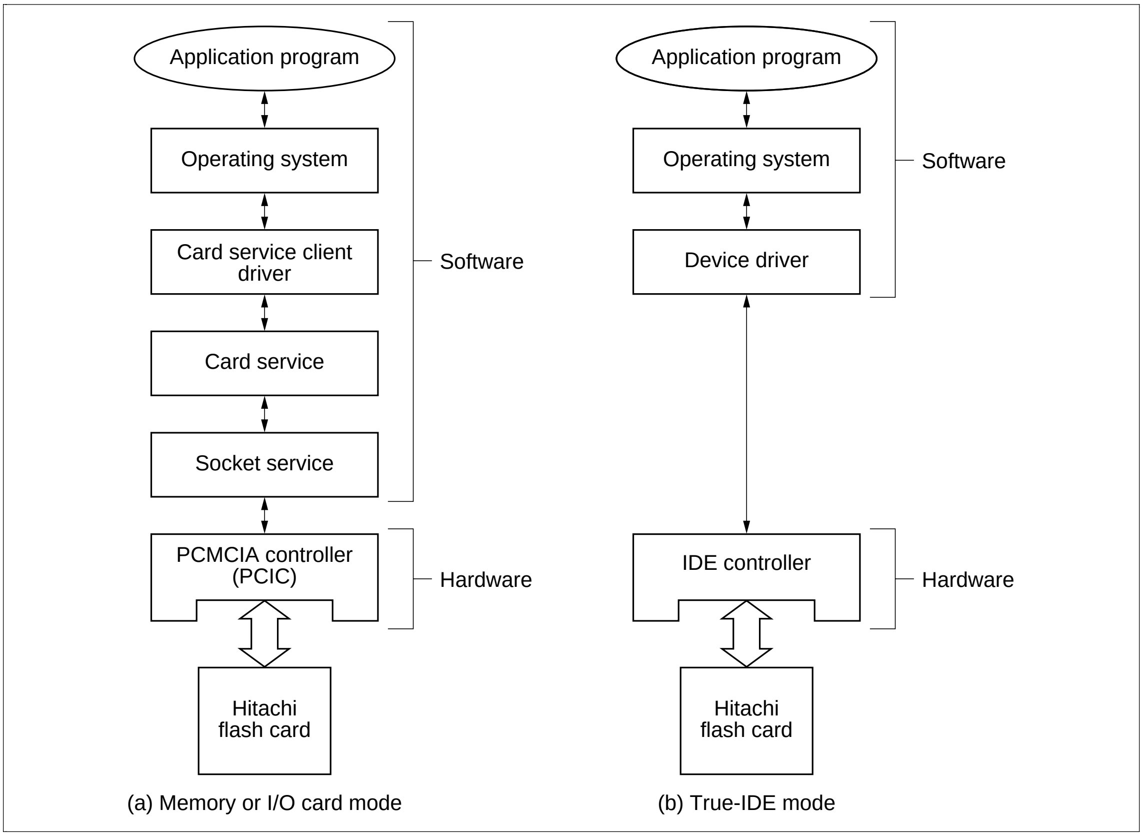


Figure 4.3 Host Configuration

4.3 ATA Commands

The task file registers are used to execute such functions as reading and writing of the Hitachi flash card. A command is executed by setting parameters relating to it in up to six task file registers and command codes in the command register in this order.

The modes for setting the card address are the cylinder·head·sector (CHS) and the logical block address (LBA) modes (refer to section 5 for these modes). Set bit6 (LBA) of the drive head register at “0” to select the CHS mode or “1” to select the LBA mode. Figures 4.4 and 4.5 show the CHS and LBA method command formats.

The Hitachi flash card supports 30 ATA commands. The read and write sector commands are explained in 4.4 and 4.5 as typical ATA commands.

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature Register	Features							
Sector Count Register	Sector count							
Sector Number Register	Sector No.							
Cylinder Low Register	Cylinder No. lower byte							
Cylinder High Register	Cylinder No. upper byte							
Drive Head Register	1	LBA = 0	1	DRV	Head No.			
Command Register	Command							

Feature register: Used when the host sets a particular function to the card. Available only for writing data and not for reading.
Sector count register: The host sets the number of sectors to transfer in this register. The default setting is "01H". The number of sectors are 256 when "00H" is set.
Sector number register: Sets the number of the sector where transfer starts.
Cylinder low register: Sets the lower 8 bits of the number of the cylinder where sector transfer starts.
Cylinder high register: Sets the upper 8 bits of the number of the cylinder where sector transfer starts.
Drive head register: Sets the LBA, DRV and head number. When LBA = 0, the cylinder head sector (CHS) mode is selected. The DRV bit is used for selecting the master or slave configuration. The card can be accessed when the DRV# bit of the socket and copy register is equal to this bit. Bit3 to bit0 are used to set the number of the head where sector transfer starts.

Figure 4.4 CHS Mode Command Format

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature Register	Features							
Sector Count Register	Sector count							
Sector Number Register	Logical block address A07 to A00							
Cylinder Low Register	Logical block address A15 to A08							
Cylinder High Register	Logical block address A23 to A16							
Drive Head Register	1	LBA = 1	1	DRV	Logical block address A27 to A24			
Command Register	Command							

Sector number register: Sets the address of the logical block (A07 to A00) where sector transfer starts.
Cylinder low register: Sets the address of the logical block (A15 to A08) where sector transfer starts.
Cylinder high register: Sets the address of the logical block (A23 to A16) where sector transfer starts.
Drive head register: When LBA = 1, the logical block address (LBA) mode is selected. Bit3 to bit0 are used to set the address of the logical block (A27 to A24) where sector transfer starts.

Figure 4.5 LBA Mode Command Format

4.4 Read Sector(s) Command Procedure

The read sectors(s) command is designed to transfer data of the 1 to 256 sectors set by the sector count register in the sector set by the sector number register from the card to the host. Figure 4.6 summarizes the read sector(s) command procedure for the card set in the I/O card mode contiguous I/O map. First, set values in the upper and lower bytes of the cylinder number, the sector count and number, and the drive head registers. The feature register needs not to be set since it is not referred to. The host sets “20H” in the command register to request command execution. The card sets the BSY in the status register at “1” after receiving the command. See figure 4.7 for the status register. When BSY = 1, internal card processing is executed. After the processing has been completed, BSY turns to 0 and DRDY, DSC and DRQ to 1 to enable data transfer, indicating that access from the host becomes available. In short, the host waits until the status register value turns from “80H” to “58H”. After this, the host reads data in the data register 256 times. Each access of word, byte or odd number byte is available for the data register. Figure 4.6 shows a typical case where 512-byte data is transferred by 256 word reads. The status register turns to “50H” after data transfer is completed, waiting for a next command.

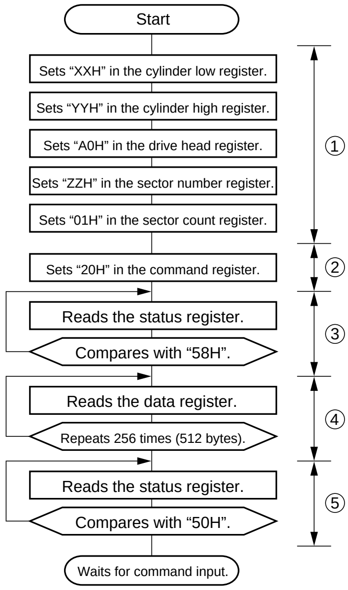
Address		Read -IORD = L	Write -IOWR = L
A10 to A4	A3 to A0		
×	4H	Cylinder Low Register	Cylinder Low Register
×	5H	Cylinder High Register	Cylinder High Register
×	6H	Drive Head Register	Drive Head Register
×	3H	Sector Number Register	Sector Number Register
×	2H	Sector Count Register	Sector Count Register
×	7H	Status Register	Command Register

A10 to A4 are optional addresses.

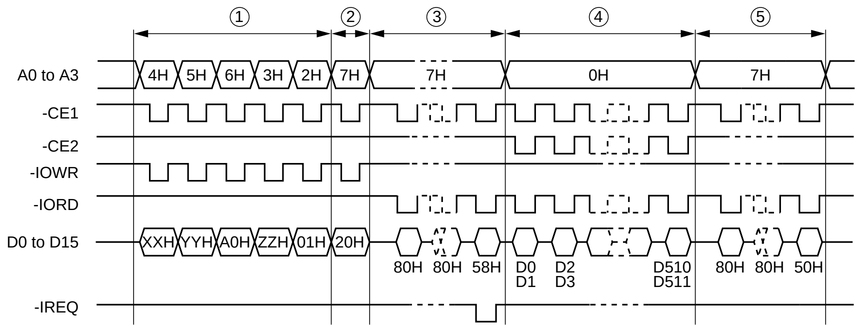
(a) Task File Register Mapping in Contiguous I/O Map

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature Register	———							
Sector Count Register	Sector count = 01H							
Sector Number Register	Sector No. = ZZH							
Cylinder Low Register	Cylinder No. lower byte = XXH							
Cylinder High Register	Cylinder No. upper byte = YYH							
Drive Head Register	1	LBA = 0	1	DRV = 0	Head number = 0H			
Command Register	Command = 20H							

(b) Command Format



(c) Flow Chart



(d) Timing Chart

Figure 4.6 Read Sector(s)

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Status Register	BSY	DRDY	DWF	DSC	DRQ	CORR	IDX	ERR

BSY (busy): Set at “1” during internal card processing.
DRDY (drive ready): Set at “1” after internal card processing has been completed and the drive has become ready for receiving access from the host.
DWF (drive write fault): Set at “1” when a write fault occurs inside the card.
DSC (drive seek complete): Set at “1” after drive seek has been completed.
DRQ (data request): Set at “1” after data transfer between the host and the data register has become ready.
CORR (corrected data): Set at “1” after an error occurring during internal card processing has been corrected.
IDX (index): Always set at “0”.
ERR (error): Set at “1” when an error occurs during processing according to the input command.
This bit is cleared after a next command is input.

Figure 4.7 Status Register

4.5 Write Sector(s) Command Procedure

The write sector(s) command is designed to transfer data of the 1 to 256 sectors set by the sector number register in the sector set by the sector count register from the host to the card. As in the previous section, figure 4.8 summarizes the write sector(s) command procedure for the card set in the I/O card mode contiguous I/O map. First, set values in the upper and lower bytes of the cylinder number, the sector count and number, and the drive head register. The host sets “30H” in the command register to request command execution. The card sets the BSY in the status register at “1” after receiving the command. After internal processing has been completed, BSY turns to 0 and DRDY, DSC and DRQ to 1 to enable data transfer, indicating that access from the host becomes available. After this, the host writes data in the data register 256 times. Each access of word, byte or odd number byte is available for the data register. Figure 4.8 shows a typical case where 512-byte data is transferred by 256 word writes. The status register turns to “50H” after data transfer is completed, waiting for a next command.

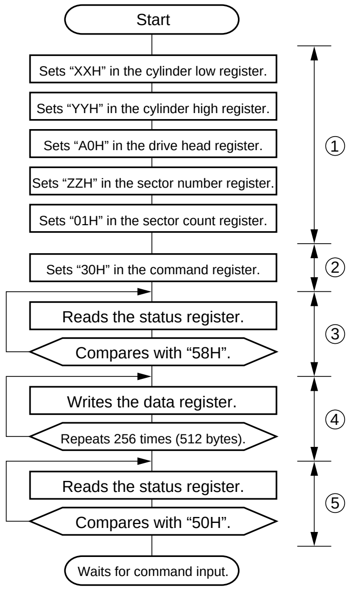
Address		Read	Write
A10 to A4	A3 to A0	-IORD = L	-IOWR = L
×	4H	Cylinder Low Register	Cylinder Low Register
×	5H	Cylinder High Register	Cylinder High Register
×	6H	Drive Head Register	Drive Head Register
×	3H	Sector Number Register	Sector Number Register
×	2H	Sector Count Register	Sector Count Register
×	7H	Status Register	Command Register

A10 to A4 are optional addresses.

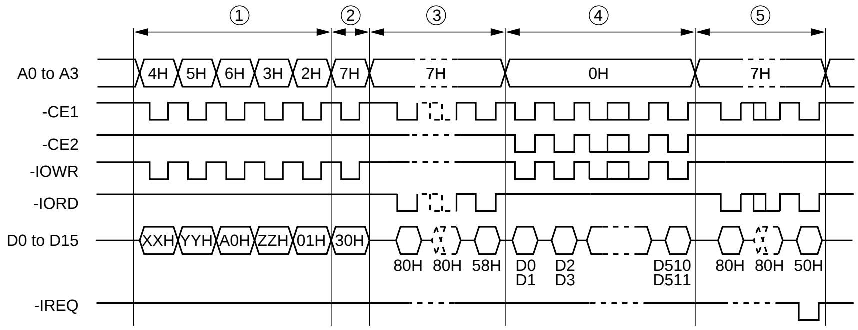
(a) Task File Register Mapping in Contiguous I/O Map

	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
Feature Register	—							
Sector Count Register	Sector count = 01H							
Sector Number Register	Sector No. = ZZH							
Cylinder Low Register	Cylinder No. lower byte = XXH							
Cylinder High Register	Cylinder No. upper byte = YYH							
Drive Head Register	1	LBA = 0	1	DRV = 0	Head number = 0H			
Command Register	Command = 30H							

(b) Command Format



(c) Flow Chart



(d) Timing Chart

Figure 4.8 Write Sector(s)

Section 5 Format

5.1 Cylinder, Head and Sector

Since the Hitachi flash cards have one or some built-in flash memories, no physical configuration is required for the hard disk cylinders, headers and sectors. Since it is controlled using the ATA commands like the hard disk, the same concept as for the disk also applies to the card format. Before explaining the format, the concept of the cylinders, heads and sectors and the logical block address (LBA) for specifying the sector address are explained.

The third-generation 8-Mbyte Hitachi flash card has one built-in 64-Mbit Hitachi flash memory. The data in this flash memory is read and written in 512-byte units. This unit is called a “sector” and one flash memory has 15,744 sectors for reading and writing. In addition to these sectors, the memory has an alternative sector to be replaced with the sector which has failed during operation.

The 15-Mbyte card has two flash memories and the 30-Mbyte type has four.

Figure 5.1 (b) shows the concept of the hard disk cylinders, heads and sectors for a third-generation 8-Mbyte card. The size of one sector is determined by the flash memory built in the card as follows:

1 sector = 512 bytes

Considering that tracks are arranged concentrically around the disk, assume as follows:

1 track = 32 sectors

Also assume that data is recorded on both surfaces of the disk, and the front surface is accessed by head 0 and the back surface by head 1. Since the tracks located away from the center by the same distance are called a “cylinder”, one cylinder contains the same number of tracks as that of heads.

1 cylinder = 2 heads × 1 track = 2 heads × 32 sectors

Assuming that the number of cylinders is 246, the total number of sectors is as follows:

Total number of sectors = 246 cylinders × 2 heads × 32 sectors = 15,744

This equals to the number of sectors built in one flash memory.

Assuming that a 15-Mbyte card has two disks, or four heads, the total number of sectors is as follows:

Total number of sectors = 246 cylinders × 4 heads × 32 sectors = 31,488

Assuming that a 30-Mbyte card has four heads, or 492 cylinders, the total number of sectors is as follows:

Total number of sectors = 492 cylinders × 4 heads × 32 sectors = 62,976

The numbers of the bytes, cylinders and heads per sector of each byte count card are described in the identify drive information which can be read using the ATA command.

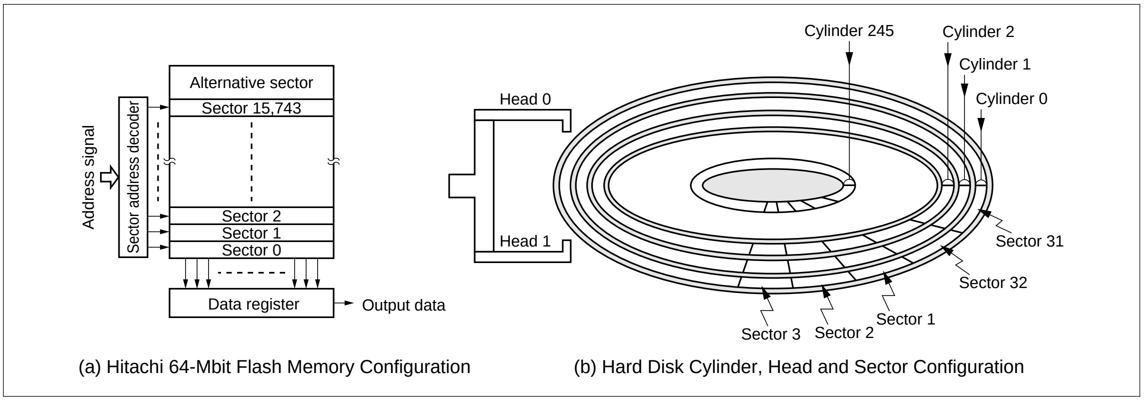


Figure 5.1 Memory Configuration of Third-generation 8-Mbyte Flash Card

5.2 Logical Block Address (LBA) Mode

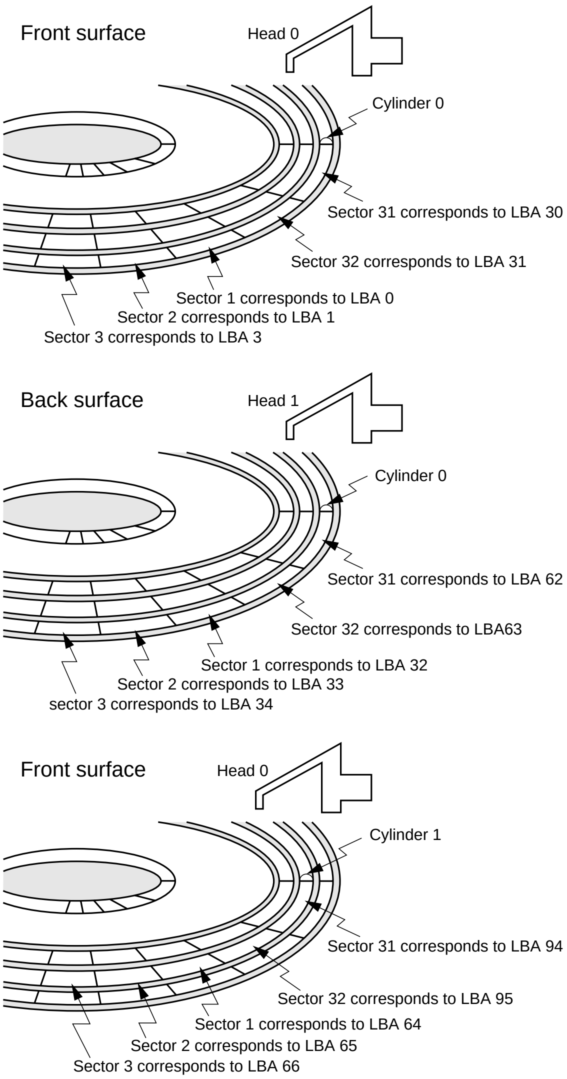
Both cylinder head sector address (CHS) and logical block address (LBA) mode can be selected using ATA commands. Figure 5.2 shows the correspondence between both modes. The figure refers to a third-generation 8-Mbyte card the same as in the previous section. With the CHS mode, each sector assigned to the front and back surfaces of the disk is selected using the cylinder, head and sector numbers. With the LBA mode, the first sector address is set as "block 0" and the following sectors are serially numbered.

A general conversion formula from CHS to LBA is as follows:

$$\text{LBA} = (\text{Cylinder No.} \times \text{Number of heads} + \text{Head No.}) \times \text{Number of sectors} + \text{Sector No.} - 1$$

Since the number of heads = 2 and that of sectors =32 for the 8-Mbyte card in figure 5.2:

$$\text{LBA} = (\text{Cylinder No.} \times 2 + \text{Head No.}) \times 32 + \text{Sector No.} - 1$$



Correspondence Between CHS and LBA

Address specification with CHS mode			Address specification with LBA mode
Cylinder No.	Header No.	Sector No.	Block No.
0	0	1	0
0	0	2	1
0	0	3	2
≈	≈	≈	≈
0	0	31	30
0	0	32	31
0	1	1	32
0	1	2	33
0	1	3	34
≈	≈	≈	≈
0	1	31	62
0	1	32	63
1	0	1	64
1	0	2	65
1	0	3	66
≈	≈	≈	≈
1	0	31	94
1	0	32	95
≈	≈	≈	≈
245	1	31	15,742
245	1	32	15,743

Figure 5.2 Logical Block Address Mode for Third-generation 8-Mbyte Flash Card

5.3 Formatting

The hard disk is formatted by the following three procedures.

(1) Low-level formatting
(2) Partition setting
(3) Partition formatting

Low-level formatting refers to preparing tracks on the disk and dividing them into sectors, partition setting to dividing the hard disk into areas called "partitions" and partition formatting to preparing operating system boot information and data areas.

The above three procedures can apply also to formatting of the Hitachi flash cards. Since the card has a built-in flash memory and the sector address and size has already been determined, it can be assumed that low-level formatting has already been completed and thus cannot be changed.

For the Hitachi flash cards, a partition is created before shipment, followed by formatting. When using the card, partition setting and formatting can be changed. Before explaining partition, the FAT file system is simply explained.

5.4 FAT File System

The FAT file system is adopted by MS-DOS* and some other operating systems.

Although the sector is the minimum unit for reading from and writing to the hard disk, this file system combinedly controls several sectors, called a "cluster". The file area (area for storing files) is divided into clusters to secure "entries", which correspond to each cluster one by one. All entries are located in the file allocation table (FAT) and data stored in each entry indicates cluster combination and usage conditions. The 12-bit FAT refers to the case when these entries are 12 bits and the 16-bit FAT to the case when these entries are 16 bits.

The size of the root directory area, where files and directory entries can be stored, is determined at formatting. Directory entries refer to 32-byte data which indicates such information as file name and attribute.

5.5 Partition Setting

Figure 5.3 shows the partition default settings of the third-generation 8-Mbyte card. Data called the "master boot record (MBR)" is written in the first sector (LBA = 0) of the card. The partition entry which describes the partition type, size and the kind is included in the MBR. The type in figure 5.3 forms one partition of the specified size from LBA = 32 to LBA = 15,679, called "MS-DOS 12-bit BPB/FAT". The size and type differ depending on the card capacity.

* MS-DOS is resistered by Microsoft.

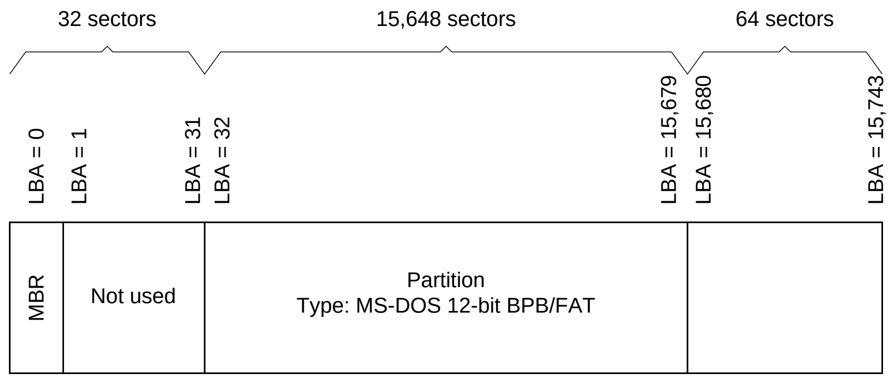


Figure 5.3 Third-generation 8-Mbyte Flash Card Partition

5.6 Partition Formatting

The third-generation 8-Mbyte card has one partition of the MS-DOS 12-bit BPB/FAT type. After formatting this partition, data called the "partition boot record (PBR)" is written in the first sector of the partition and information called the "BIOS parameter block (BPB)" is described in the PBR, where the following information is described:

(1) Number of sectors per cluster
(2) Number of sectors per FAT
(3) Number of FATs
(4) Number of directory entries storable in the root directory area

FATs are written in the sectors following where PBRs are written, and the root directory area is secured in the sectors following the above sectors.

The default settings of the 8-Mbyte card are as follows: (1) number of sectors per cluster = 8; (2) number of sectors per FAT = 6; (3) number of FATs = 2; and (4) number of directory entries storable in the root directory area = 512. Following PBRs, two FATs of 6 sectors each are written. Since the FAT is 12 bits, each cluster in the file area is specified in 12-bit units. For the root directory entry area, 32 sectors are secured so as to store 512 32-bit root directory entries (see figure 5.4).

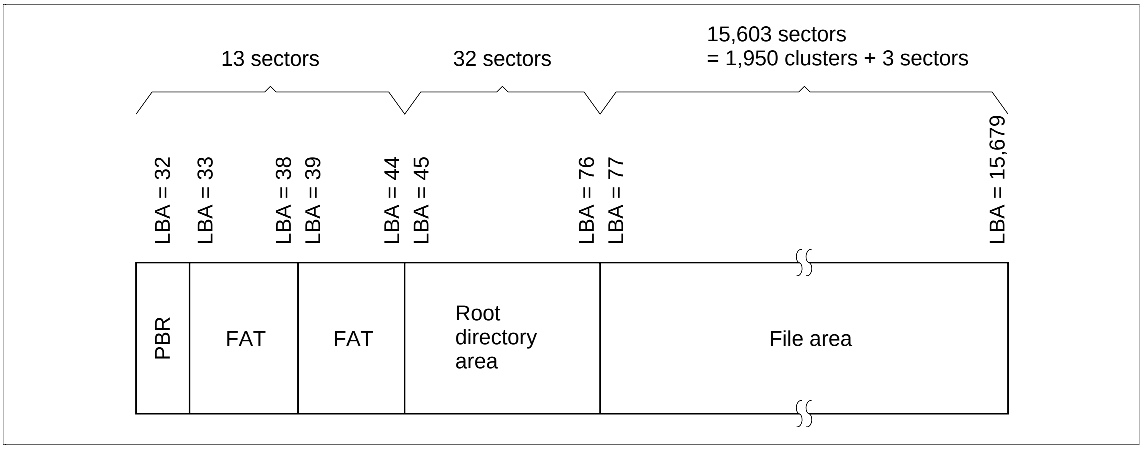


Figure 5.4 Third-generation 8-Mbyte Flash Card Partition Configuration

5.7 Memory Density After Formatting

The Hitachi flash cards partition has already been formatted before shipment. The file area as shown in figure 5.4 is displayed as the all disk area when checking the card memory space of this state using functions like the MS-DOS CHKDSK command. Since 8 sectors = 1 cluster for the third-generation 8-Mbyte card, the file area is as follows:

File area = 15,679 – 76 sectors = 15,603 sectors = 1,950 clusters + 3 sectors

And accordingly:

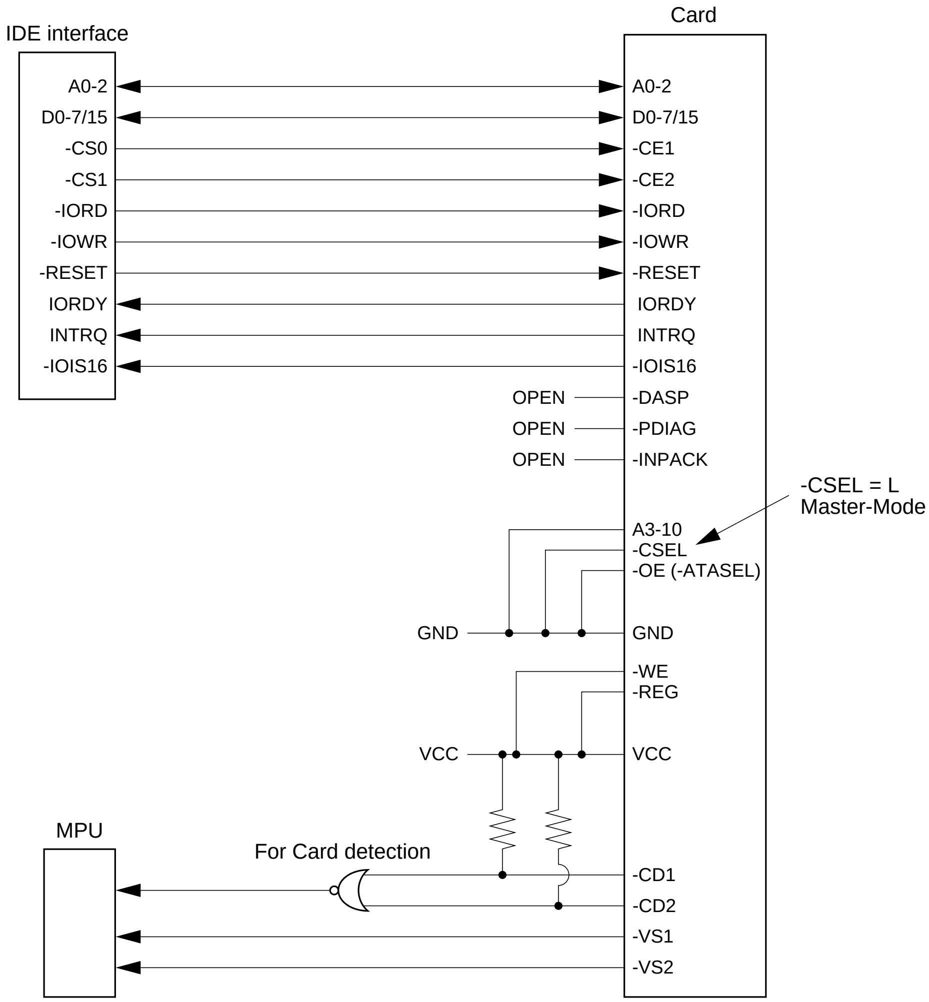
All disk area = 1,950 clusters × 8 sectors × 512 bytes = 7,987,200 bytes

Appendixes

A. Pin Connection in True-IDE Mode

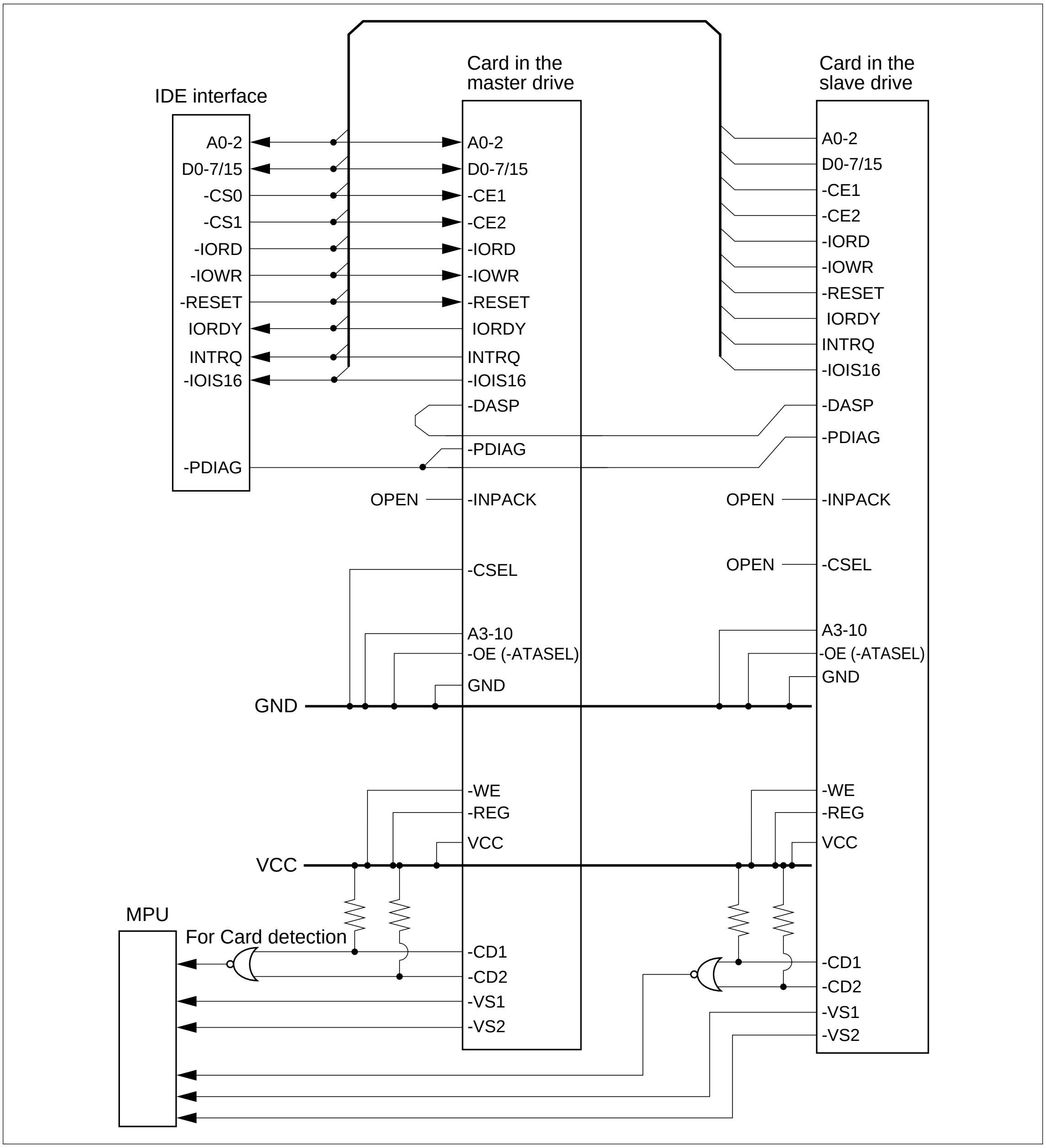
There are two ways of using the Hitachi flash cards in the True-IDE mode, namely, using only one card as the master drive and using two cards as the master and slave drives. Pin connection in each method is described below.

(1) Pin connection when only one card is used as the master drive. (example)



Note: In this case slave drive should not be accessed.

(2) Pin connection when two cards are used as the master and slave drives. (example)



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B. Typical Questions and Answers

(1) What will happen if power break occurs during writing?

Although no physical damage is applied to the chip (no chip or sector breakage), a logical error occurs in the corresponding sector, disabling written data. If the failed sector belongs to a file, the file may seem to break. It can be reused after formatting it again.

(2) How does the reading or writing procedure differ between the cylinder head sector address (CHS) and logical block address (LBA) mode?

Set bit6 of the drive head register (one of the task file registers) at “0” to select the CHS mode or “1” to select the LBA mode. The sector where transfer starts is specified as follows for each mode:

Task file register	CHS mode	LBA mode
Sector number register	Sector No.	Logical block address (A07 to A00)
Cylinder low register	Cylinder No. lower 8 bits	Logical block address (A15 to A08)
Cylinder high register	Cylinder No. upper 8 bits	Logical block address (A23 to A16)
Bit3 to bit0 of drive head register	Head No.	Logical block address (A27 to A24)

(3) Can data be written starting from the middle of a sector?

No. Writing is available only in 1-sector units.

(4) Data of more than 512 bytes can be written at one time?

As many number of sectors as specified by the sector count register can be written when executing the “Write Sector(s)” command.

(5) Is a sector required to be erased before writing data?

Since executing the “Write Sector(s)” command erases the sector before writing data, no “Erase Sector(s)” command is required before executing the “Write Sector(s)” command.

(6) What state will be assumed after writing to the card has been interrupted?

The state to wait for data will be assumed until 512-byte data is transferred.

(7) How does the “Format Track” ATA command function?

Although the “Format Track” command of the hard disk is designed to reformat a track and initialize a data field, that of the Hitachi flash cards is a NOP command and thus conducts no operation.

(8) What is the difference between the “Read Long Sector” and “Read Sector(s)” ATA commands?

512-byte data is transferred by the “Read Sector(s)” command and 516-byte data by the “Read Long Sector” command. Since the latter command executes ECC in the host, four more bytes of data are transferred. Since the Hitachi flash cards internally execute ECC, however, no “Read Long Sector” command is required.