hcAT91 CPU card User Manual

Revision: 1.0

Introduction

The hcAT91 CPU card is a member of the H-Storm system CPU card family. The H-Storm project is a modular system-level design approach targeting hobby electronics, robotics and fast prototyping. The project defines a standard 72-pin connector as the interconnect between the various elements of the system with two optional 20-pin extension connectors. The elements of an H-Storm system are CPU cards, peripherial cards and system-boards. For detailed information on the H-Storm project please see the H-Storm System Manual available from the H-Storm website.

The hcAT91 CPU card is a standard H-Storm system component and is built around the ATMEL AT91R40008 microcontroller. That device integrates a 66MHz ARM7TDMI processor core with 256kBytes of on-chip SRAM and a wide set of peripherials. The processor employs a 32-bit internal and a 16-bit external bus architecture.

The CPU card combines this microcontroller with a 16-bit FLASH ROM of up to 8MByte in size, and some support circuitry.

The low power microcontroller is run on 1.8V core and 3.3V I/O power supply voltages. The core power can be produced on-board by a small LDO regulator or provided externally.

The processor module can be programmed in a variety of languages using the GNU toolchain, like C/C++ Pascal or ADA. There are also several other commercial development tools available from many vendors.

Table of Contents

Features

- 66MHz ARM7TDMI processor core
- 256kb zero wait-state RAM
- Up to 8MBytes of 16-bit FLASH memory (2MB standard)
- A user-programmable LED to display program state
- A watch-dog LED that lights up if a watch-dog event occurred
- Optional internal core power supply
- 8-bit or 16-bit external bus operations are supported
- Versatile bus-interface with programmable speed for each different peripherial slot
- Two serial ports
- Three timer/counters
- Up-to 22 digital I/O lines (27 in non-H-Storm compatible mode)
- JTAG debug interface provided
- Can boot from internal FLASH or from external memory connected to nSEL0
- On-board reset generator

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Theory of operation

The hcAT91 module contains three main components and some additional support circuitry. The tree main components are the AT91R40008 microcontroller, the 16-bit FLASH memory and the 72-pin H-Storm standard connector.

System-bus

The integrated memory-controller of the microcontroller is used to address the three available peripherial regions (nSEL0, nSEL1, nSEL2) and the FLASH memory. All I/O regions are mapped to memory locations. The mapping between these signals and the microcontrollers' external chip-selects under normal operation is as follows:

H-Storm signal	***AT91R40008 signal***
FLASH memory	CS0
nSEL0	CS1
nSEL1	CS2
nSEL2	CS3

When the module is in programming mode (nPROG is low), the previous assignment is modified as follows:

H-Storm signal	***AT91R40008 signal***
nSEL0	CS0
nSEL0	CS1
nSEL1	CS2
nSEL2	CS3

Since the microcontroller boots from external memory connected to CS0, this change makes it possible to boot the processor from either the internal FLASH memory for normal operation or from an external memory connected to nSEL0 for initial programming purposes.
Upon reset the microcontroller starts execution of the program found in a memory connected to CS0. This memory is initially mapped to physical address 0. The execution starts in ARM mode. The memory access cycles are programmed to be rather slow so that all types of FLASH devices would be compatible with the processor. After the initial program startup, the application can program faster accesses to CS0 to better match the capabilities of the FLASH memory, switch to THUMB mode to better facilitate the narrow 16-bit external bus, or copy itself into internal RAM where it can be executed full-speed with zero wait-states.
Additional chip-select signals (CS1-CS3) are used to access the H-Storm peripherial and the system-board. These chip-select signals can be assigned to arbitrary physical memory locations to better suite the application needs and are highly programmable so that various communication speeds can be used with different peripherials.
The CPU module supports both 8-bit and 16-bit access cycles, with and without wait-states. It does not generate burst cycles.
The module support both edge- and level-triggered interrupts. The nIRQx lines of the H-Storm connector are connected to IRQ lines of the microcontroller as follows:

H-Storm signal	*AT91R40008 signal*
nIRQ0	FIQ
nIRQ1	IRQ1
nIRQ2	IRQ2

Integrated peripherials

The microcontroller contains three timers/counters, two serial ports, a watch-dog timer and 32-bit GPIO lines. Many of these lines however are multiplexed to the same pins of the processor chip. All of the available peripherials are connected to the H-Storm bus, with the exception of a couple of the GPIO lines. The user-defined part of the H-Storm connector is connected to the microcontroller pins as follows:

H-Storm signal	*AT91R40008 signal*
IOA0	P13/SCK0
IOA1	none
IOA2	P15/RXD0
IOA3	P13/SCK0
IOA4	none
IOA5	P14/TXD0
IOB0	P20/SCK1
IOB1	none
IOB2	P22/RXD1
IOB3	P20/SCK1
IOB4	none
IOB5	P21/TXD1

H-Storm signal	*AT91R40008 signal*
IOC0	P0/TCLK0
IOC1	P1/TIOA0
IOC2	P2/TIOB0
IOC3	P3/TCLK1
IOC4	P4/TIOA1
IOC5	P5/TIOB1
IOD0	P6/TCLK2
IOD1	P7/TIOA2
IOD2	P8/TIOB2
IOD3	P9/IRQ0
IOD4	P16
IOD5	P17
IOD6	P18
IOD7	P19

PnP Bus

The H-Storm PnP bus signals are connected to two GPIO lines of the microcontroller. The protocol of the PnP bus is implemented in SW. The pin assignment is as follows:

H-Storm signal	*AT91R40008 signal*
PnP_C	P23
PnP_D	P31

Programming mode

When the nPROG signal is tied low upon reset, the microcontroller will boot from an external memory connected to nSEL0 for initial programming purposes. This allows for program execution on a module where the on-board flash is corrupted or simply blank. The external memory can contain code that erases and re-programs the FLASH memory such that consequent boot attempts from that memory would succeed. Since the standard H-Storm bus is capable of accessing only 2kBytes of external memory connected to any single peripherial select signal, only a very small boot-loader program can be placed in that external memory. The usual method therefore would be that that small boot-loader would download a bigger binary image from a host computer by means of one of the serial ports of the microcontroller. This larger program would than be capable of initializing the FLASH memory to a valid state and program a boot-image into it.
When the nPROG signal is high upon reset, normal boot-sequence from the on-board FLASH memory us used.

Power considerations

Two versions of the module exist. One contains an integrated 1.8V voltage regulator and requires only a single power source of 3.3V. The other does not contain this integrated power supply and relies on dual 3.3V/1.8V external power. The power consumption of the module under various circumstances is as follows:

Condition	*Power consumption*		
	single power version	*dual power version*	
	3.3V	*3.3V*	*1.8V*
Power down	TBD	TBD	TBD
Idle	TBD	TBD	TBD
Normal	55mA	TBD	TBD
Peak	TBD	TBD	TBD

H-Storm module connector pin-out

Pin number	*Pin function*	*Pin name*	*Note*
A1	O	nRD	Active low read enable
A2	O	nUWE	Active low upper byte write enable
A3	O	nLWE	Active low lower byte write enable
A4	IOCPU	nRESET	Active low reset input/output
A5	O	nESEL0	Active low external module select 0
A6	O	nESEL1	Active low external module select 1
A7	O	nESEL2	Active low external module select 2
A8	IPU	nFIRQ	Active low fast-interrupt request input
A9	IPU	nIRQ1	Active low interrupt request input
A10	IPU	nIRQ2	Active low interrupt request input
A11	IPU	nWAIT	Active low external wait-state input
A12	IPU	nPROG	Active low programming mode select
A13	O	A0	Address lines
A14	O	A1	
A15	O	A2	
A16	O	A3	
A17	O	A4	
A18	O	A5	
A19	O	A6	
A20	O	A7	
A21	O	A8	
A22	O	A9	

Pin number	*Pin function*	*Pin name*	*Note*
A23	IO	D0	Data lines
A24	IO	D1	
A25	IO	D2	
A26	IO	D3	
A27	IO	D4	
A28	IO	D5	
A29	IO	D6	
A30	IO	D7	
A31	IO	D8	
A32	IO	D9	
A33	IO	D10	
A34	IO	D11	
A35	IO	D12	
A36	IO	D13	
A37	IO	D14	
A38	IO	D15	
A39	PWR	VCC	3.3V power supply
A40	PWR	VCC	
A41	PWR	GND	Ground power line
A42	PWR	GND	
A43	PWR	VCC_1_8	1.8V power supply or n.c. if the CPU card is single supply
A44		n.c.	
A45	IO	P13/SCK0	General purpose I/O line, serial port 0 clock
A46		none	
A47	IO	P15/RXD0	General purpose I/O line, serial port 0 data transmit line
A48	IO	P13/SCK0	General purpose I/O line, serial port 0 clock
A49		none	
A50	IO	P14/TXD0	General purpose I/O line, serial port 0 data receive line
A51	IO	P20/SCK1	General purpose I/O line, serial port 1 clock
A52		none	
A53	IO	P22/RXD1	General purpose I/O line, serial port 1 data transmit line
A54	IO	P20/SCK1	General purpose I/O line, serial port 1 clock
A55		none	

Pin number	*Pin function*	*Pin name*	*Note*
A56	IO	P21/TXD1	General purpose I/O line, serial port 1 data receive line
A57	IO	P0/TCLK0	General purpose I/O line, timer 0 clock
A58	IO	P1/TIOA0	General purpose I/O line, timer 0 I/O A
A59	IO	P2/TIOB0	General purpose I/O line, timer 0 I/O D
A60	IO	P3/TCLK1	General purpose I/O line, timer 1 clock
A61	IO	P4/TIOA1	General purpose I/O line, timer 1 I/O A
A62	IO	P5/TIOB1	General purpose I/O line, timer 1 I/O D
A63	IO	P6/TCLK2	General purpose I/O line, timer 2 clock
A64	IO	P7/TIOA2	General purpose I/O line, timer 2 I/O A
A65	IO	P8/TIOB2	General purpose I/O line, timer 2 I/O D
A66	IO	P9/IRQ0	General purpose I/O line, interrupt signal 0
A67	IO	P16	General purpose I/O line
A68	IO	P17	General purpose I/O line
A69	IO	P18	General purpose I/O line
A70	IO	P19	General purpose I/O line
A71	IOPU	PnP_C/P23	Plug-and-play bus clock signal, General purpose I/O line
A72	IOPU	PnP_D/P31	Plug-and-play bus data signal, General purpose I/O line

Mechanical design

The module adheres to the H-Storm standard module specification. It is 100mm wide and 47.5mm high. It is implemented on a standard double-sided 1.5mm laminate PCB process with 0.5mm via hole size and 0.2mm track width.