FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-13104-3E

Memory FRAM

CMOS

1 M Bit (64 K × 16)

MB85R1002

■ DESCRIPTIONS

The MB85R1002 is an FRAM (Ferroelectric Random Access Memory) chip consisting of 65,536 words x 16 bits of non-volatile memory cells created using ferroelectric process and silicon gate CMOS process technologies.
The MB85R1002 is able to retain data without using a back-up battery, as is needed for SRAM.
The memory cells used in the MB85R1002 can be used for at least 10^{10} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E^2PROM.
The MB85R1002 uses a pseudo-SRAM interface that is compatible with conventional asynchronous SRAM.

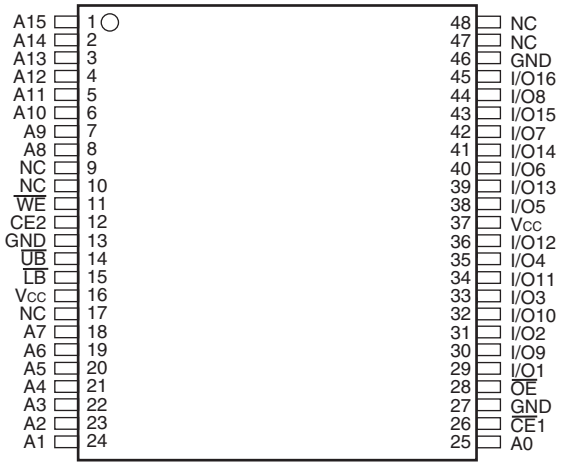
■ FEATURES

- Bit configuration : 65,536 words × 16 bits
- Read/write endurance : 10^{10} times/bit (Min)
- Operating power supply voltage : 3.0 V to 3.6 V
- Operating temperature range : − 20 °C to +85 °C
- Data retention : 10 years (+55 °C)
- $\overline{LB}$ and $\overline{UB}$ data byte control
- Package : 48-pin plastic TSOP (1)
  : 48-pin plastic FBGA

FUJITSU

■ PIN ASSIGNMENT

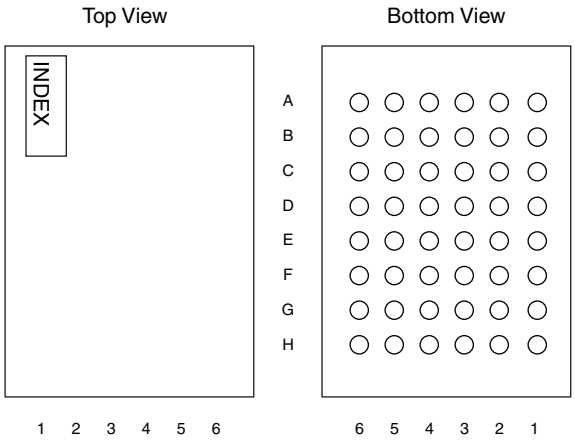
(TOP VIEW)



(FPT-48P-M25)

(Continued)

(Continued)



	1	2	3	4	5	6
A	$\overline{LB}$	$\overline{OE}$	A0	A1	A2	CE2
B	I/O9	$\overline{UB}$	A3	A4	$\overline{CE1}$	I/O1
C	I/O10	I/O11	A5	A6	I/O2	I/O3
D	GND	I/O12	NC	A7	I/O4	V_{CC}
E	V_{CC}	I/O13	NC	NC	I/O5	GND
F	I/O15	I/O14	A14	A15	I/O6	I/O7
G	I/O16	NC	A12	A13	$\overline{WE}$	I/O8
H	NC	A8	A9	A10	A11	NC

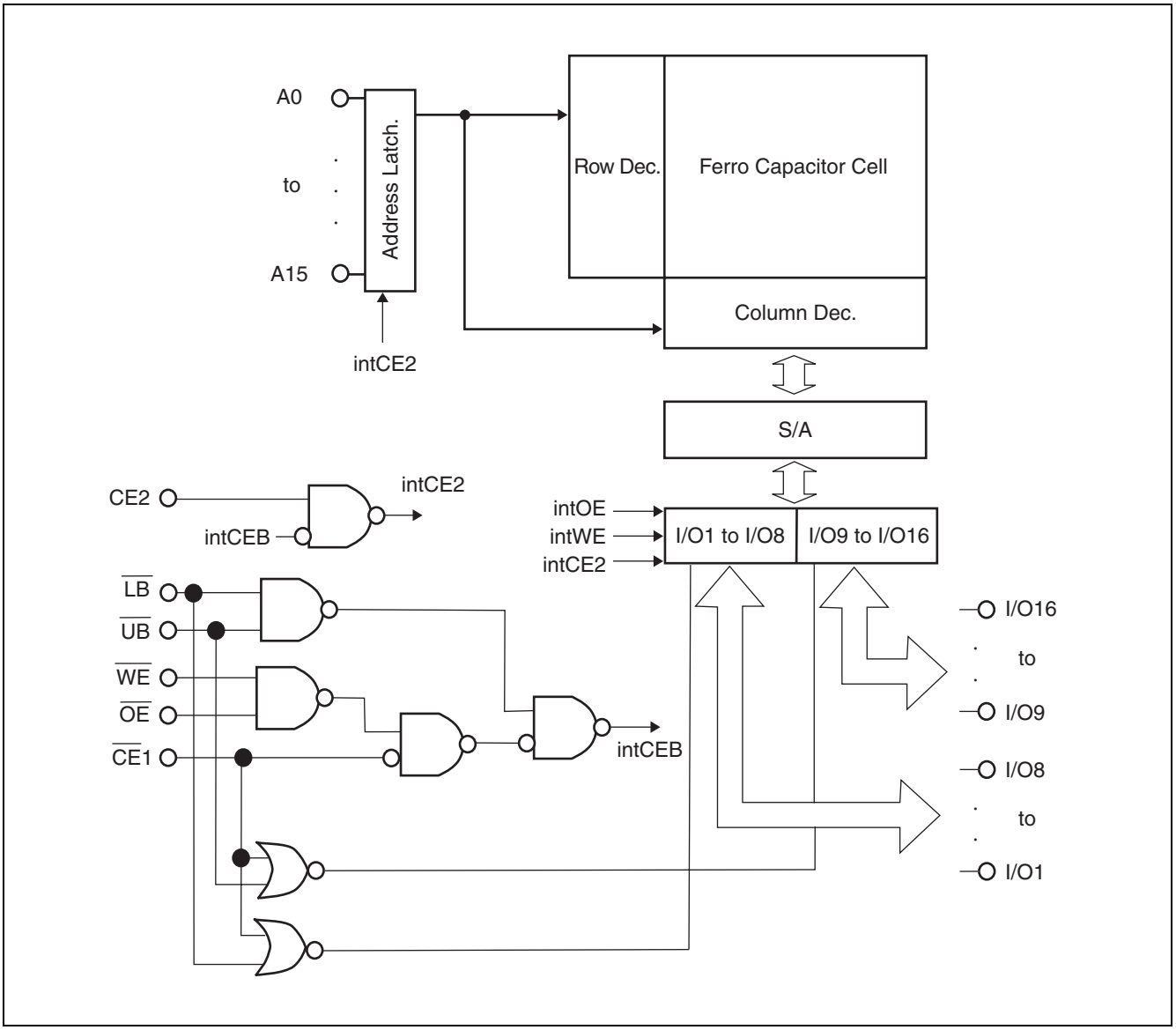
	6	5	4	3	2	1
A	CE2	A2	A1	A0	$\overline{OE}$	$\overline{LB}$
B	I/O1	$\overline{CE1}$	A4	A3	$\overline{UB}$	I/O9
C	I/O3	I/O2	A6	A5	I/O11	I/O10
D	V_{CC}	I/O4	A7	NC	I/O12	GND
E	GND	I/O5	NC	NC	I/O13	V_{CC}
F	I/O7	I/O6	A15	A14	I/O14	I/O15
G	I/O8	$\overline{WE}$	A13	A12	NC	I/O16
H	NC	A11	A10	A9	A8	NC

(BGA-48P-M23)

■ PIN DESCRIPTION

Pin name	Function
A0 to A15	Address In
I/O1 to I/O16	Data Input/Output
$\overline{CE}$1	Chip Enable 1 in
CE2	Chip Enable 2 in
$\overline{WE}$	Write Enable in
$\overline{OE}$	Output Enable in
$\overline{LB}$, $\overline{UB}$	Data Byte Control in
V_{CC}	Power Supply
GND	Ground
NC	No Connection

■ BLOCK DIAGRAM



■ FUNCTION TRUTH TABLE

Mode	$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$	$\overline{UB}$	I/O1 to I/O8	I/O9 to I/O16	Supply Current
Standby Pre-charge	H	X	X	X	X	X	High-Z	High-Z	Standby (I_{SB})
	X	L	X	X	X	X			
	X	X	H	H	X	X			
	X	X	X	X	H	H			
Read	↓ L	H ↑	H	L	L	L	Dout	Dout	Operation (I_{CC})
					L	H	Dout	High-Z	
					H	L	High-Z	Dout	
Read ($\overline{OE}$ control*1)	L	H	H	↓	L	L	Dout	Dout	
					L	H	Dout	High-Z	
					H	L	High-Z	Dout	
Write	↓ L	H ↑	L	X	L	L	Din	Din	
					L	H	Din	High-Z	
					H	L	High-Z	Din	
Write ($\overline{WE}$ control*2)	L	H	↓	H	L	L	Din	Din	
					L	H	Din	High-Z	
					H	L	High-Z	Din	

Notes : L = V_{IL}, H = V_{IH}, X can be either V_{IL} or V_{IH}, High-Z = High Impedance

↓ : Latch address and latch data at falling edge, ↑ : Latch address and latch data at rising edge

*1 : $\overline{OE}$ control of the Pseudo-SRAM means the valid address at the falling edge of $\overline{OE}$ to read.

*2 : $\overline{WE}$ control of the Pseudo-SRAM means the valid address and data at the falling edge of $\overline{WE}$ to write.

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Supply Voltage*	V_{CC}	–0.5	+4.0	V
Input Voltage*	V_{IN}	–0.5	V_{CC} + 0.5	V
Output Voltage*	V_{OUT}	–0.5	V_{CC} + 0.5	V
Ambient Operating Temperature	T_A	–20	+85	°C
Storage Temperature	T_{stg}	–40	+125	°C

* : All voltages are referenced to GND.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage*	V_{CC}	3.0	3.3	3.6	V
Input Voltage (high)*	V_{IH}	$V_{CC} \times 0.8$	—	V_{CC} + 0.5	V
Input Voltage (low)*	V_{IL}	–0.5	—	+0.6	V
Ambient Operating Temperature	T_A	– 20	—	+85	°C

* : All voltages are referenced to GND.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC CHARACTERISTICS

(within recommended operating conditions)

Parameter	Symbol	Test Conditions	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = 0 V to V_{CC}	—	—	10	µA
Output Leakage Current	$\|I_{LO}\|$	V_{OUT} = 0 V to V_{CC}, $\overline{CE}1$ = V_{IH} or $\overline{OE}$ = V_{IH}	—	—	10	µA
Operating Power Supply Current	I_{CC}	$\overline{CE}1$ = 0.2 V, CE2 = V_{CC}–0.2 V, I_{out} = 0 mA*1	—	10	15	mA
Standby Current	I_{SB}	$\overline{CE}1 \geq V_{CC}$–0.2 V	—	10	50	µA
		CE2 ≤ 0.2 V*2				
		$\overline{OE} \geq V_{CC}$–0.2 V, $\overline{WE} \geq V_{CC}$–0.2 V*2				
		$\overline{LB} \geq V_{CC}$–0.2 V, $\overline{UB} \geq V_{CC}$–0.2 V*2				
Output Voltage (high)	V_{OH}	I_{OH} = –0.1 mA	$V_{CC} \times 0.8$	—	—	V
Output Voltage (low)	V_{OL}	I_{OL} = 2.0 mA	—	—	0.4	V

*1 : During the measurement of I_{CC} , the Address, Data In were taken to only change once per active cycle.
Iout : output current

*2 : All pins other than setting pins should be input at the CMOS level voltages such as H $\geq V_{CC}$ – 0.2 V, L $\leq$ 0.2 V.

2. AC TEST CONDITIONS

Supply Voltage : 3.0 V to 3.6 V
Operating Temperature : –20 °C to +85 °C
Input Voltage Amplitude : 0.3 V to 2.7 V
Input Rising Time : 5 ns
Input Falling Time : 5 ns
Input Evaluation Level : 2.0 V / 0.8 V
Output Evaluation Level : 2.0 V / 0.8 V
Output Impedance : 50 pF

(1) Read Operation

(within recommended operating conditions)

Parameter	Symbol	Value		Unit
		Min	Max	
Read Cycle time	t_{RC}	150	—	ns
$\overline{CE}1$ Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
$\overline{OE}$ Active Time	t_{RP}	120	—	ns
$\overline{LB}$, $\overline{UB}$ Active Time	t_{BP}	120	—	ns
Pre-charge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
$\overline{OE}$ Setup Time	t_{ES}	0	—	ns
$\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	5	—	ns
Output Data Hold time	t_{OH}	0	—	ns
Output Set Time	t_{LZ}	30	—	ns
$\overline{CE}1$ Access Time	t_{CE1}	—	100	ns
CE2 Access Time	t_{CE2}	—	100	ns
$\overline{OE}$ Access Time	t_{OE}	—	100	ns
Output Floating Time	t_{OHZ}	—	20	ns

(2) Write Operation

(within recommended operating conditions)

Parameter	Symbol	Value		Unit
		Min	Max	
Write Cycle Time	t_{WC}	150	—	ns
$\overline{CE}$1 Active Time	t_{CA1}	120	—	ns
CE2 Active Time	t_{CA2}	120	—	ns
$\overline{LB}$, $\overline{UB}$ Active Time	t_{BP}	120	—	ns
Pre-Charge Time	t_{PC}	20	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
$\overline{LB}$, $\overline{UB}$ Setup Time	t_{BS}	5	—	ns
Write Pulse Width	t_{WP}	120	—	ns
Data Setup Time	t_{DS}	0	—	ns
Data Hold Time	t_{DH}	50	—	ns
Write Setup Time	t_{WS}	0	—	ns

(**3**) **Power ON/OFF Sequence**

(within recommended operating conditions)

Parameter	Sym-bol	Value			Unit
		Min	Typ	Max	
$\overline{CE}$1 LEVEL hold time for Power OFF	t_{pd}	85	—	—	ns
$\overline{CE}$1 LEVEL hold time for Power ON	t_{pu}	85	—	—	ns

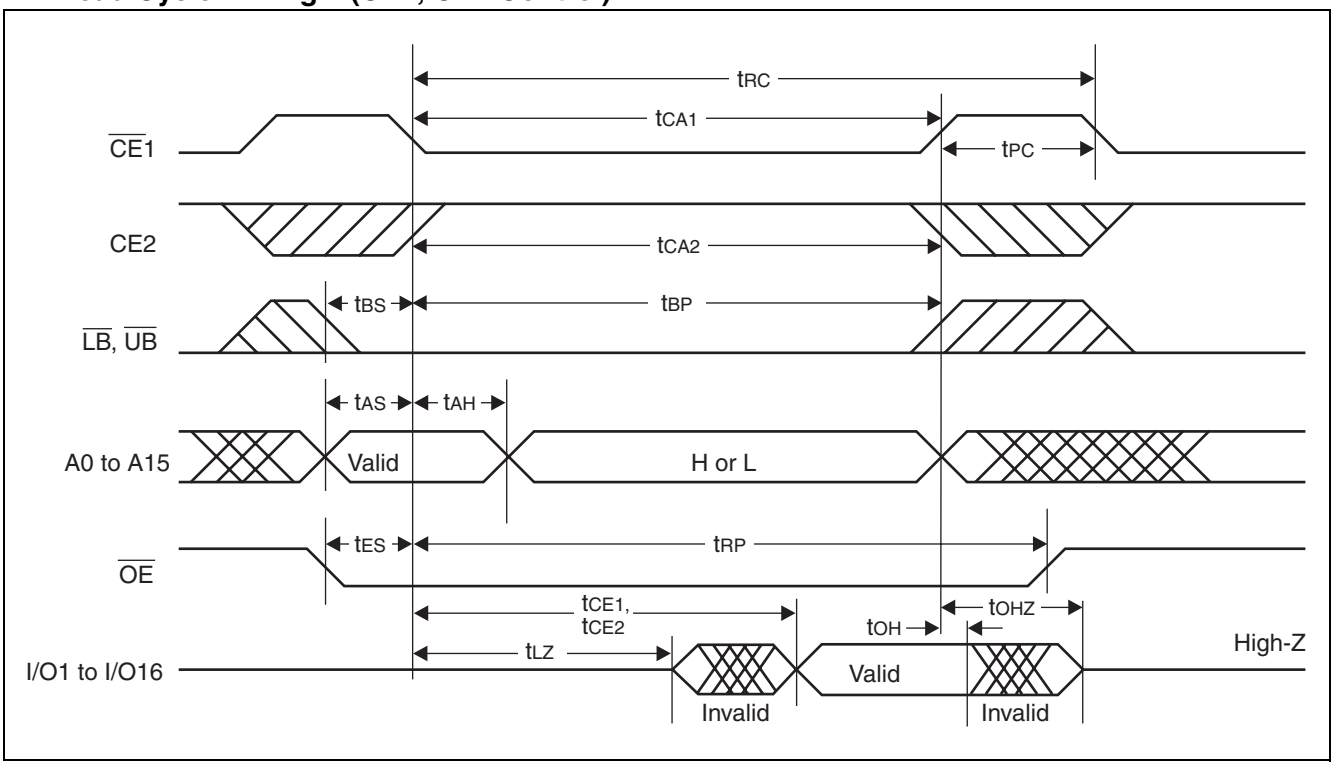
3. Pin Capacitance

(f = 1 MHz, T_A = +25 °C)

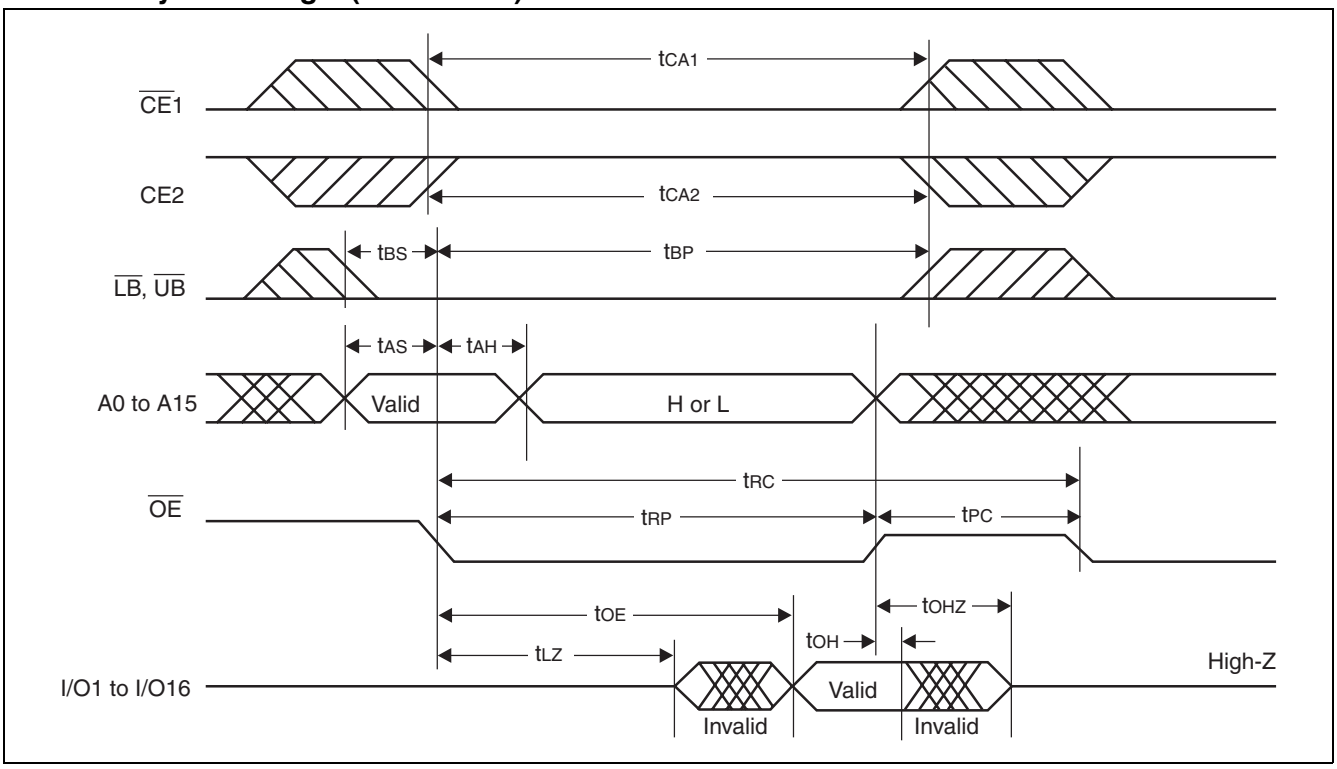
Parameter	Symbol	Test Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	V_{IN} = GND	—	—	10	pF
Output Capacitance	C_{OUT}	V_{OUT} = GND	—	—	10	pF

■ TIMING DIAGRAMS

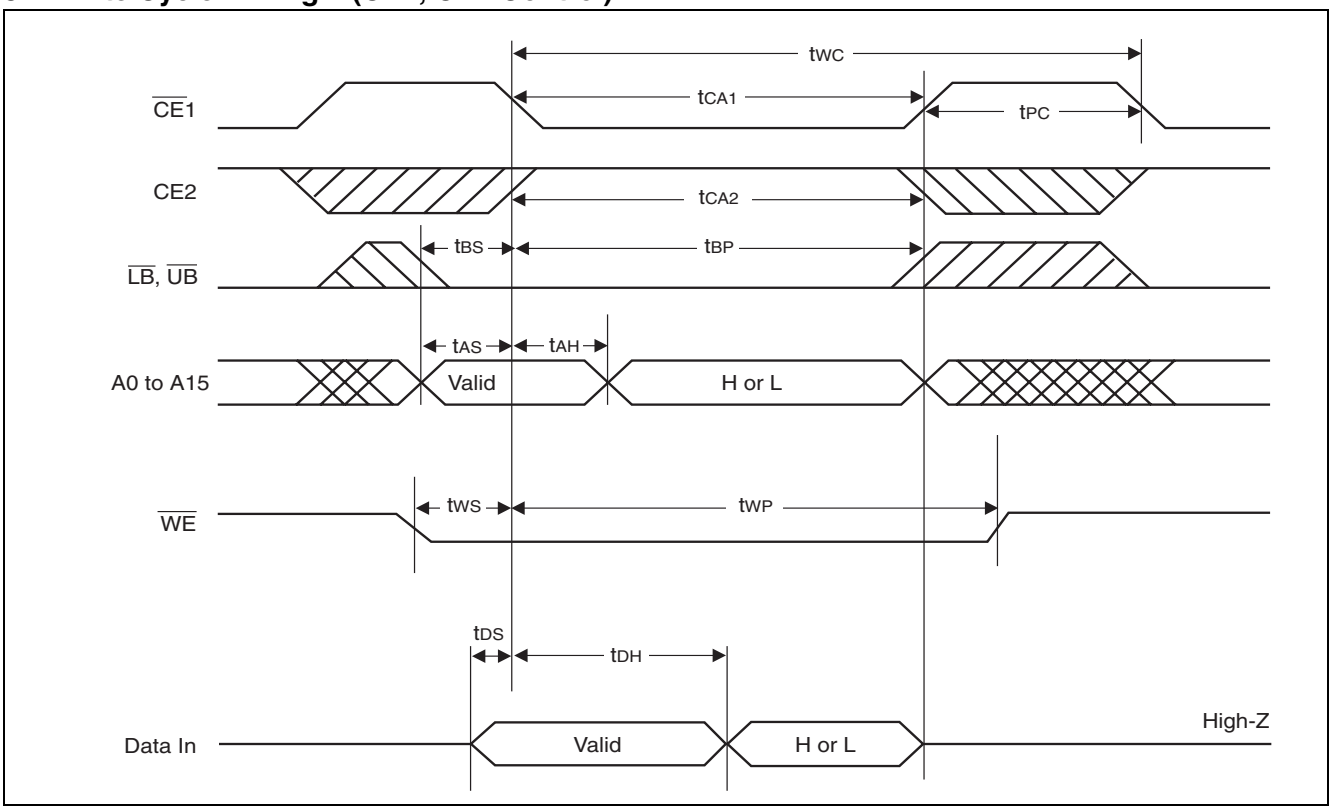
1. Read Cycle Timing 1 ($\overline{CE}$1, CE2 Control)



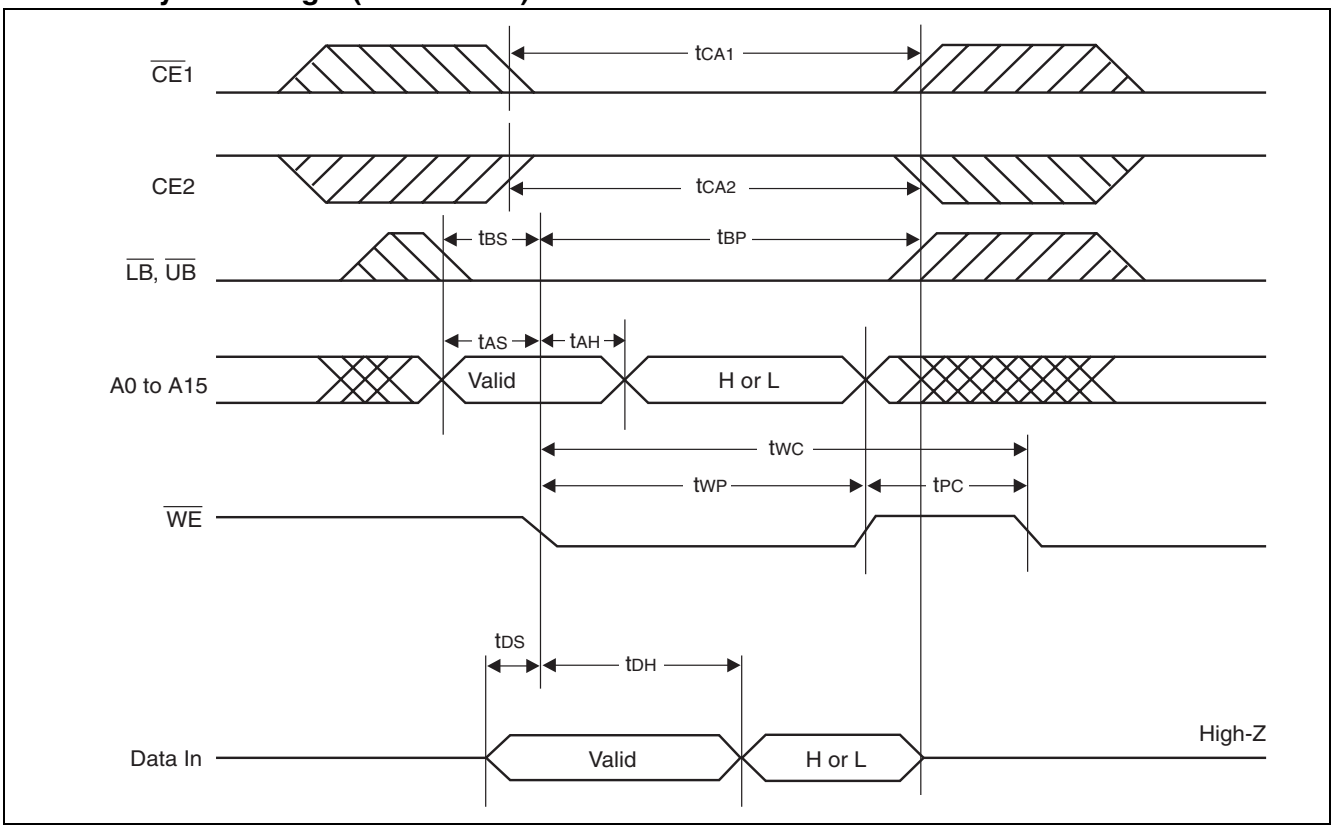
2. Read Cycle Timing 2 ($\overline{OE}$ Control)



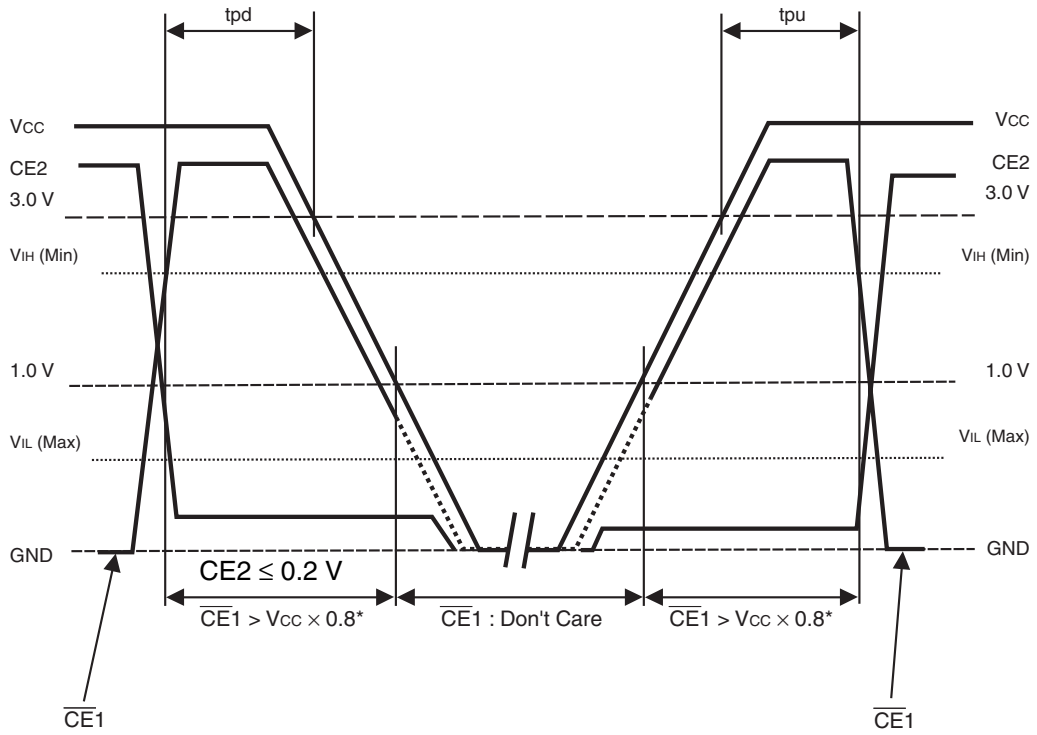
3. Write Cycle Timing 1 ($\overline{CE}$1, CE2 Control)



4. Write Cycle Timing 2 ($\overline{WE}$ Control)



■ POWER ON/OFF SEQUENCE



* : $\overline{CE}1$ (Max) < V_{CC} + 0.5 V

Note : You can choose either of $\overline{CE}1$ or CE2, or both for disenable control of the device.

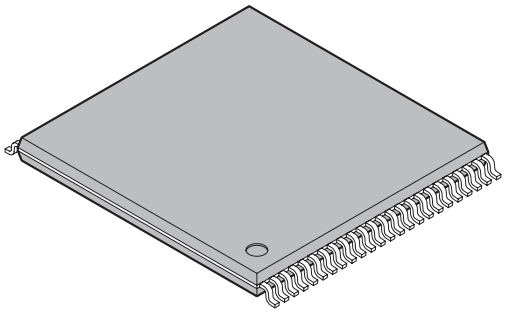
■ NOTES ON USE

Data that is written prior to IR reflow is not guaranteed to be retained after IR reflow.

■ ORDERING INFOMATION

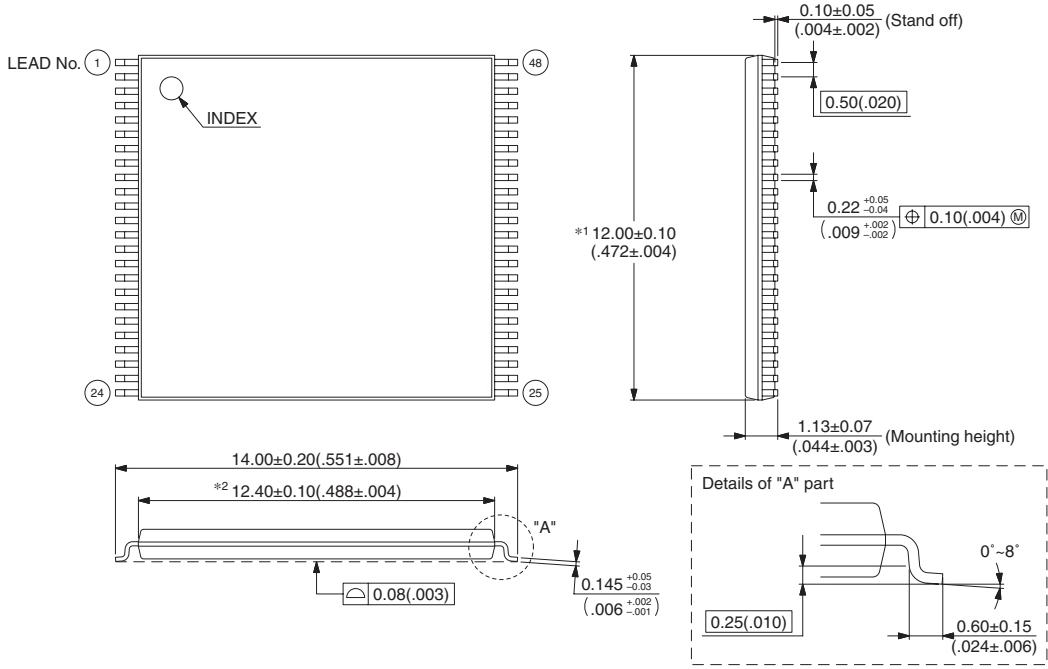
Part number	Package
MB85R1002PFTN-GE1	48-pin plastic TSOP(1) (FPT-48P-M25)
MB85R1002BGT-GE1	48-pin plastic FBGA (BGA-48P-M23)

■ PACKAGE DIMENSIONS

48-pin plastic TSOP(1)		
	Lead pitch	0.50 mm
	Package width × package length	12.00 × 12.40 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.20 mm MAX
	Weight	0.37 g
(FPT-48P-M25)	Code (Reference)	P-TSOP(1)48-12×12.4-0.50

48-pin plastic TSOP(1)
(FPT-48P-M25)

Note 1) *1 : Resin protrusion. (Each side : +0.15 (.006) Max).
Note 2) *2 : These dimensions do not include resin protrusions.
Note 3) Pin widths and pin thicknesses include plating thickness.
Note 4) Pin widths do not include tie bar cutting burrs.

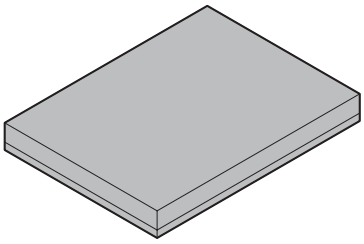


Dimensions in mm (inches).
Note: The values in parentheses are reference values

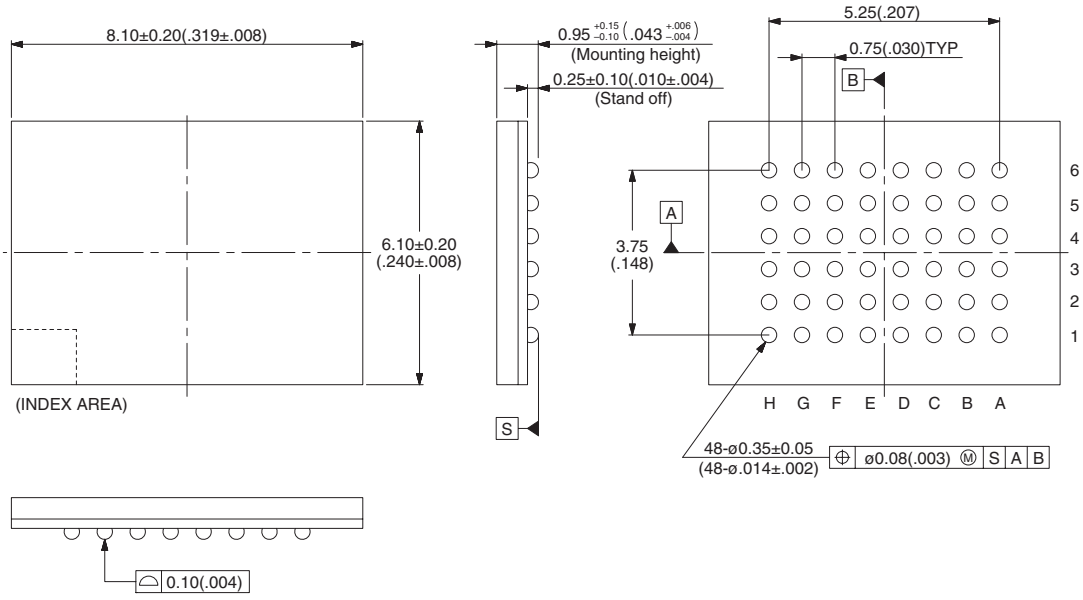
Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

(Continued)

(Continued)

48-pin plastic FBGA		
 (BGA-48P-M23)	Lead pitch	0.75 mm
	Package width × package length	8.10 mm × 6.10 mm
	Lead shape	Ball
	Sealing method	Plastic mold
	Mounting height	1.10 mm Max
	Weight	0.08 g

48-pin plastic FBGA
(BGA-48P-M23)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/fj/DATASHEET/ef-ovpklv.html

FUJITSU LIMITED

The contents of this document are subject to change without notice. Customers are advised to consult with FUJITSU sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of Fujitsu semiconductor device; Fujitsu does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information. Fujitsu assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of Fujitsu or any third party or does Fujitsu warrant non-infringement of any third-party's intellectual property right or other right by using such information. Fujitsu assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that Fujitsu will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

The company names and brand names herein are the trademarks or registered trademarks of their respective owners.

Edited Business Promotion Dept.