



Preliminary

March 2005

RMPA2458

2.4–2.5 GHz InGaP HBT Low Current Linear Power Amplifier

Features

- 31.5dB small signal gain
- 27dBm output power @ 1dB compression
- 103mA total current at 19dBm modulated power out
- 2.5% EVM at 19 dBm modulated power out
- 3.3V collector supply operation
- 2.9V mirror supply operation
- Power saving shutdown options (bias control)
- Integrated power detector with 20dB dynamic range
- Lead-free RoHS compliant 3 x 3 x 0.9mm leadless package
- Internally matched to 50 Ohms and DC blocked RF input/output
- Optimized for use in 802.11b/g applications

General Description

The RMPA2458 power amplifier is designed for high performance WLAN applications in the 2.4–2.5 GHz frequency band. The low profile 16 pin 3 x 3 x 0.9 mm package with internal matching on both input and output to 50 Ohms minimizes next level PCB space and allows for simplified integration. The on-chip detector provides power sensing capability while the bias control provides power saving shutdown capability. The PA's industry leading low power consumption and excellent linearity are achieved using our InGaP Heterojunction Bipolar Transistor (HBT) technology.

Device



Electrical Characteristics¹ 802.11g OFDM Modulation

(176 μ s burst time, 100 μ s idle time) 54 Mbps Data Rate, 16.7 MHz Bandwidth

Parameter	Min	Typ	Max	Units
Frequency	2.4		2.5	GHz
Collector Supply Voltage	3.0	3.3	3.6	V
Mirror Supply Voltage		2.9		V
Mirror Supply Current		3.3		mA
Gain		31.5		dB
Total Current @ 19dBm P _{OUT}		103		mA
EVM @ 19dBm P _{OUT} ²		2.5		%
Detector Output @ 19dBm P _{OUT}		340		mV
Detector Threshold ³		5		dBm

Notes:

1. VC1, VC2, VC3 = 3.3V, VM123 = 2.9V, T_A = 25°C, PA is constantly biased, 50 Ω system.

2. Percentage includes system noise floor of EVM = 0.8%.

3. P_{OUT} measured at P_{IN} corresponding to power detection threshold.

Electrical Characteristics¹ 802.11b CCK Modulation (RF not framed) 11 Mbps Data Rate 22.0 MHz Bandwidth

Parameter	Min	Typ	Max	Units
Frequency	2.4		2.5	GHz
Collector Supply Voltage	3.0	3.3	3.6	V
Mirror Supply Voltage		2.9		V
Mirror Supply Current		3.3		mA
Gain		32		dB
Total Current @ 19dBm Pout		130		mA
First Side Lobe Power @ 19dBm Pout		-36		dBm
Second Side Lobe Power @ 19dBm Pout		-60		dBm
Max Pout Spectral Mask Compliance ²		24		dBm
Detector Output @ 19dBm Pout		1.15		V
Detector Pout Threshold ³		5		dBm

Electrical Characteristics¹ Single Tone

Parameter	Min	Typ	Max	Units
Frequency	2.4		2.5	GHz
Collector Supply Voltage	3.0	3.3	3.6	V
Mirror Supply Voltage (VM123)	2.6	2.9	3.1	V
Gain		31.5		dB
Total Quiescent Current		49		mA
Bias Current at pin VM123 ⁴		3.2		mA
P1dB Compression		27		dBm
Current @ P1dB Compression		600		mA
Shutdown Current (VM123 = 0V)		<1.0		μA
Input Return Loss		12		dB
Output Return Loss		9		dB
Detector Output at P1dB Compression		2.4		V
Detector Pout Threshold ³		5		V
Turn-on Time ⁵		<1.0		μS
Spurious (Stability) ⁶		-65		dBc

Notes:

- VC1, VC2, VC3 = 3.3V, VM123 = 2.9 Volts, Ta = 25°C, PA is constantly biased, 50Ω system.
- Pin is adjusted to point where performance approaches spectral mask requirements.
- Pout measured at Pin corresponding to power detection threshold.
- Mirror bias current is included in the total quiescent current.
- Measured from Device On signal turn on to the point where RF Pout stabilizes to 0.5dB.
- Load VSWR is set to 8:1 and the angle is varied 360 degrees. Pout = -30dBm to P1dB.

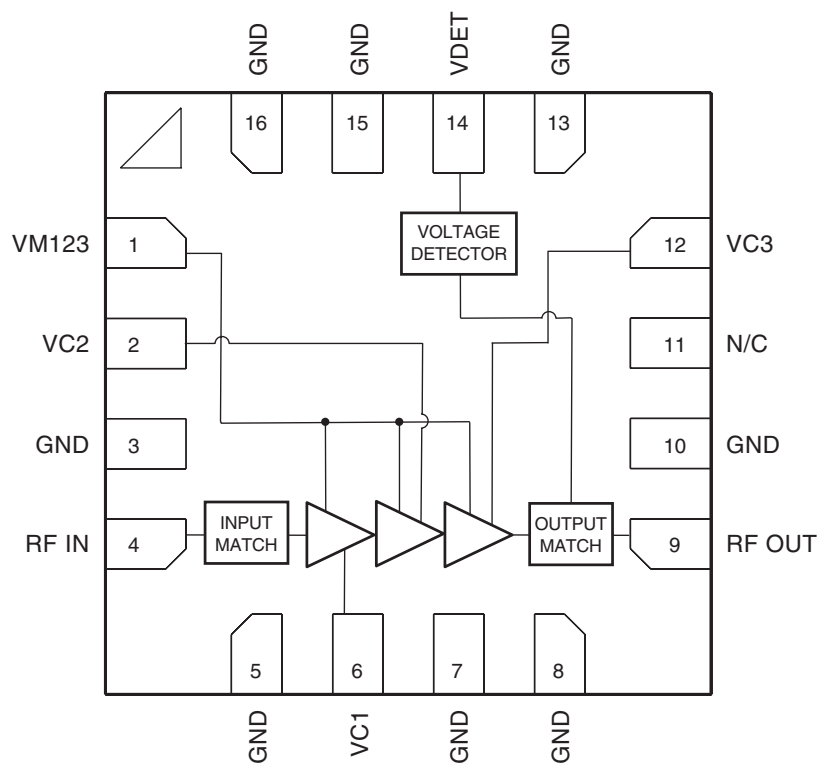
Absolute Ratings¹

Symbol	Parameter	Ratings	Units
VC1, VC2, VC3	Positive Supply Voltage	5	V
IC1, IC2, IC3	Supply Current IC1 IC2 IC3	50 150 700	mA mA mA
VM123	Positive Bias Voltage	3.6	V
P _{IN}	RF Input Power	+5	dBm
T _{CASE}	Case Operating Temperature	-40 to +85	°C
T _{STG}	Storage Temperature	-55 to +150	°C

Note:

1. No permanent damage with one parameter set at extreme limit. Other parameters set to typical values.

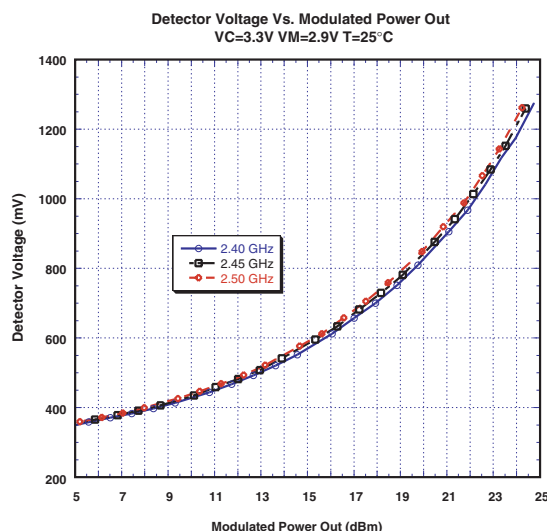
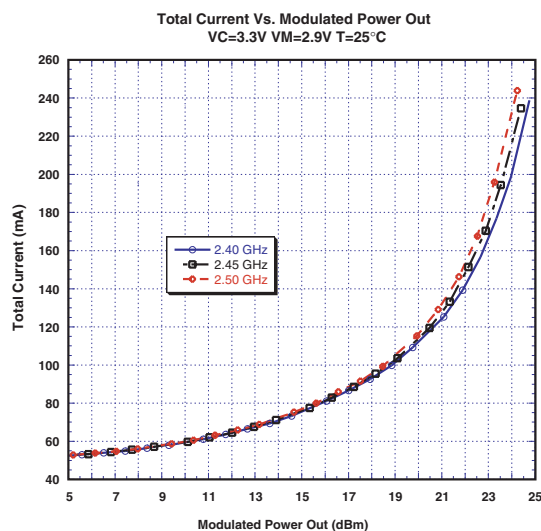
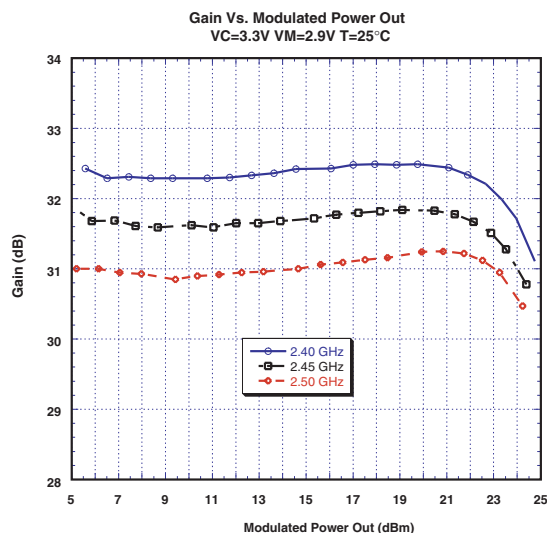
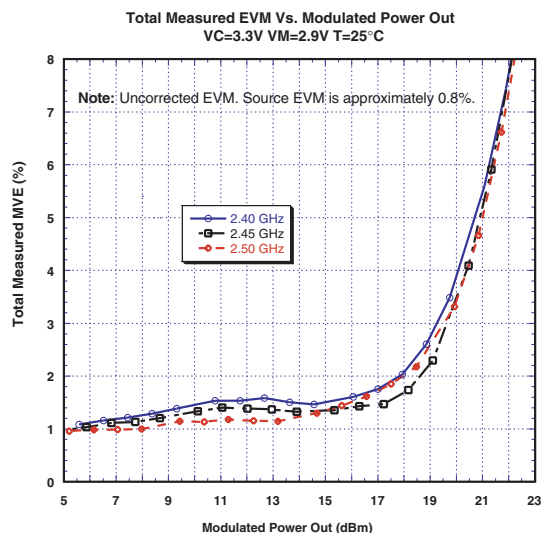
Functional Block Diagram



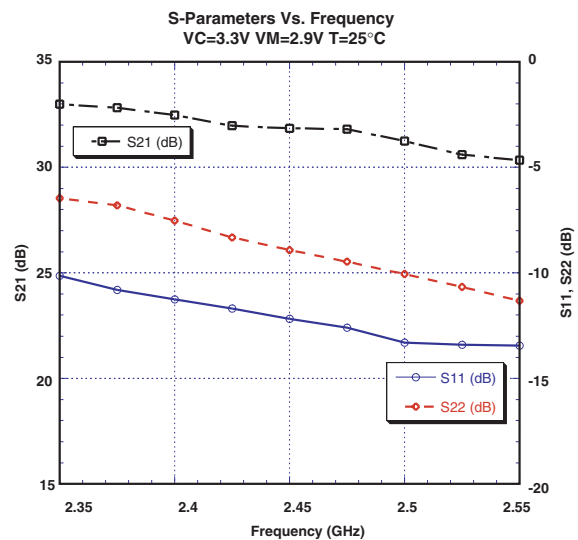
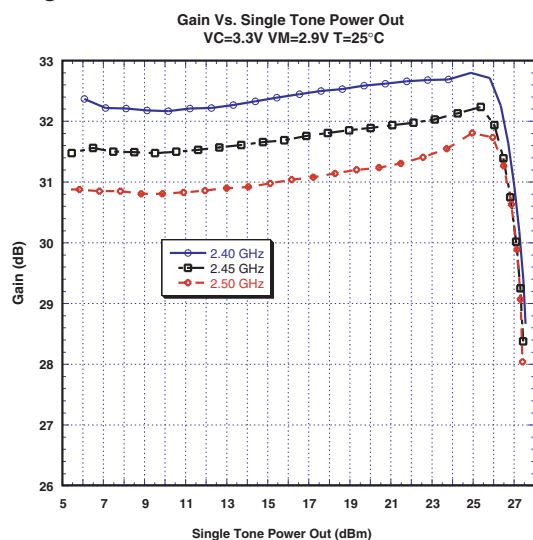
Pin	Description
1	VM123
2	VC2
3	GND
4	RF IN
5	GND
6	VC1
7	GND
8	GND
9	RF OUT
10	GND
11	N/C
12	VC3
13	GND
14	VDET
15	GND
16	GND

Performance Data 802.11g OFDM Modulation

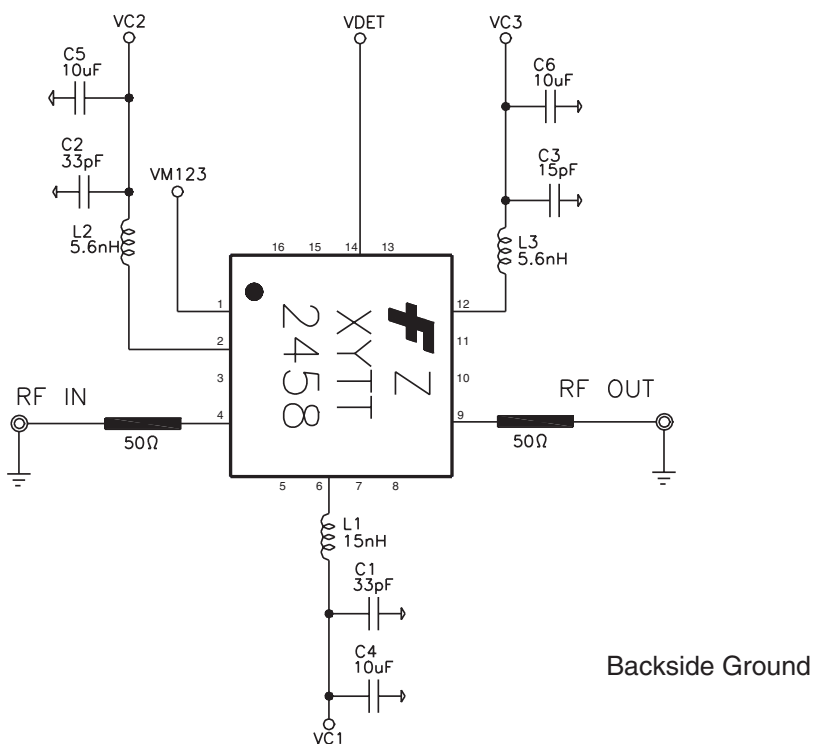
(176 μ s burst time, 100 μ s idle time) 54 Mbps Data Rate, 16.7 MHz Bandwidth



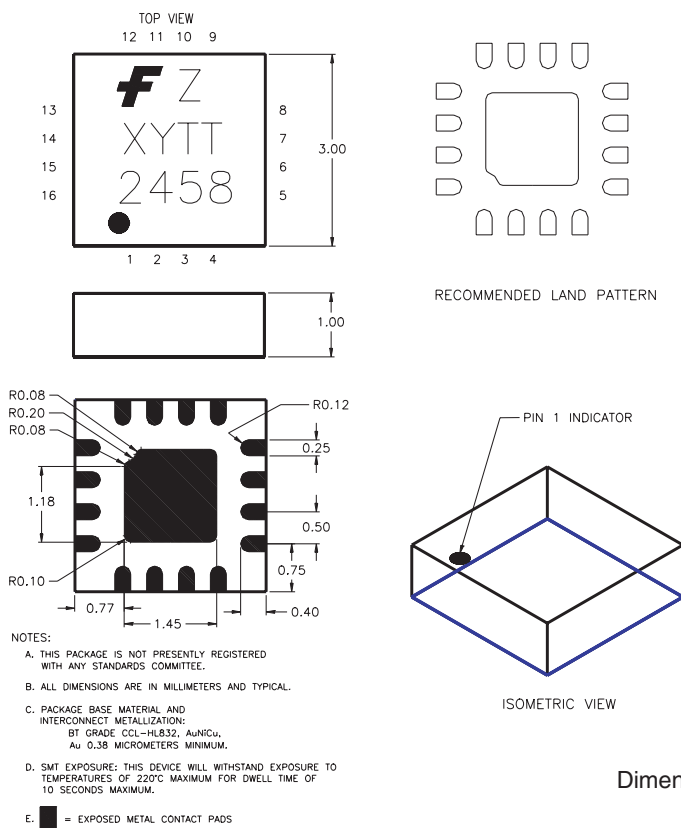
Single Tone



Evaluation Board Schematic



Package Outline

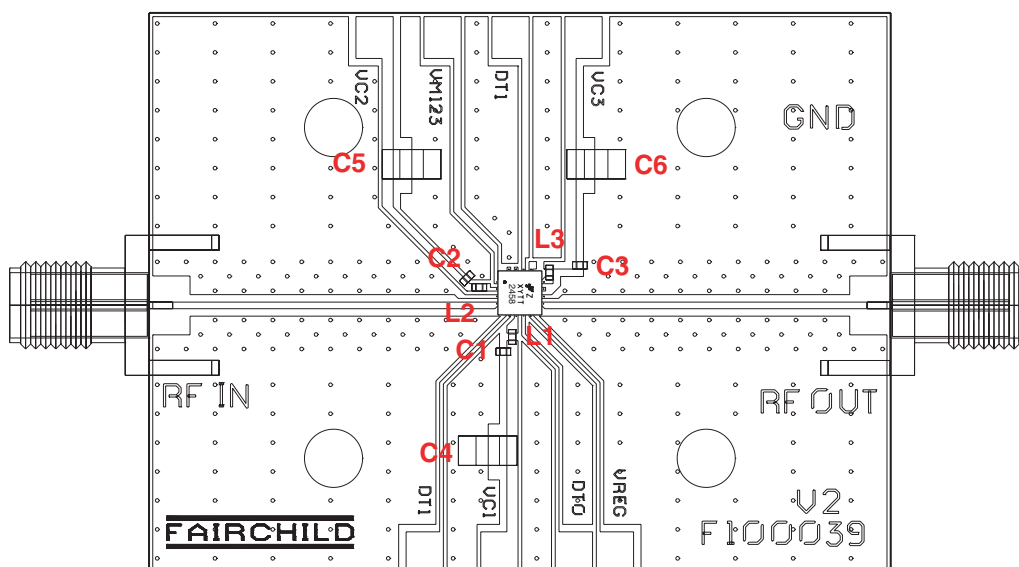


Note: Dimensions do not include protrusions or mold flash. These are not to exceed 0.006" (.155mm) on any side.

Evaluation Board of Materia

Qty	Item No.	Part Number	Description	Vendor
1	1	F100039	PC Board	Fairchild
2	2	#142-0701-841	SMA Connector	Johnson
7	3	#S1322-XX-ND	RT Angle Sgl M Header	Digikey
Ref	4	F1XXXXX	Assembly, RMPA2458	Fairchild
1	5 (C3)	06035A150J	15pF Capacitor	AVX
2	6 (C1, C2)	GRM39C0G330J50D500	33pF Capacitor	Murata
3	7 (C4, C5, C6)	CC1206JX5R106M	10μF Capacitor	TDK
2	8 (L2, L3)	LLV1005FB5N6S	5.6nH Inductor	Toko
1	9 (L1)	LLV1005FH15NK	15nH Inductor	Toko
A/R	10	SN63	Solder Paste	Indium Corp.
A/R	11	SN96	Solder Paste	Indium Corp.

Evaluation Board Layout



Actual Board Size = 2.0" X 1.5"

Evaluation Board Turn-On Sequence¹

Recommended turn-on sequence:

- 1) Connect common ground terminal to the Ground (GND) pin on the board.
- 2) Connect voltmeter to pin DT1 (VDET, voltage detector).
- 3) Apply positive supply voltage VC1 (=3.3 V) to pin VC1 (first stage collector).
- 4) Apply positive supply voltage VC2 (=3.3 V) to pin VC2 (second stage collector).
- 5) Apply positive supply voltage VC3 (=3.3 V) to pin VC3 (third stage collector).
- 6) Apply positive bias voltage VM123 (=2.9 V) to pin VM123 (bias networks).
- 7) At this point, you should expect to observe the following positive currents flowing into the pins:

Pin	Current
VM123	1.0 – 5.0 mA
VC1	1.0 – 9.0 mA
VC2	5.0 – 25.0 mA
VC3	22.0 – 42.0 mA

- 8) Apply input RF power to SMA connector pin RFIN. Currents in pins VC1, VC2 and VC3 will vary depending on the input drive level.

- 9) Vary positive voltage on pin VM123 from +2.9 V to +0 V to shut down the amplifier or alter the power level. Shut down current flow into the pins:

Pin	Current
VC1	<1 nA
VC2	<1 nA
VC3	<1 nA

Recommended turn-off sequence:

Use reverse order described in the turn-on sequence above.

Note:

1. Turn on sequence is not critical and it is not necessary to sequence power supplies in actual system level design

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