



May 2000

QFET™

FQS4410

Single N-Channel, Logic Level, Power MOSFET

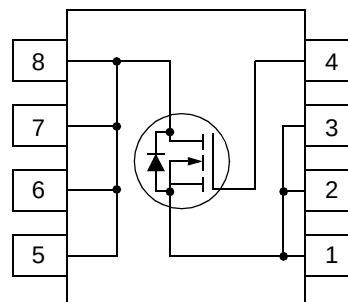
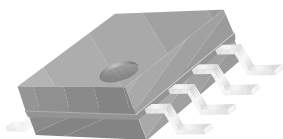
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as DC/DC converters, high efficiency switching for power management in portable and battery operated products.

Features

- 10A, 30V, $R_{DS(on)} = 0.0135\Omega$ @ $V_{GS} = 10V$
- Low gate charge (typical 21 nC)
- Low C_{rss} (typical 145 pF)
- Fast switching
- Improved dv/dt capability
- 175°C maximum junction temperature rating



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQS4410	Units
V_{DSS}	Drain-Source Voltage	30	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$)	10	A
	- Continuous ($T_C = 70^\circ\text{C}$)	8	A
I_{DM}	Drain Current - Pulsed (Note 1)	50	A
V_{GSS}	Gate-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt (Note 3)	7.0	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$)	2.5	W
	Linear Derating Factor	0.02	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	50	°C/W

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	30	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.03	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 24\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.0	--	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$	--	--	0.0135	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$ (Note 4)	--	--	0.02	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 10\text{ V}, I_D = 5\text{ A}$	--	16	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	980	1280	pF
C_{oss}	Output Capacitance		--	590	770	pF
C_{rss}	Reverse Transfer Capacitance		--	145	190	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}, I_D = 5\text{ A},$ $R_G = 50\text{ }\Omega$ (Note 4, 5)	--	30	70	ns
t_r	Turn-On Rise Time		--	165	340	ns
$t_{d(off)}$	Turn-Off Delay Time		--	65	140	ns
t_f	Turn-Off Fall Time		--	110	230	ns
Q_g	Total Gate Charge	$V_{DS} = 24\text{ V}, I_D = 10\text{ A},$ $V_{GS} = 5\text{ V}$ (Note 4, 5)	--	21	28	nC
Q_{gs}	Gate-Source Charge		--	4.2	--	nC
Q_{gd}	Gate-Drain Charge		--	12	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	2.3	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	50	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 2.3 A	--	--	1.1	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 24 A, (Note 4) dI _F / dt = 100 A/μs	--	45	--	ns
Q _{rr}	Reverse Recovery Charge		--	45	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 3\text{ mH}, I_{AS} = 10\text{ A}, V_{DD} = 15\text{ V}, R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 10\text{ A}, dI/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

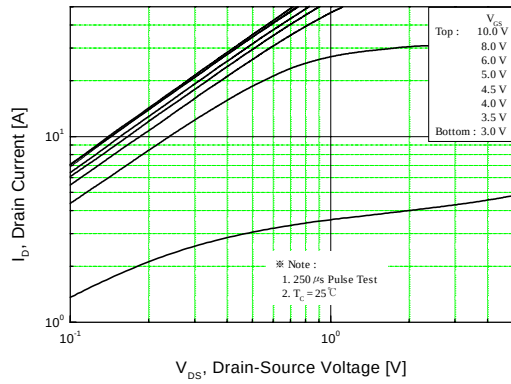


Figure 1. Output Characteristics

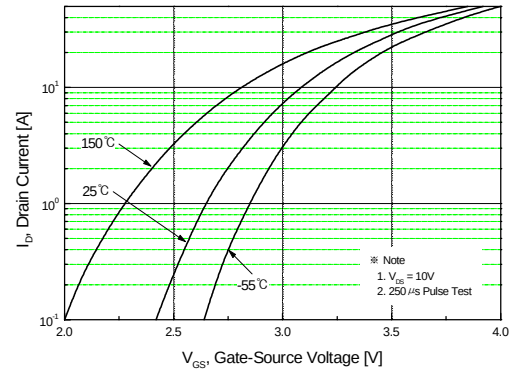


Figure 2. Transfer Characteristics

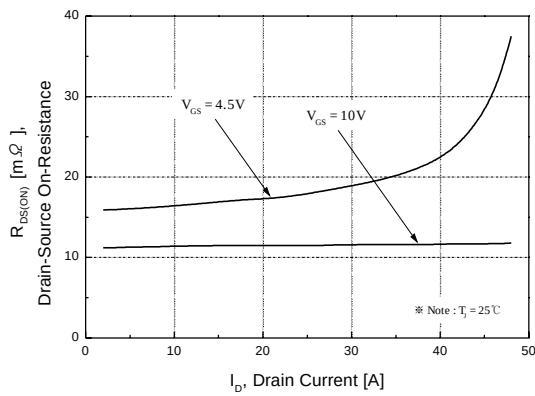


Figure 3. On-Resistance Variation vs. Drain Current

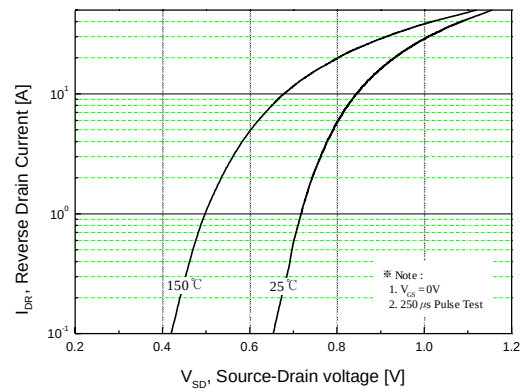


Figure 4. Source-Drain Diode Forward Voltage

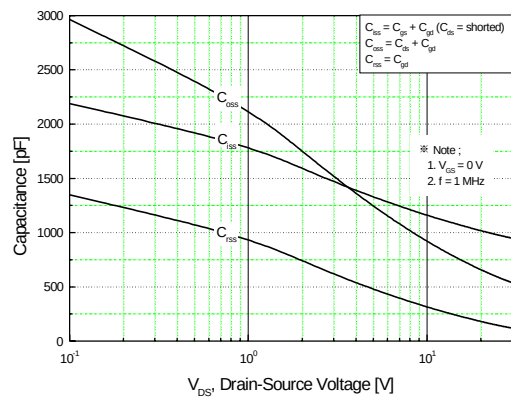


Figure 5. Capacitance vs. Drain-Source Voltage

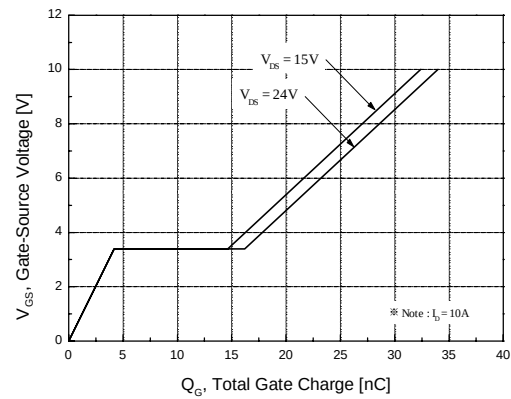


Figure 6. Gate Charge vs. Gate-Source Voltage

Typical Characteristics (Continued)

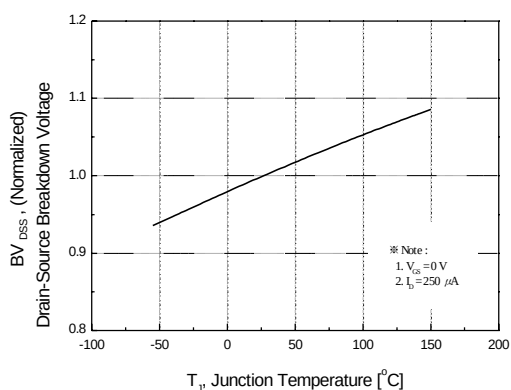


Figure 7. Breakdown Voltage vs. Temperature

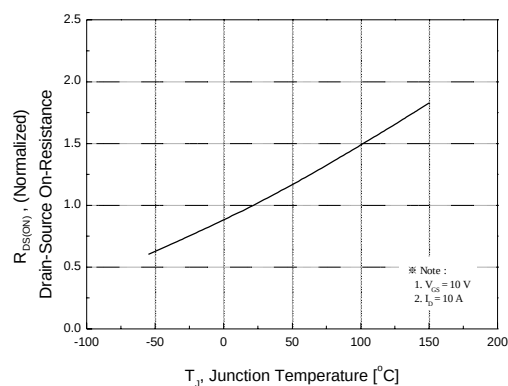


Figure 8. On-Resistance vs. Temperature

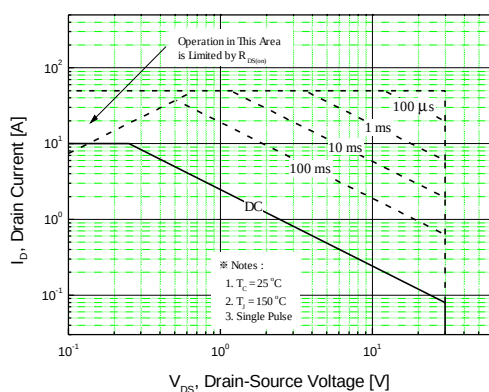


Figure 9. Maximum Safe Operating Area

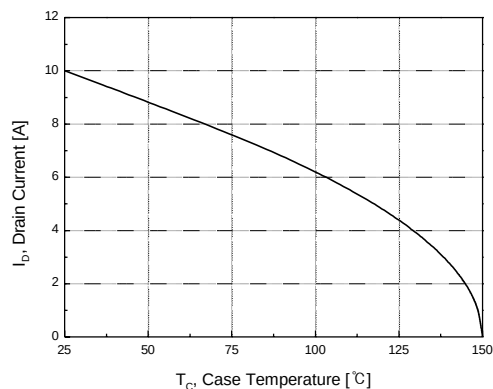


Figure 10. Maximum Drain Current vs. Case Temperature

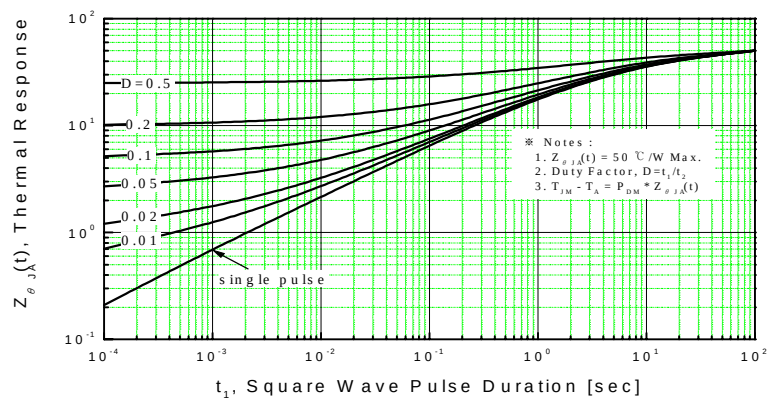
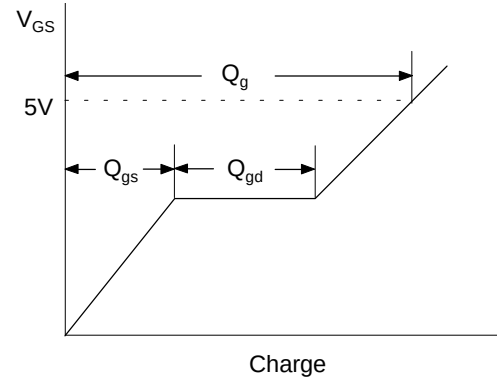
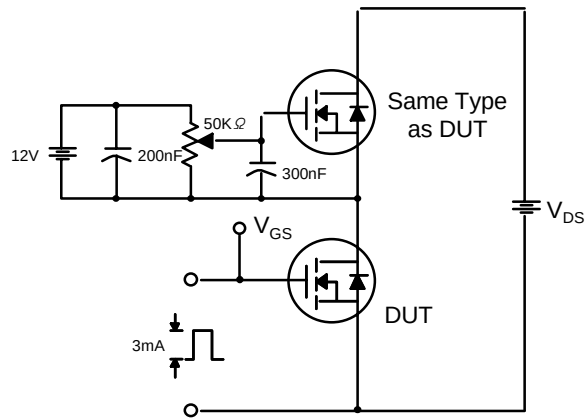
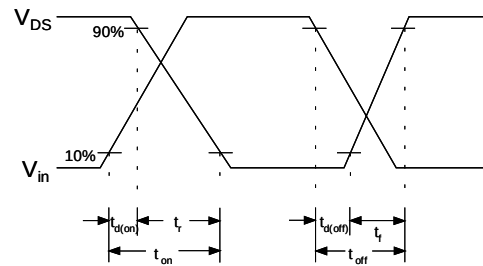
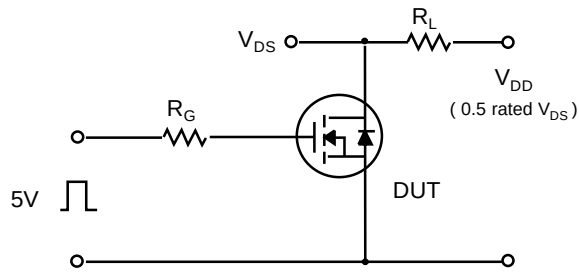


Figure 11. Thermal Response

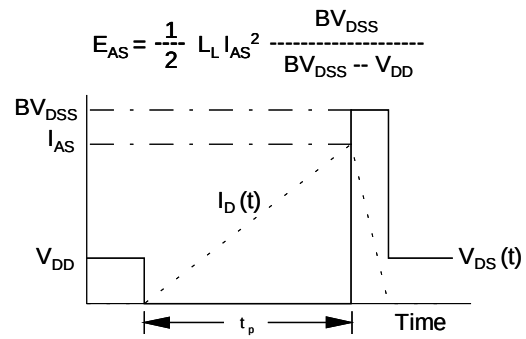
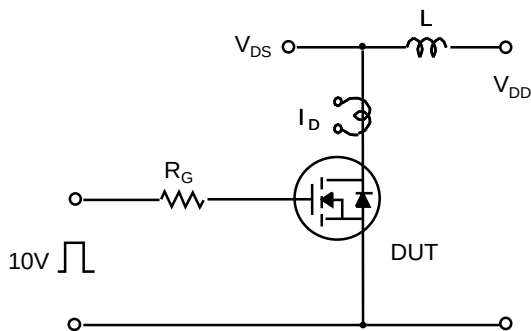
Gate Charge Test Circuit & Waveform



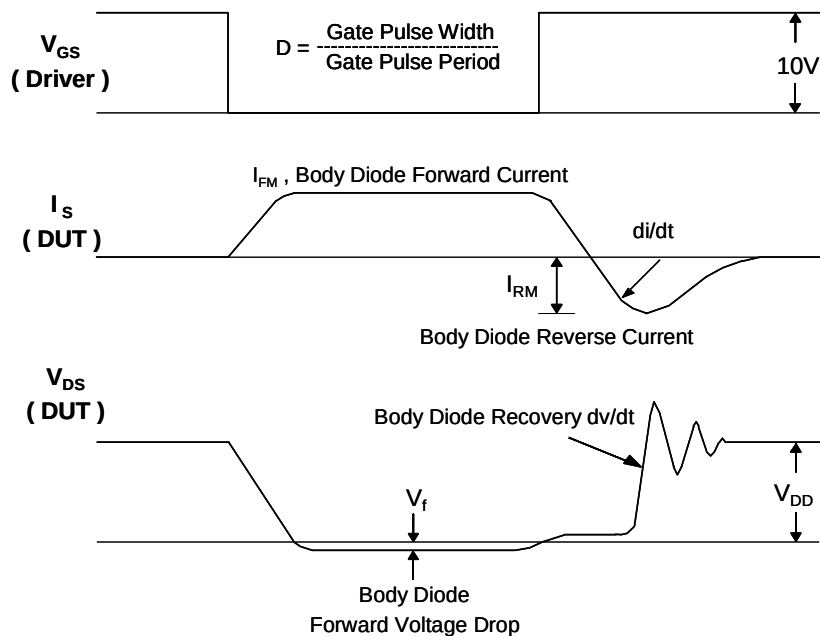
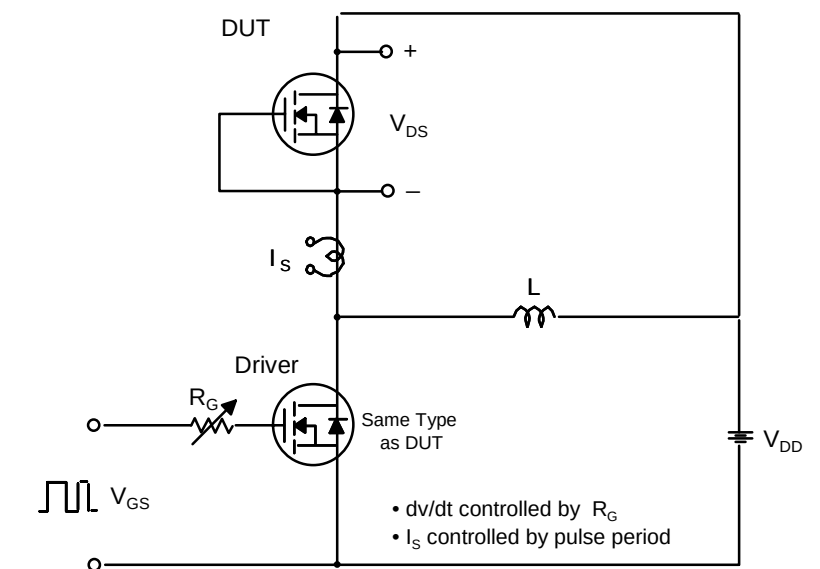
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms



Technical drawing of a 16-pin DIP package showing top, side, and end views with dimensions in mm and mils.

Top View Dimensions:

- Pin 1 to Pin 8 distance: 6.00 ± 0.30 mm / 0.236 ± 0.012 in
- Pin 4 to Pin 5 distance: 3.95 ± 0.20 mm / 0.156 ± 0.008 in
- Pin 1 to Pin 4 distance: 0.15 ± 0.10 mm / 0.006 ± 0.002 in

Side View Dimensions:

- Package height: 1.55 ± 0.20 mm / 0.061 ± 0.008 in
- Pin height: 4.92 ± 0.20 mm / 0.194 ± 0.008 in
- Pin pitch: 0.56 ± 0.022 mm
- Pin width: 0.41 ± 0.10 mm / 0.016 ± 0.004 in
- Pin thickness: 0.127 ± 0.050 mm

End View Dimensions:

- Package width: 5.72 ± 0.225 mm
- Package thickness: 0.50 ± 0.20 mm / 0.020 ± 0.008 in
- Lead angle: $0 \sim 8^\circ$

Other Dimensions:

- Pin 1 to Pin 5 distance: 5.13 ± 0.202 mm / 0.202 in
- Pin 1 to Pin 8 distance: 1.80 ± 0.071 mm / 0.071 in
- Pin 1 to Pin 4 distance: 1.27 ± 0.050 mm
- Pin 1 to Pin 5 distance: 1.27 ± 0.050 mm
- Pin 1 to Pin 8 distance: 1.27 ± 0.050 mm
- Pin 1 to Pin 5 distance: 1.27 ± 0.050 mm
- Pin 1 to Pin 8 distance: 1.27 ± 0.050 mm

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