FAIRCHILD SEMICONDUCTOR TM

May 2000

QFET™

FQS4410

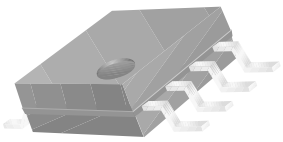
Single N-Channel, Logic Level, Power MOSFET

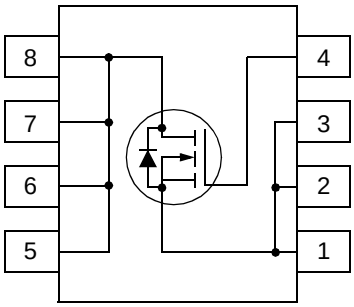
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as DC/DC converters, high efficiency switching for power management in portable and battery operated products.

Features

- 10A, 30V, $R_{DS(on)}$ = 0.0135Ω @V_{GS} = 10 V
- Low gate charge (typical 21 nC)
- Low Crss (typical 145 pF)
- Fast switching
- Improved dv/dt capability
- 175°C maximum junction temperature rating





Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQS4410	Units
V_{DSS}	Drain-Source Voltage		30	V
I_D	Drain Current - Continuous (T_C = 25°C)		10	A
	- Continuous (T_C = 70°C)		8	A
I_{DM}	Drain Current - Pulsed	(Note 1)	50	A
V_{GSS}	Gate-Source Voltage		± 20	V
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	7.0	V/ns
P_D	Power Dissipation (T_C = 25°C)		2.5	W
	Linear Derating Factor		0.02	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +175	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	50	°C/W

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	30	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C	--	0.03	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 30 V, V_{GS} = 0 V	--	--	1	µA
		V_{DS} = 24 V, T_C = 125°C	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = 20 V, V_{DS} = 0 V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = -20 V, V_{DS} = 0 V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.0	--	2.5	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = 10 V, I_D = 10 A	--	--	0.0135	Ω
		V_{GS} = 4.5 V, I_D = 5 A (Note 4)	--	--	0.02	
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 5 A	--	16	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	--	980	1280	pF
C_{oss}	Output Capacitance		--	590	770	pF
C_{rss}	Reverse Transfer Capacitance		--	145	190	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 15 V, I_D = 5 A, R_G = 50 Ω (Note 4, 5)	--	30	70	ns
t_r	Turn-On Rise Time		--	165	340	ns
$t_{d(off)}$	Turn-Off Delay Time		--	65	140	ns
t_f	Turn-Off Fall Time		--	110	230	ns
Q_g	Total Gate Charge	V_{DS} = 24 V, I_D = 10 A, V_{GS} = 5 V (Note 4, 5)	--	21	28	nC
Q_{gs}	Gate-Source Charge		--	4.2	--	nC
Q_{gd}	Gate-Drain Charge		--	12	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	2.3	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	50	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 2.3 A	--	--	1.1	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = 24 A, (Note 4) dI_F / dt = 100 A/µs	--	45	--	ns
Q_{rr}	Reverse Recovery Charge		--	45	--	nC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 3mH, I_{AS} = 10A, V_{DD} = 15V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 10A, di/dt ≤ 300A/us, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

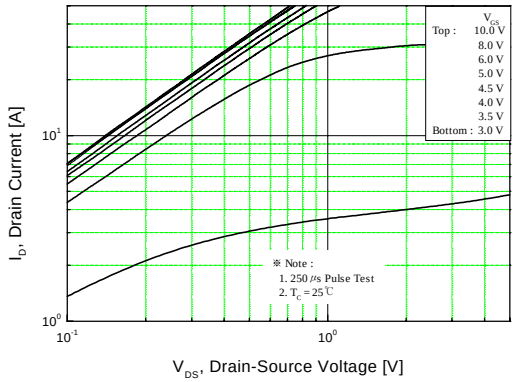


Figure 1. Output Characteristics

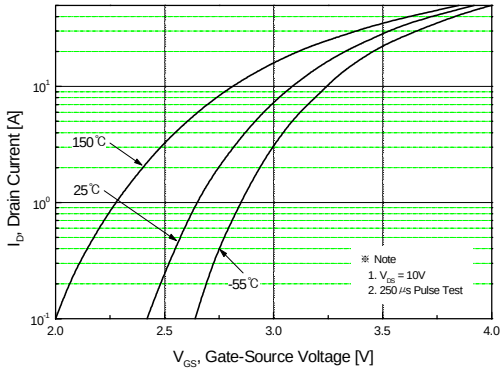


Figure 2. Transfer Characteristics

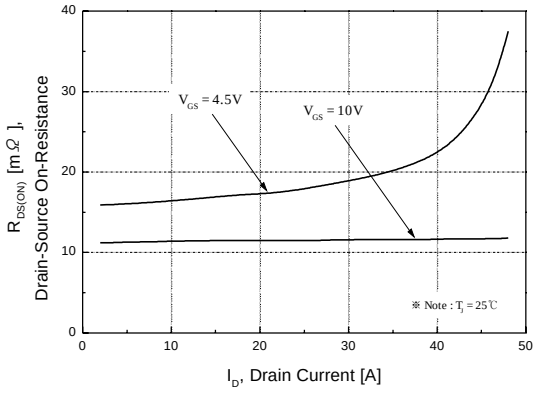


Figure 3. On-Resistance Variation vs. Drain Current

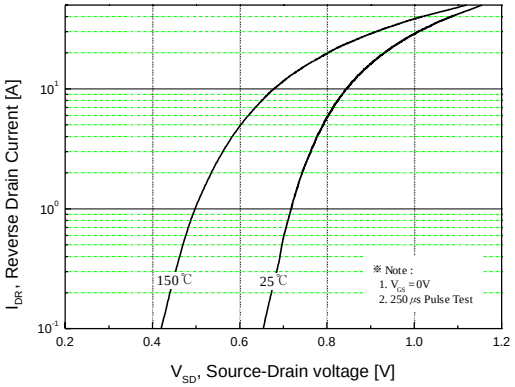


Figure 4. Source-Drain Diode Forward Voltage

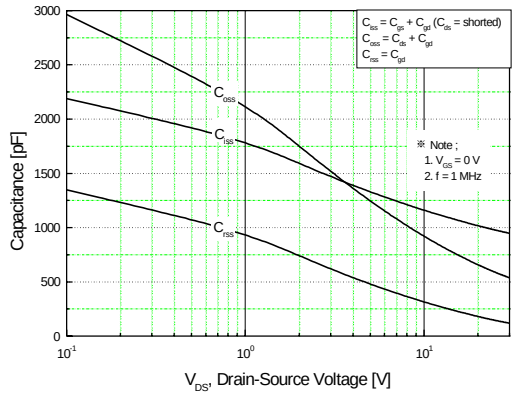


Figure 5. Capacitance vs. Drain-Source Voltage

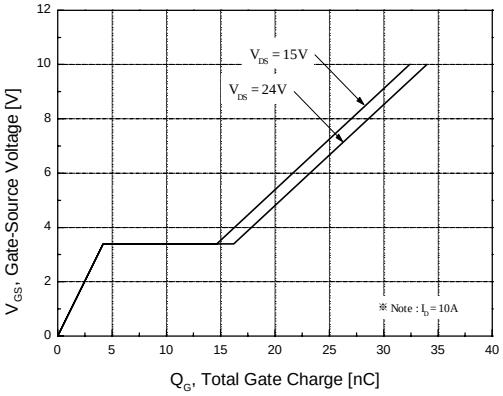


Figure 6. Gate Charge vs. Gate-Source Voltage

Typical Characteristics (Continued)

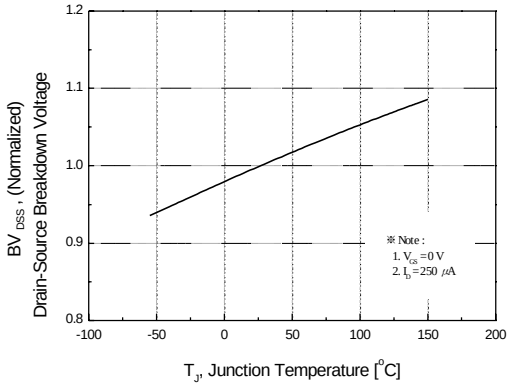


Figure 7. Breakdown Voltage vs. Temperature

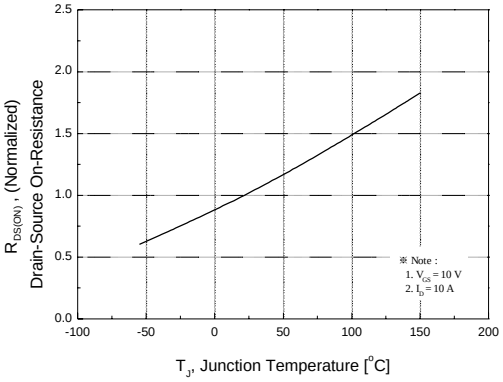


Figure 8. On-Resistance vs. Temperature

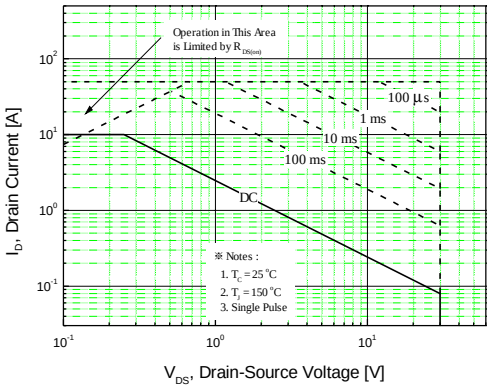


Figure 9. Maximum Safe Operating Area

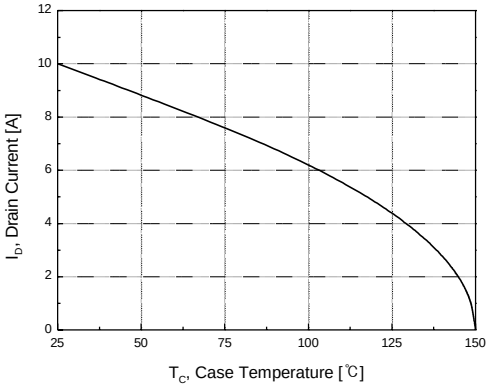


Figure 10. Maximum Drain Current vs. Case Temperature

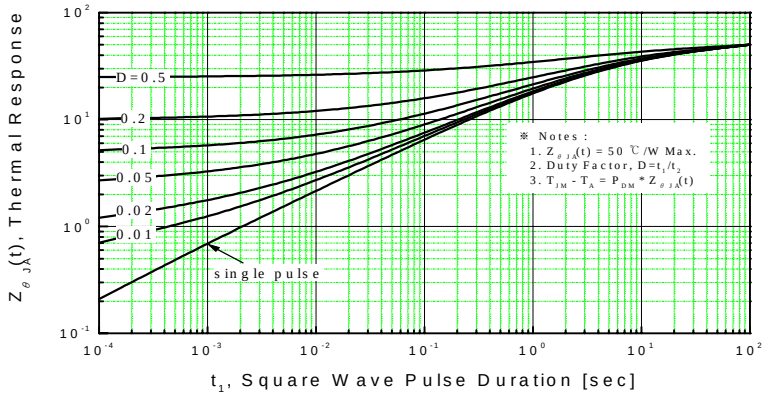
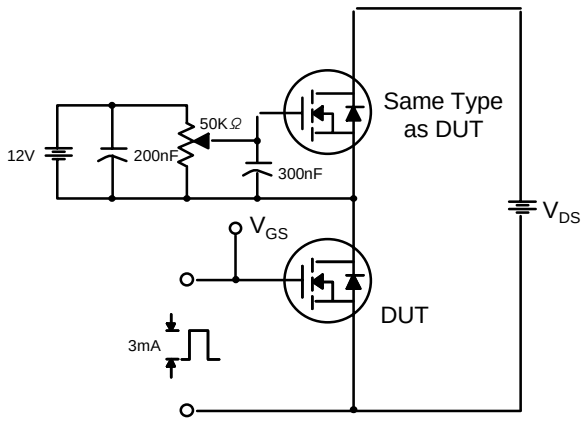
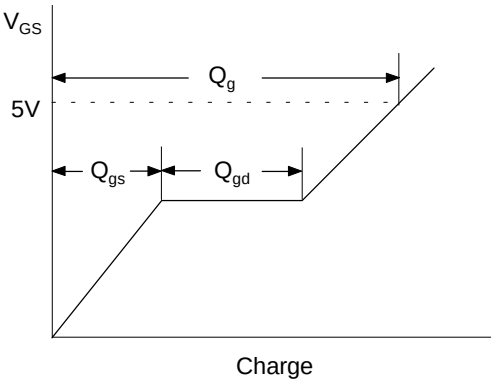


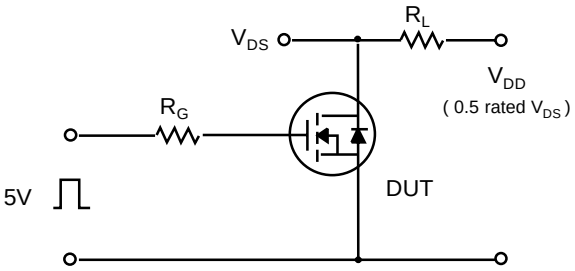
Figure 11. Thermal Response

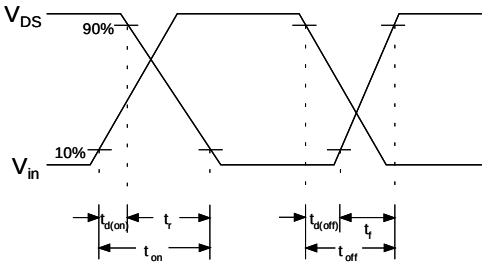
Gate Charge Test Circuit & Waveform



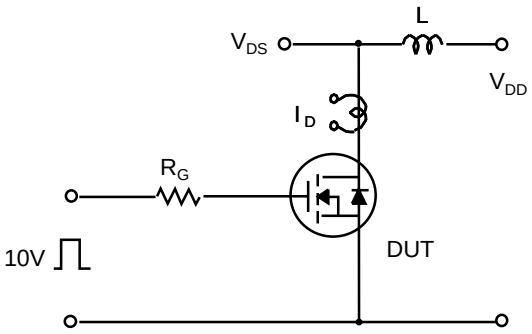


Resistive Switching Test Circuit & Waveforms

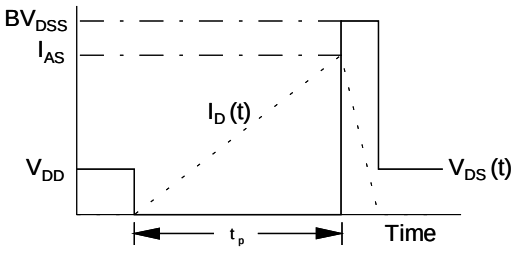




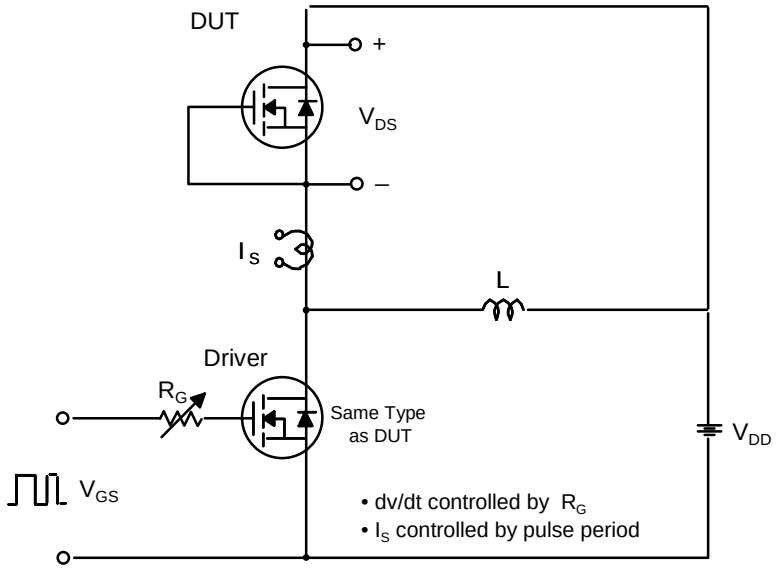
Unclamped Inductive Switching Test Circuit & Waveforms

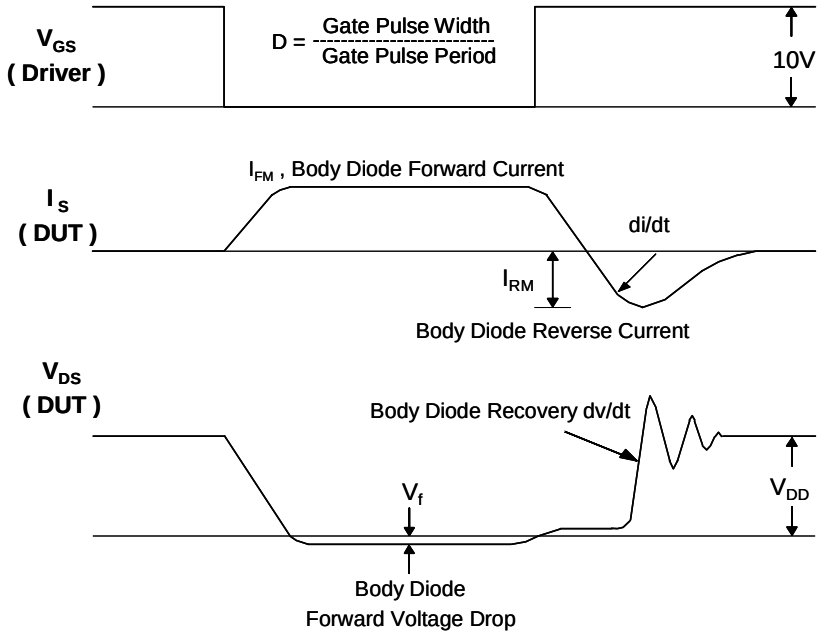


$$E_{AS} = \frac{1}{2} L_L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



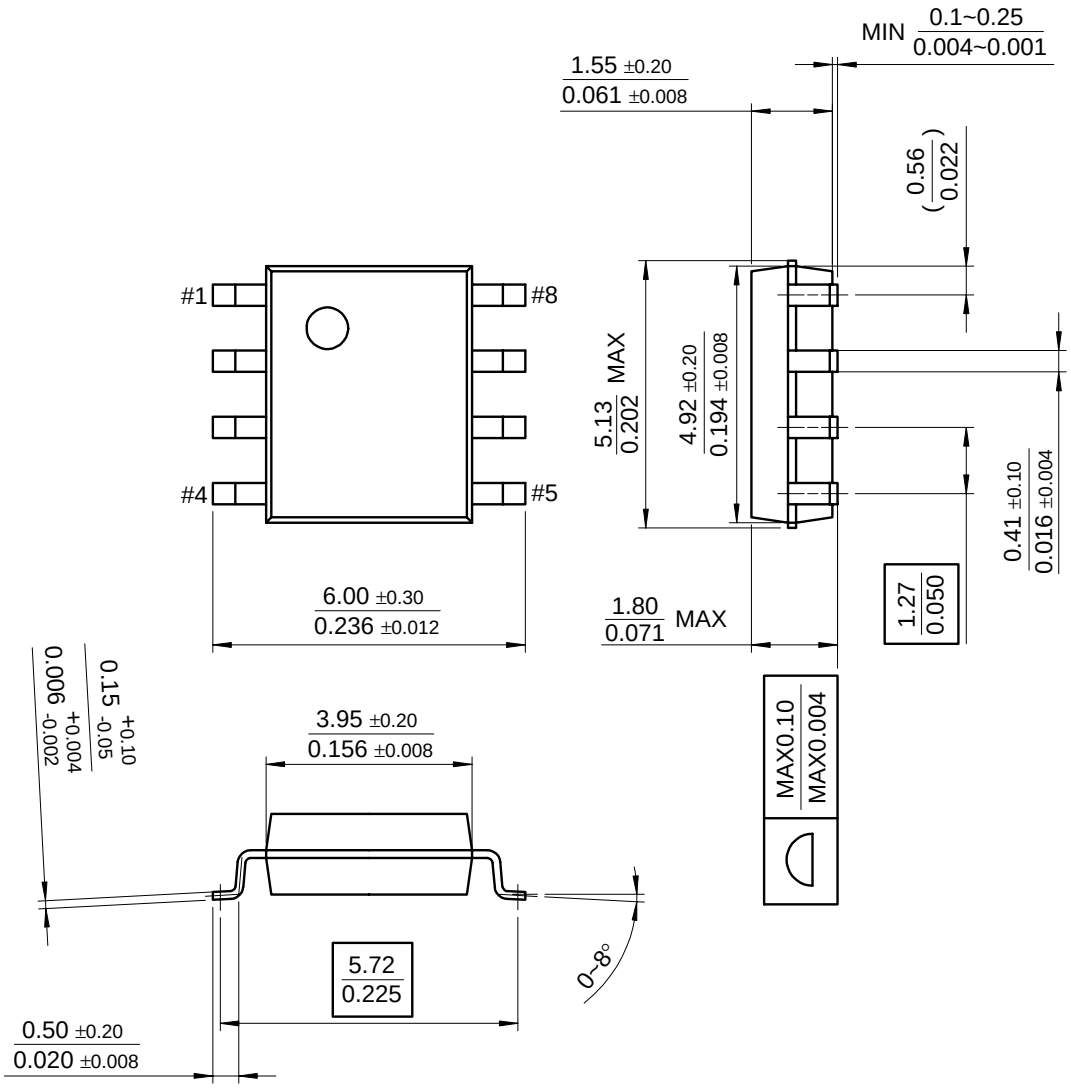
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimensions

8-SOP



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