

July 2000 PRELIMINARY

# **FDN5618P**

# 60V P-Channel Logic Level PowerTrench® MOSFET

### **General Description**

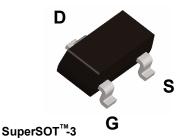
This 60V P-Channel MOSFET uses Fairchild's high voltage PowerTrench process. It has been optimized for power management applications.

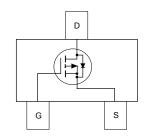
### **Applications**

- DC-DC converters
- Load switch
- Power management

### **Features**

- -1.25 A, -60 V.  $R_{DS(ON)} = 0.170 \Omega @ V_{GS} = -10 V$  $R_{DS(ON)} = 0.230 \Omega @ V_{GS} = -4.5 V$
- · Fast switching speed
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS}(\mbox{\scriptsize ON})}$





Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter		Ratings		
$V_{DSS}$	Drain-Source Voltage		-60	V	
$V_{GSS}$	Gate-Source Voltage		±20	V	
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	-1.25	А	
	- Pulsed		-10		
	Maximum Power Dissipation	(Note 1a)	0.5	W	
$P_D$		(Note 1b)	0.46		
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temp	perature Range	-55 to +150	°C	

### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	75	°C/W

**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
618	FDN5618P	7"	8mm	3000 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	acteristics	-			I	I
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$	-60			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A,Referenced to 25°C		-58		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -48 \text{ V},  V_{GS} = 0 \text{ V}$			-1	μА
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	$V_{GS} = 20V$ , $V_{DS} = 0 V$			100	nA
I <sub>GSSR</sub>	Gate–Body Leakage, Reverse	$V_{GS} = -20 \text{ V}$ $V_{DS} = 0 \text{ V}$			-100	nA
On Char	racteristics (Note 2)					
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	<b>–</b> 1	-1.6	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = -250 $\mu$ A,Referenced to 25°C		4		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$V_{GS} = -10 \text{ V},  I_D = -1.25 \text{ A}$ $V_{GS} = -4.5 \text{ V},  I_D = -1.0 \text{ A}$ $V_{GS} = -10 \text{ V}, I_D = -3 \text{ A} \text{ T}_J = 125^{\circ}\text{C}$		0.148 0.185 0.245	0.170 0.230 0.315	Ω
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = -10 \text{ V}, \qquad V_{DS} = -5 \text{ V}$	<b>-</b> 5			Α
<b>g</b> <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5 \text{ V}, \qquad I_{D} = -1.25 \text{ A}$		4.3		S
Dvnamio	Characteristics					
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -30 \text{ V},  V_{GS} = 0 \text{ V},$		430		pF
Coss	Output Capacitance	f = 1.0 MHz		52		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			19		pF
Switchin	ng Characteristics (Note 2)					•
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = -30 \text{ V}, \qquad I_{D} = -1 \text{ A},$		6.5	13	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = -10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		8	16	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			16.5	30	ns
t <sub>f</sub>	Turn-Off Fall Time			4	8	ns
$Q_g$	Total Gate Charge	$V_{DS} = -30 \text{ V}, \qquad I_{D} = -1.25 \text{ A},$		8.6	13.8	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = -10 V		1.5		nC
$Q_{gd}$	Gate-Drain Charge			1.3		nC
Drain-S	ource Diode Characteristics	and Maximum Ratings				
Is	Maximum Continuous Drain-Source				-0.42	Α
V <sub>SD</sub>	Drain–Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_S = -0.42  \text{(Note 2)}$		-0.7	-1.2	V

### Notes:

<sup>1.</sup>  $R_{\theta,JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta,JC}$  is guaranteed by design while  $R_{\theta,CA}$  is determined by the user's board design.



a) 250°C/W when mounted on a 0.02 in² pad of 2 oz. copper.

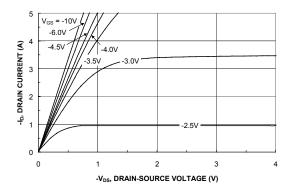


b) 270°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300~\mu\text{s},~\text{Duty Cycle} \leq 2.0$ 

### **Typical Characteristics**



2.2

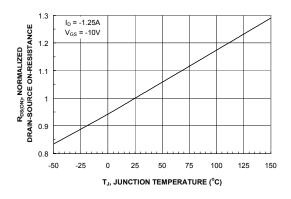
BANALIZED

ORANALIZED

OR

Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.



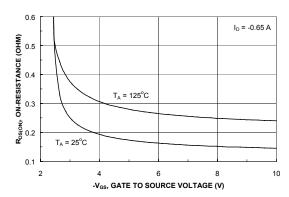
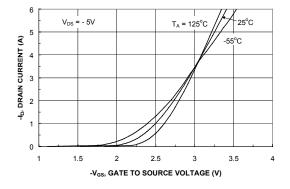


Figure 3. On-Resistance Variation withTemperature.

Figure 4. On-Resistance Variation with Gate-to-Source Voltage.



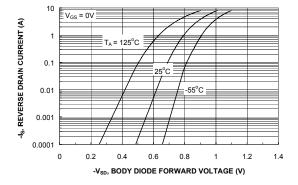
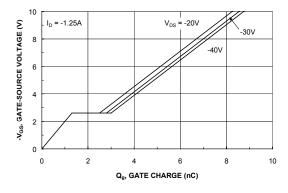


Figure 5. Transfer Characteristics.

Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### **Typical Characteristics**



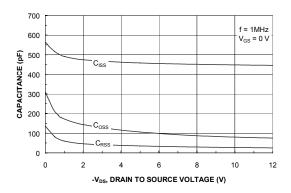


Figure 7. Gate Charge Characteristics.

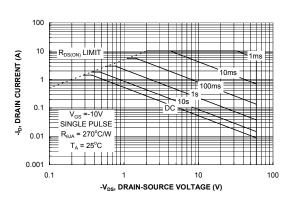


Figure 8. Capacitance Characteristics.

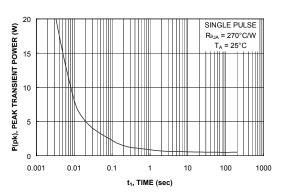


Figure 9. Maximum Safe Operating Area.



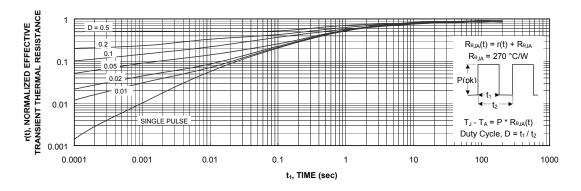
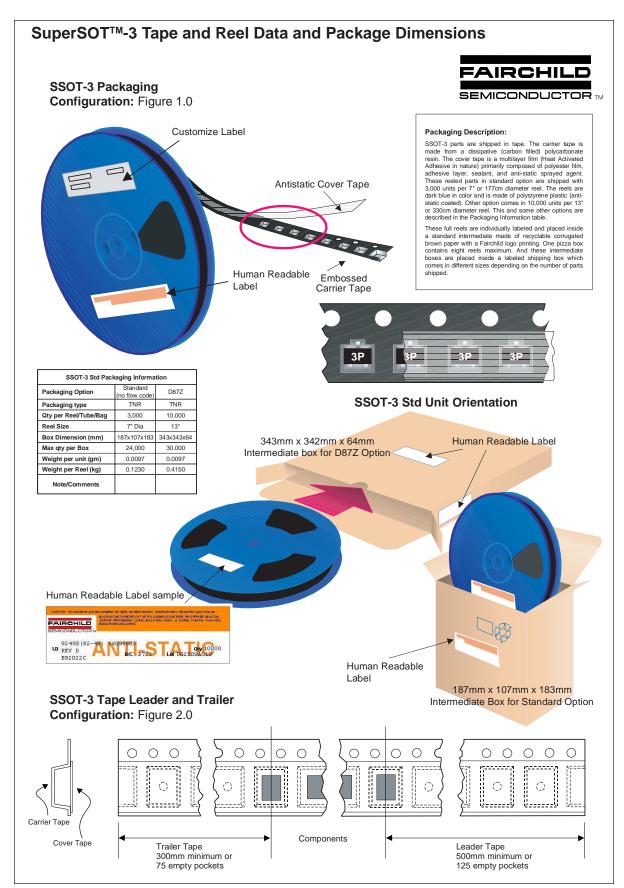
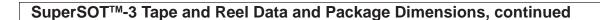


Figure 11. Transient Thermal Response Curve.

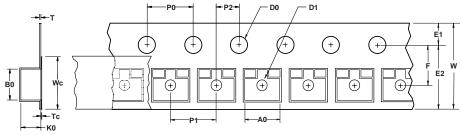
Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

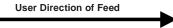




### **SSOT-3 Embossed Carrier Tape**

Configuration: Figure 3.0



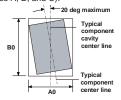


	Dimensions are in millimeter													
Pkg type	A0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	т	Wc	Тс
SSOT-3 (8mm)	3.15 +/-0.10	2.77 +/-0.10	8.0 +/-0.3	1.55 +/-0.05	1.125 +/-0.125	1.75 +/-0.10	6.25 min	3.50 +/-0.05	4.0 +/-0.1	4.0 +/-0.1	1.30 +/-0.10	0.228 +/-0.013	5.2 +/-0.3	0.06 +/-02

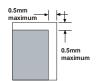
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation



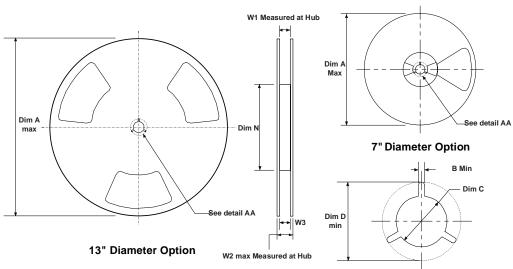
Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

DETAIL AA

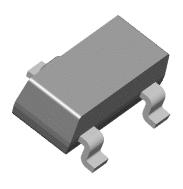
## **SSOT-3 Reel Configuration:** Figure 4.0

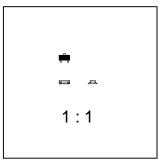


	Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)	
8mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9	
8mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.331 +0.059/-0.000 8.4 +1.5/0	0.567 14.4	0.311 - 0.429 7.9 - 10.9	

### SuperSOT™-3 Tape and Reel Data and Package Dimensions, continued

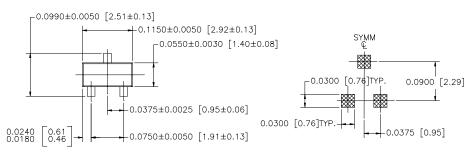
# SuperSOT™-3 (FS PKG Code 32)



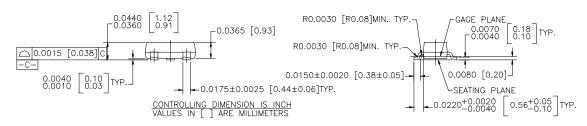


Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0097



LAND PATTERN RECOMMENDATION



NOTES: UNLESS OTHERWISE SPECIFIED

SUPER SOT , 3 LEADS

- 1. STANDARD LEAD FINISH TO BE 150 MICROINCHES / 3.81 MICROMETERS MINIMUM TIN/LEAD (SOLDER) ON COPPER.
- 2. NO JEDEC REGISTRATION AS OF DEC. 1995.

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