



July 1988  
 Revised August 2000

# 100324 Low Power Hex TTL-to-ECL Translator

## General Description

The 100324 is a hex translator, designed to convert TTL logic levels to 100K ECL logic levels. The inputs are compatible with standard or Schottky TTL. A common Enable (E), when LOW, holds all inverting outputs HIGH and holds all true outputs LOW. The differential outputs allow each circuit to be used as an inverting/non-inverting translator, or as a differential line driver. The output levels are voltage compensated over the full -4.2V to -5.7V range.

When the circuit is used in the differential mode, the 100324, due to its high common mode rejection, overcomes voltage gradients between the TTL and ECL ground systems. The  $V_{EE}$  and  $V_{TTL}$  power may be applied in either order.

The 100324 is pin and function compatible with the 100124 with similar AC performance, but features power dissipation roughly half of the 100124 to ease system cooling requirements.

## Features

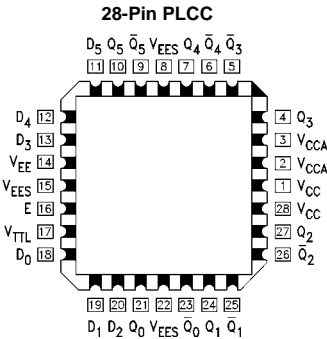
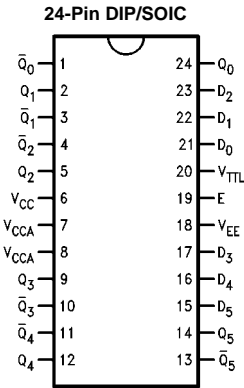
- Pin/function compatible with 100124
- Meets 100124 AC specifications
- 50% power reduction of the 100124
- Differential outputs
- 2000V ESD protection
- -4.2V to -5.7V operating range
- Available to MIL-STD-883
- Available to industrial grade temperature range (PLCC package only)

## Ordering Code:

Order Number	Package Number	Package Description
100324SC	M24B	28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
100324PC	N24E	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide
100324QC	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square
100324QI	V28A	28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square Industrial Temperature Range (-40°C to +85°C)

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

## Connection Diagrams



100324 Low Power Hex TTL-to-ECL Translator

## Pin Descriptions

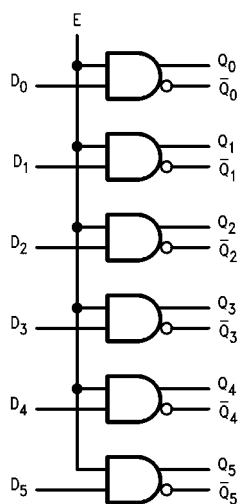
Pin Names	Description
$D_0$ – $D_5$	Data Inputs
E	Enable Input
$Q_0$ – $Q_5$	Data Outputs
$\overline{Q_0}$ – $\overline{Q_5}$	Complementary Data Outputs

## Truth Table

Inputs		Outputs	
$D_n$	E	$Q_n$	$\overline{Q_n}$
X	L	L	H
L	H	L	H
H	H	H	L

H = HIGH Voltage Level  
L = LOW Voltage Level

## Logic Diagram



**Absolute Maximum Ratings**(Note 1)

Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Maximum Junction Temperature ( $T_J$ )	+150°C
$V_{EE}$ Pin Potential to Ground Pin	-7.0V to +0.5V
$V_{TTL}$ Pin Potential to Ground Pin	-0.5V to +6.0V
Input Voltage (DC)	-0.5V to +6.0V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	≥2000V

**Recommended Operating Conditions**

Case Temperature ( $T_C$ )	0°C to +85°C
Commercial	-40°C to +85°C
Industrial	-5.7V to -4.2V
Supply Voltage ( $V_{EE}$ )	

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum rating. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** ESD testing conforms to MIL-STD-883, Method 3015.

**Commercial Version****DC Electrical Characteristics** (Note 3)

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = 0^\circ C$  to  $+85^\circ C$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$

Symbol	Parameter	Min	Typ	Max	Units	Conditions
$V_{OH}$	Output HIGH Voltage	-1025	-955	-870	mV	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$ Loading with 50Ω to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1705	-1620		
$V_{OHC}$	Output HIGH Voltage	-1035			mV	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$ Loading with 50Ω to -2.0V
$V_{OLC}$	Output LOW Voltage			-1610		
$V_{IH}$	Input HIGH Voltage	2.0		5.0	V	Guaranteed HIGH Signal for All Inputs
$V_{IL}$	Input LOW Voltage	0		0.8	V	Guaranteed LOW Signal for All Inputs
$V_{CD}$	Input Clamp Diode Voltage	-1.2			V	$I_{IN} = -18$ mA
$I_{IH}$	Input HIGH Current Data			20	μA	$V_{IN} = +2.4V$ , All Other Inputs $V_{IN} = GND$
	Enable			120		
$I_{IL}$	Input LOW Current Data	-0.9			mA	$V_{IN} = +5.5V$ , All Other Inputs = GND
	Enable	-5.4				$V_{IN} = +0.4V$ , All Other Inputs $V_{IN} = V_{IH}$
$I_{EE}$	$V_{EE}$ Power Supply Current	-70	-45	-22	mA	All Inputs $V_{IN} = +4.0V$
$I_{TTL}$	$V_{TTL}$ Power Supply Current		25	38	mA	All Inputs $V_{IN} = GND$

**Note 3:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

**DIP AC Electric Characteristics**

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	0.50	3.00	0.50	2.90	0.50	3.00	ns	Figures 2, 1
$t_{PHL}$	Data and Enable to Output								
$t_{TLH}$	Transition Time	0.45	1.80	0.45	1.80	0.45	1.80	ns	
$t_{THL}$	20% to 80%, 80% to 20%								

## Commercial Version (Continued) SOIC and PLCC AC Electrical Characteristics

$V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$

Symbol	Parameter	$T_C = 0^\circ C$		$T_C = +25^\circ C$		$T_C = +85^\circ C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay Data and Enable to Output	0.50	2.80	0.50	2.70	0.50	2.80	ns	Figures 2, 1
$t_{TLH}$ $t_{THL}$	Transition Time 20% to 80%, 80% to 20%	0.45	1.70	0.45	1.70	0.45	1.70	ns	
$t_{OSHL}$	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		0.95		0.95		0.95	ns	PLCC Only (Note 4)
$t_{OSLH}$	Maximum Skew Common Edge Output-to-Output Variation Data to Output Path		0.70		0.70		0.70	ns	PLCC Only (Note 4)
$t_{OST}$	Maximum Skew Opposite Edge Output-to-Output Variation Data to Output Path		1.60		1.60		1.60	ns	PLCC Only (Note 4)
$t_{PS}$	Maximum Skew Pin (Signal) Transition Variation Data to Output Path		1.20		1.20		1.20	ns	PLCC Only (Note 4)

**Note 4:** Output-to-Output Skew is defined as the absolute value of the difference between the actual propagation delay for any outputs within the same packaged device. The specifications apply to any outputs switching in the same direction either HIGH-to-LOW ( $t_{OSHL}$ ), or LOW-to-HIGH ( $t_{OSLH}$ ), or in opposite directions both HL and LH ( $t_{OST}$ ). Parameters  $t_{OST}$  and  $t_{PS}$  guaranteed by design.

**Industrial Version****DC Electrical Characteristics** (Note 5)
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $T_C = -40^{\circ}C$  to  $+85^{\circ}C$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

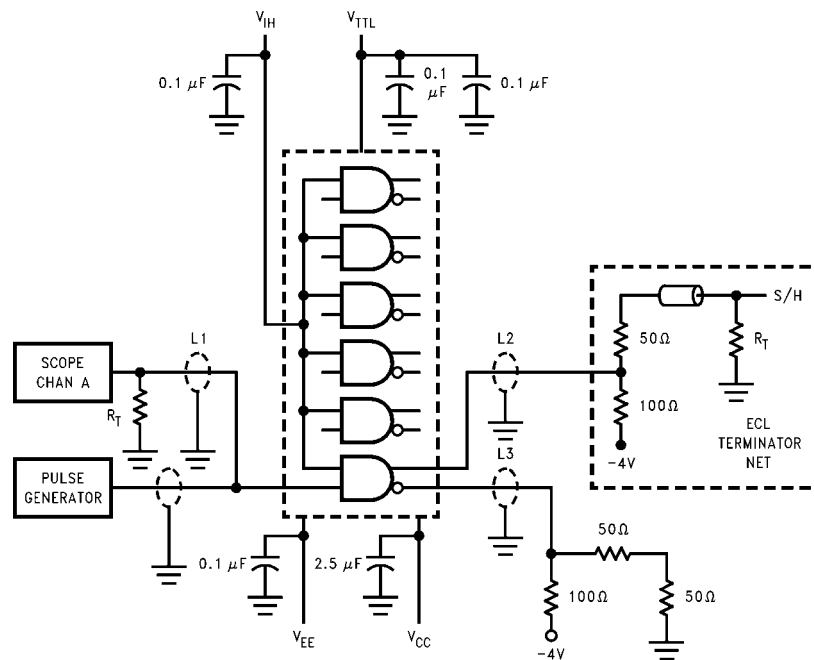
Symbol	Parameter	$T_C = -40^{\circ}C$		$T_C = 0^{\circ}C$ to $+85^{\circ}C$		Units	Conditions	
		Min	Max	Min	Max			
$V_{OH}$	Output HIGH Voltage	-1085	-870	-1025	-870	mV	$V_{IN} = V_{IH} (Max)$ or $V_{IL} (Min)$	Loading with 50 $\Omega$ to -2.0V
$V_{OL}$	Output LOW Voltage	-1830	-1575	-1830	-1620			
$V_{OHC}$	Output HIGH Voltage	-1095		-1035		mV	$V_{IN} = V_{IH} (Min)$ or $V_{IL} (Max)$	Loading with 50 $\Omega$ to -2.0V
$V_{OLC}$	Output LOW Voltage		-1565		-1610			
$V_{IH}$	Input HIGH Voltage	2.0	5.0	2.0	5.0	V	Guaranteed HIGH Signal for All Inputs	
$V_{IL}$	Input LOW Voltage	0	0.8	0	0.8	V	Guaranteed LOW Signal for All Inputs	
$V_{CD}$	Input Clamp Diode Voltage	-1.2		-1.2		V	$I_{IN} = -18$ mA	
$I_{IH}$	Input HIGH Current					$\mu A$	$V_{IN} = +2.4V$ , All Other Inputs $V_{IN} = GND$	
	Data		20		20			
	Enable		120		120			
$I_{IL}$	Input HIGH Current Breakdown Test, All Inputs		1.0		1.0	mA	$V_{IN} = +5.5V$ , All Other Inputs = GND	
	Input LOW Current						$V_{IN} = +0.4V$ , All Other Inputs $V_{IN} = V_{IH}$	
$I_{IL}$	Data	-0.9		-0.9		mA		
	Enable	-5.4		-5.4				
$I_{EE}$	$V_{EE}$ Power Supply Current	-70	-22	-70	-22	mA	All Inputs $V_{IN} = +4.0V$	
$I_{TTL}$	$V_{TTL}$ Power Supply Current		38		38		All Inputs $V_{IN} = GND$	

**Note 5:** The specified limits represent the "worst case" value for the parameter. Since these values normally occur at the temperature extremes, additional noise immunity and guardbanding can be achieved by decreasing the allowable system operating ranges. Conditions for testing shown in the tables are chosen to guarantee operation under "worst case" conditions.

**AC Electrical Characteristics**
 $V_{EE} = -4.2V$  to  $-5.7V$ ,  $V_{CC} = V_{CCA} = GND$ ,  $V_{TTL} = +4.5V$  to  $+5.5V$ 

Symbol	Parameter	$T_C = -40^{\circ}C$		$T_C = +25^{\circ}C$		$T_C = +85^{\circ}C$		Units	Conditions
		Min	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	0.50	2.80	0.50	2.70	0.50	2.80	ns	Figures 2, 1
$t_{PHL}$	Data and Enable to Output								
$t_{TLH}$	Transition Times	0.35	1.80	0.45	1.70	0.45	1.70	ns	Figures 2, 1
$t_{THL}$	20% to 80%, 80% to 20%								

## Test Circuit



### Note:

- $V_{CC}$ ,  $V_{CCA} = 0V$ ,  $V_{EE} = -4.5V$ ,  $V_{TTL} = +5.0V$ ,  $V_{IH} = +3.0V$
- L1, L2 and L3 = equal length 50Ω impedance lines
- $R_T = 50\Omega$  terminator internal to scope
- Decoupling 0.1  $\mu F$  from GND to  $V_{CC}$ ,  $V_{EE}$  and  $V_{TTL}$
- All unused outputs are loaded with 50Ω to -2V or with equivalent ECL terminator network
- $C_L$  = Fixture and stray capacitance  $\leq 3$  pF

FIGURE 1. AC Test Circuit

## Switching Waveform

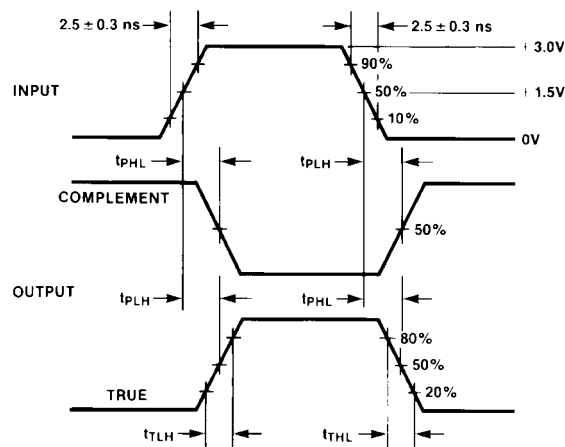
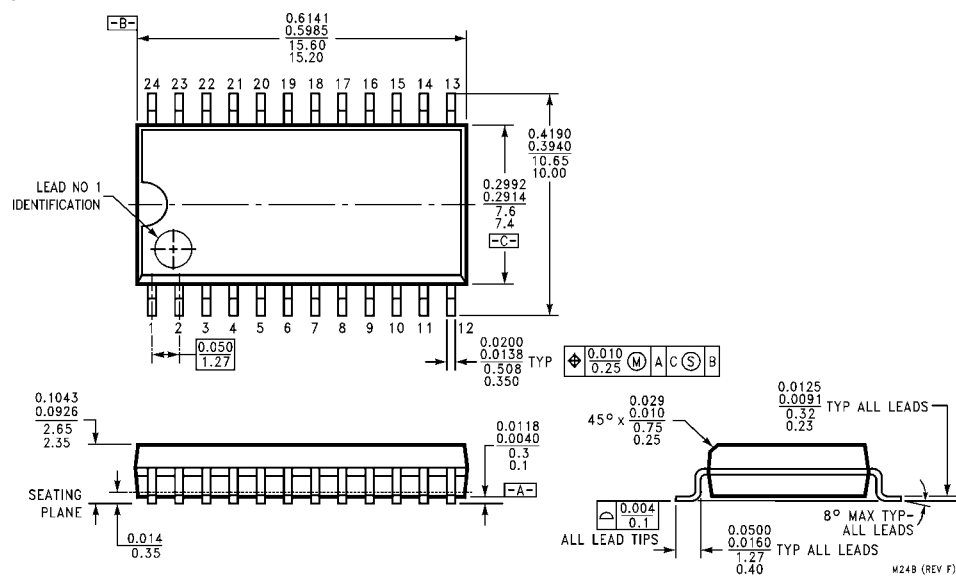
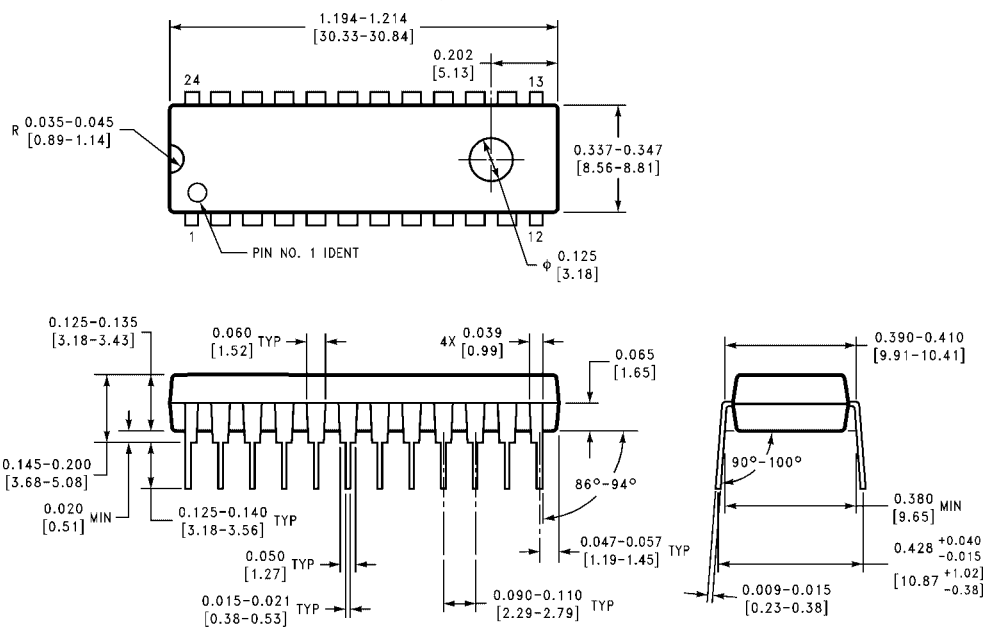


FIGURE 2. Propagation Delay and Transition Times

# Physical Dimensions inches (millimeters) unless otherwise noted

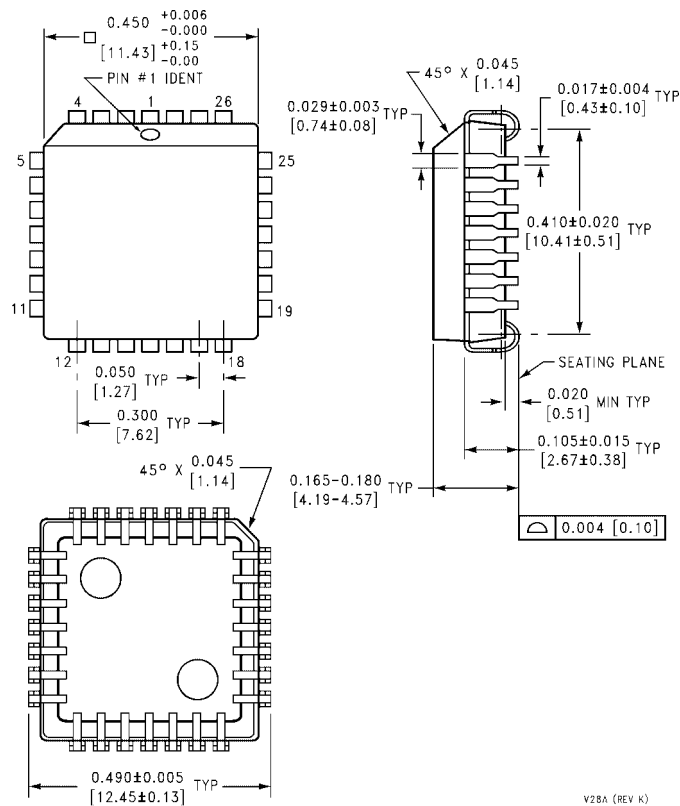


**28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M24B**



**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-010, 0.400 Wide  
Package Number N24E**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**28-Lead Plastic Lead Chip Carrier (PLCC), JEDEC MO-047, 0.450 Square)  
Package Number V28A**

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