EPSON

SRM20116LFT85/10

1M-Bit Static RAM

- Low Supply Current
- Access Time 85ns/100ns
- 65,536 Words×16-Bit Asynchronous
- Industrial Temperature Range

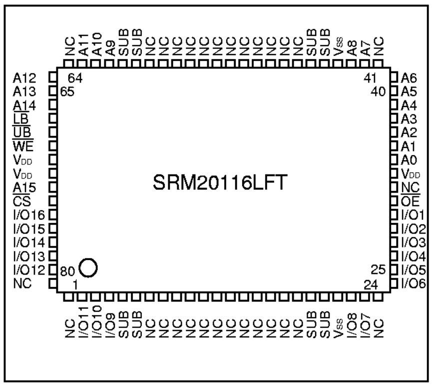
■ DESCRIPTION

The SRM20116LFT85/10 is a 65,536 words×16-bit asynchronous, static, random access memory on a monolithic CMOS chip. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refreshing circuit. It is possible to control the data width by the data byte control. Both the input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.
The temperature range of the SRM20116LFT85/10 is from –40 to +85 degree C, and it is suitable for the industrial products.

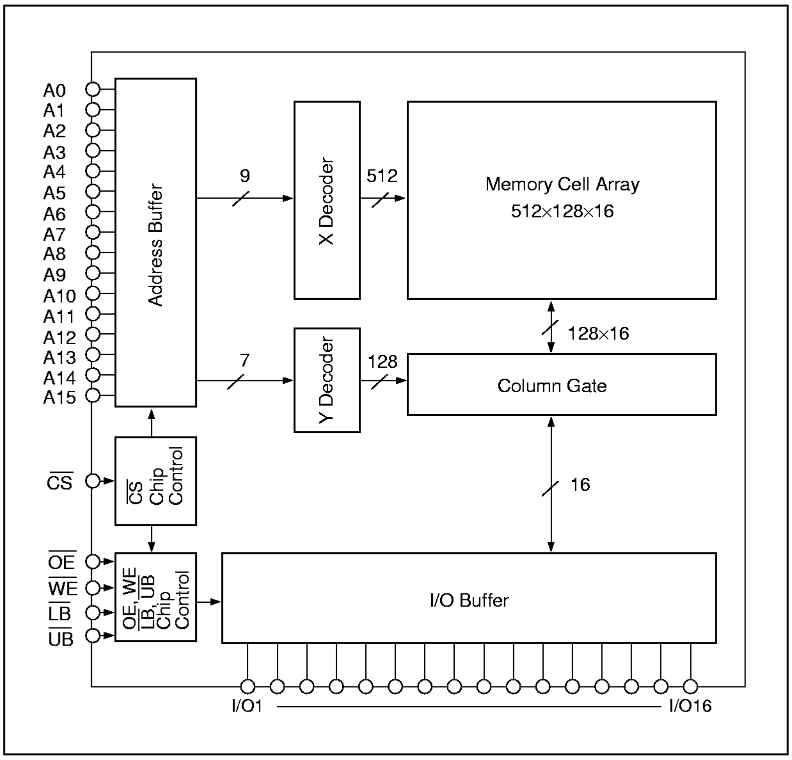
■ FEATURES

- Fast Access time SRM20116LFT85 85ns
  SRM20116LFT10 100ns
- Low supply current .... standby: 2µA (Typ.)
  operation: 35mA/MHz (Typ.)
- Completely static .... No clock required
- Single power supply .... 5V±10%
- TTL compatible inputs and outputs
- 3-state output with wired-OR capability
- Non-volatile storage with back-up batteries
- Package .... QFP5-80pin (plastic)

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ PIN DESCRIPTION

A0 to A15	Address Input
WE	Write Enable
OE	Output Enable
CS	Chip Select
LB	LOWER byte Enable
UB	UPPER byte Enable
I/O1 to 16	Data I/O
VDD	Power Supply (+5V)
Vss	Power Supply (0V)
SUB (VDD)	Substrate
NC	No connection

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	–0.5 to 7.0	V
Input voltage	V_I	–0.5*to 7.0	V
Input/Output voltage	$V_{I/O}$	–0.5*to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	–40 to 85	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (at lead)	—

*V_I, $V_{I/O}$ Min. = –3.0V (Pulse width is 50ns)

■ DC RECOMMENDED OPERATING CONDITIONS

(Ta = –40 to 85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
input voltage	V_{IH}	2.2	—	V_{DD}+0.3	V
	V_{IL}	–0.3*	—	0.8	V

*if pulse width is less than 50ns it is –3.0V

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 5V±10%, V_{SS} = 0V,Ta = –40 to 85°C)

Parameter	Symbol	Conditions	SRM20116LFT85			SRM20116LFT10			Unit
			Min.	Typ.*	Max.	Min.	Typ.*	Max.	
Input leakage	L_{LI}	V_I = 0 to V_{DD}	–1	—	1	–1	—	1	µA
Standby supply current	I_{DDS}	$\overline{CS}$ = V_{IH}	—	1.0	3.0	—	1.0	3.0	mA
	I_{DDS1}	$\overline{CS}$≥V_{DD}–0.2V	—	2	200	—	2	200	µA
Average operating current	I_{DDA}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA, tcyc = Min.	—	60	100	—	60	100	mA
	I_{DDA1}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA, tcyc = 1µA	—	35	70	—	35	70	mA
Operating supply current	I_{DDO}	V_I = V_{IL}, V_{IH} $I_{I/O}$ = 0mA	—	35	70	—	35	70	mA
Output leakage	I_{LO}	$\overline{CS}$ = V_{IH} or $\overline{WE}$ = V_{IL} or $\overline{OE}$ = V_{IH} $V_{I/O}$ = 0 to V_{DD}	–1	—	1	–1	—	–1	µA
High level output voltage	V_{OH}	I_{OH} = –1.0mA	2.4	—	—	2.4	—	—	V
Low level output voltage	V_{OL}	I_{OL} = 2.1mA	—	—	0.4	—	—	0.4	V

*Typical values are measured at Ta = 25°C and V_{DD} = 5.0V

■ Terminal Capacitance

(f = 1MHz, Ta = 25°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Address Capacitance	C_{ADD}	V_{ADD} = 0V	—	—	9	pF
Input Capacitance	C_I	V_I = 0V	—	—	10	pF
I/O Capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	10	pF

● AC Electrical Characteristics

❍ Read Cycle

(V_{DD} = 5V±10%, V_{SS} = 0V, Ta = –40 to 85°C)

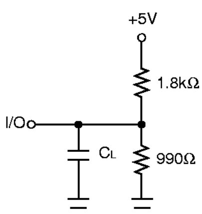
Parameter	Symbol	Condition	SRM20116LFT85		SRM20116LFT10		Unit
			Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	*1	85	—	100	—	ns
Address access time	t_{ACC}		—	85	—	100	ns
$\overline{CS}$ access time	t_{ACS}		—	85	—	100	ns
$\overline{OE}$ access time	t_{OE}		—	45	—	50	ns
$\overline{LB}$, $\overline{UB}$ access time	t_{AB}		—	45	—	50	ns
$\overline{CS}$ output st time	t_{CLZ}	*2	10	—	10	—	ns
$\overline{CS}$ output foating	t_{CHZ}		—	30	—	35	ns
$\overline{LB}$, $\overline{UB}$ output set time	t_{BLZ}		0	—	0	—	ns
$\overline{LB}$, $\overline{UB}$ output floating	t_{BHZ}		—	30	—	35	ns
$\overline{OE}$ output set time	t_{OLZ}		0	—	0	—	ns
$\overline{OE}$ output floating	t_{OHZ}		—	30	—	35	ns
Output hold time	t_{OH}	*1	10	—	10	–	ns

❍ Write Cycle

(V_{DD} = 5V±10%, V_{SS} = 0V, Ta = –40 to 85°C)

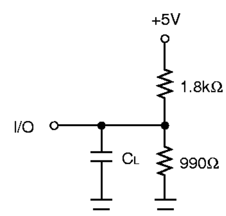
Parameter	Symbol	Condition	SRM20116LFT85		SRM20116LFT10		Unit
			Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	*1	85	—	100	—	ns
Chip select time	t_{CW}		70	—	80	—	ns
Address enable time	t_{AW}		70	—	80	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		65	—	75	—	ns
LB, UB select time	t_{BW}		65	—	75	—	ns
Address hold time	t_{WR}		0	—	0	—	ns
Data setup time	t_{DW}		40	—	40	—	ns
Data hold time	t_{DH}		0	—	0	—	ns
WE output floating	t_{WHZ}	*2	—	30	—	35	ns
WE output set time	t_{OW}		5	—	5	—	ns

*1 Test Conditions
1. Input pulse level: 0.6V to 2.4V
2. t_r = t_f = 5ns
3. Input and output timing reference levels: 1.5V
4. Output load C_L = 100pF



C_L = 100pF (Includes Jig Capacitance)

*2 Test Conditions
1. Input pulse level: 0.6V to 2.4V
2. t_r = t_f = 5ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels: ±200mA (the level displaced from stable output voltage level)
5. Output load C_L = 5pF



C_L = 5pF (Includes Jig Capacitance)

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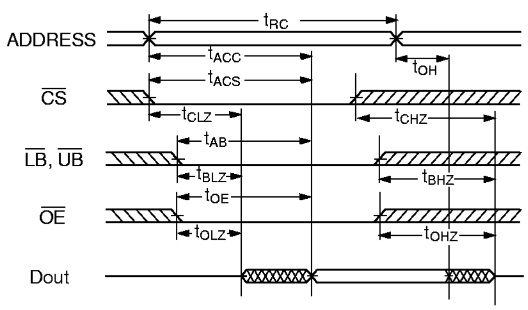
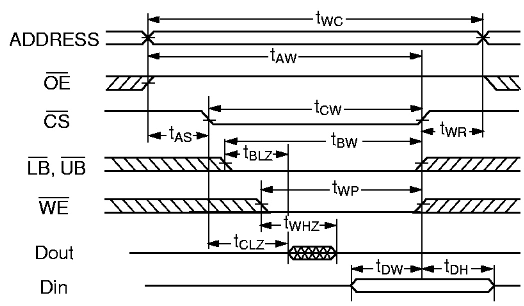
● AC Electrical Characteristics

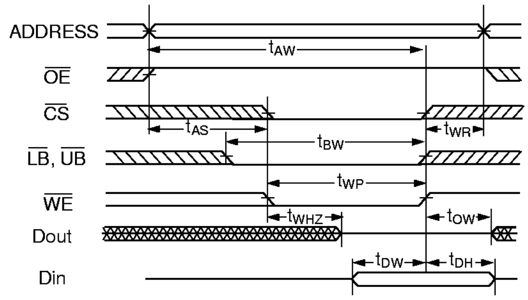
○Read Cylcle (Note: 1)



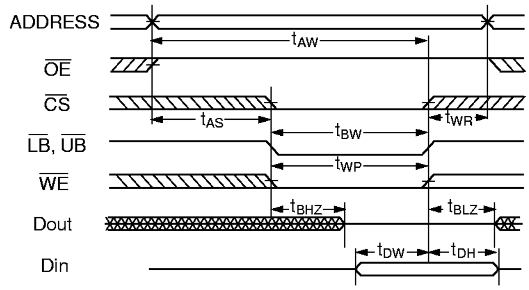
○Write Cycle (1) ($\overline{CS}$ control) (Note: 2)



○Write Cycle (2) ($\overline{WE}$ control) (Note: 3)



○Write Cycle (3) ($\overline{UB}$, $\overline{LB}$ control) (Note: 3)



Note : 1. During read cycle time, $\overline{WE}$ is to be "High" level.
2. In write cycle time that is controlled by $\overline{CS}$, output buffer is to be "Hi-Z" state if $\overline{OE}$ is "Low" level.
3. When output buffer is in output state, be careful that do not input the opposite signals to the output data.

■ FUNCTIONS

● Truth Table

$\overline{CS}$	$\overline{LB}$	$\overline{UB}$	$\overline{OE}$	$\overline{WE}$	I/O1 to 8	I/O9 to 16	MODE	I_{DD}
H	X	X	X	X	Hi–Z	Hi–Z	Standby	I_{DDS}, I_{DDS1}
L	L	H	X	L	Input data	Hi–Z	Write (Lower byte)	I_{DDA}, I_{DDA1}
L	H	L	X	L	Hi–Z	Input data	Write (Upper byte)	I_{DDA}, I_{DDA1}
L	L	L	X	L	Input data	Input data	Write (All data)	I_{DDA}, I_{DDA1}
L	L	H	L	H	Output data	Hi–Z	Read (Lower byte)	I_{DDA}, I_{DDA1}
L	H	L	L	H	Hi–Z	Output data	Read (Upper byte)	I_{DDA}, I_{DDA1}
L	L	L	L	H	Output data	Output data	Read (All data)	I_{DDA}, I_{DDA1}
L	L	L	H	H	Hi–Z	Hi–Z	Output disable	I_{DDA}, I_{DDA1}
L	H	H	X	X	Hi-Z	Hi–Z	Output disable	I_{DDA}, I_{DDA1}

X : High or Low

● Reading data

It is possible to control the data width by $\overline{LB}$/$\overline{UB}$.

(1) Reading data from lower

Data is able to be read when the address is set while holding $\overline{CS}$ = "Low", $\overline{OE}$ = "Low", $\overline{LB}$ = "Low" and $\overline{WE}$ = "High".

(2) Reading data from upper byte

Data is able to be read when the address is set while holding $\overline{CS}$ = "Low", $\overline{OE}$ = "Low", $\overline{UB}$ = "Low" and $\overline{WE}$ = "High".

(3) Reading all data

Data is able to be read when the address is set while holding $\overline{CS}$ = "Low", $\overline{OE}$ = "Low", $\overline{UB}$ = "Low" $\overline{LB}$ = "Low" and $\overline{WE}$ = "High".

Since I/O pins are in "Hi-Z" state when $\overline{OE}$ = "High", the data bus line can be used for any other objective, then access time apparently is able to be cut down.

● Writing data

(1) Writing data into lower byte

There are the following three ways of writing data into the memory.

i) Hold $\overline{WE}$ = "Low" and $\overline{LB}$ = "Low", set address and give "Low" pulse to $\overline{CS}$.

ii) Hold $\overline{CS}$ = "Low" and $\overline{LB}$ = "Low", set address and give "Low" pulse to $\overline{WE}$.

iii) Set address and give "Low" pulse to $\overline{CS}$, $\overline{WE}$ and $\overline{LB}$.

Anyway, data on I/O pins are latched up into the memory cell during $\overline{CS}$, $\overline{WE}$, and $\overline{LB}$ are "Low".

(2) Writing data into upper byte

There are the following three ways of writing data into the memory.

i) Hold $\overline{WE}$ = "Low" and $\overline{UB}$ = "Low", set address and give "Low" pulse to $\overline{CS}$.

ii) Hold $\overline{CS}$ = "Low" and $\overline{UB}$ = "Low", set address and give "Low" pulse to $\overline{WE}$.

iii) Set address and give "Low" pulse to $\overline{CS}$, $\overline{WE}$ and $\overline{UB}$.

Anyway, data on I/O pins are latched up into the memory cell during $\overline{CS}$, $\overline{WE}$, and $\overline{UB}$ are "Low".

(3) Writing all data

There are the following three ways of writing data into the memory.

i) Hold $\overline{WE}$ = "Low", $\overline{LB}$ = "Low" and $\overline{UB}$ = "Low", set address and give "Low" pulse to $\overline{CS}$.

ii) Hold $\overline{CS}$ = "Low", $\overline{LB}$ = "Low" and $\overline{UB}$ = "Low", set address and give "Low" pulse to $\overline{WE}$.

iii) Set address and give "Low" pulse to $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ and $\overline{UB}$.

Anyway, data on I/O pins are latched up into the memory cell during $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ and $\overline{UB}$ are "Low". As data I/O pins are in "Hi-Z" when any of $\overline{CS}$ or $\overline{OE}$ is "High" level, the contention on the data bus can be avoided. But during I/O pins are in the output state, the data that is opposite to the output data should not be given.

● Standby mode

When $\overline{CS}$ is "High" level, the chip is in the standby mode which has retaining data operation. In this case data I/O pins are Hi-Z, and all inputs of addresses, $\overline{WE}$, $\overline{OE}$ and all input data are inhibited. When $\overline{CS}$ level are in the range over V_{DD}-0.2V, there is almost no current flow except throungh the high resistance parts of the memory.

● Data retention at low voltage

In case of the data retention in the standby mode, the power supply can be gone down till the specified voltage. But it is impossible to write or read in this mode.

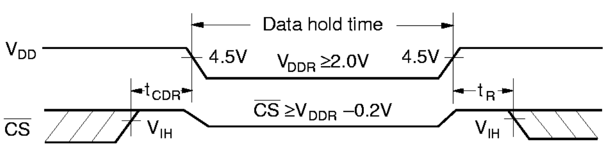
■ DATA RETENTION CHARACTERISTIC WITH LOW VOLTAGE POWER SUPPLY

(V_{SS} = 0V, Ta = –40 to 85°C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	V_{DD} = 3V $\overline{CS} \geq V_{DD}-0.2V$	—	1*	100	µA
Chip select • data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		5	—	—	ms

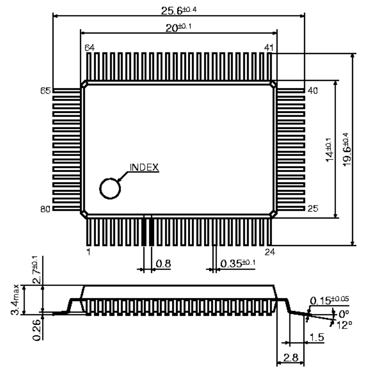
* Ta = 25°C

Data retention timing ($\overline{CS}$ Control)



■ PACKAGE DIMENSIONS

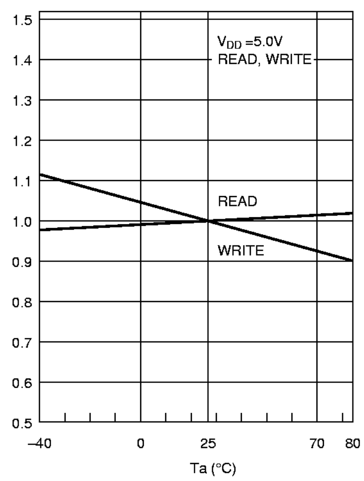
Plastic QFP5-80pin



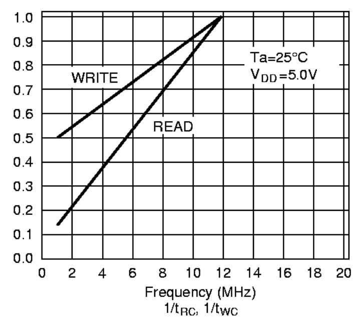
Unit : mm

■ CHARACTERISTICS CURVES

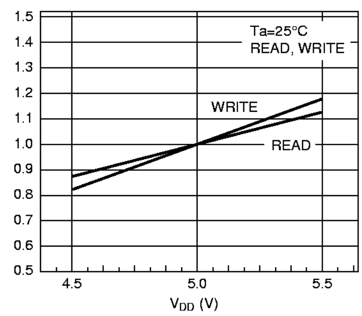
Normalized I_{DDS1}-Ta



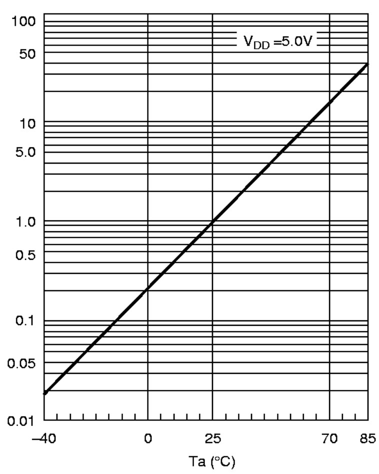
Normalized I_{DDA}-Frequency



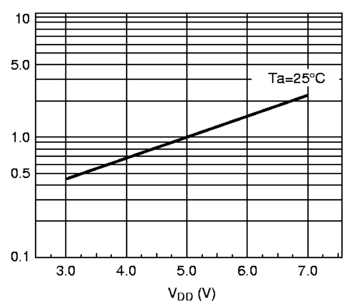
Normalized I_{DDA}-V_{DD}



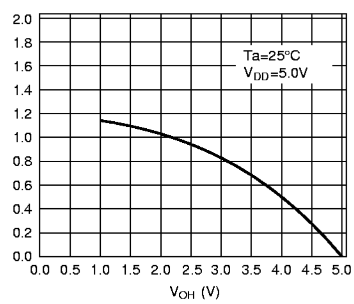
Normalized I_{DDA}-Ta



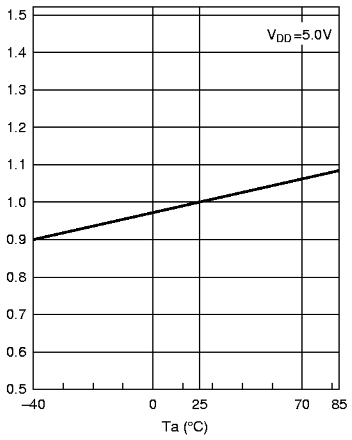
Normalized I_{DDS1}-V_{DD}



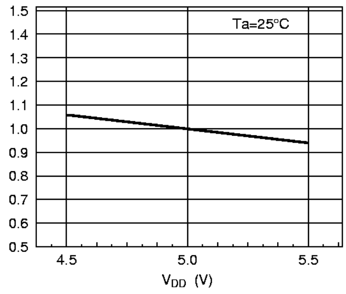
Normalized I_{OH}-V_{OH}



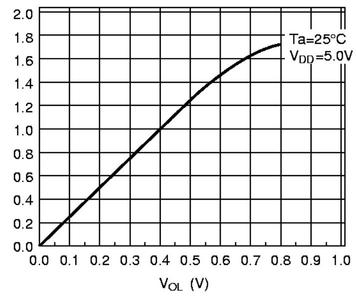
Normalized $\frac{t_{ACS}}{t_{ACC}}$ -Ta



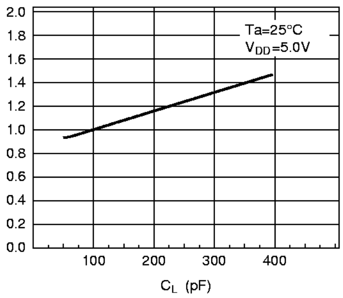
Normalized $\frac{t_{ACS}}{t_{ACS}}$ -VDD



Normalized I_{OL}-V_{OL}



Normalized $\frac{t_{ACC}}{t_{ACS}}$ -C_L



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