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<i>Bob Hu</i>		ISSUE : NOV.27, 2007
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<i>David Chang</i>		VERSION : 2
CUSTOMER ACCEPTANCE SPECIFICATIONS		
MODEL NO. : <u>ET028002DMU</u> (RoHS) FOR MESSRS : _____		
CUSTOMER'S APPROVAL DATE : _____ BY : _____		

RECORDS OF REVISION

DOC . FIRST ISSUE

NOV.05, 2007

DATE

REVISED
PAGE
NO.

SUMMARY

NOV.27, 2007

1

2. MECHANICAL SPECIFICATIONS

(1)DISPLAY SIZE (inch) : 2.8" → DIAGONALS : 2.8 inch

ADD (10) INTERFACE MODE : RGB : 16/18 BIT

MCU : 8/16/18 BIT PARALLEL DATA

SPI DATA

2

3.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	REMARK
POWER SUPPLY FOR DIGITAL	IOVCC	-0.3	3.3	V	→
PARAMETER	SYMBOL	MIN.	MAX.	UNIT	REMARK
POWER SUPPLY FOR DIGITAL	IOVCC	-0.3	4.6	V	

3

ADD 4.2 AC CHARACTERISTICS

9, 10

5. OPTICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
VIEWING ANGLE	HOR.	0x+	70	75	—	deg.	—
		0x-	65	70	—		
	VER.	0y+	70	75	—		
		0y-	50	55	—		
CONTRAST RATIO	CR	VIEWING NORMAL AUNLE 0x = 0° 0y = 0°	400	500	—	—	—
RESPONSE TIME		tr (rise)	—	10	20	ms	—
		tf (fall)	—	15	30		
THE BRIGHTNESS OF MODULE	B		300	350	—	cd/m²	→
COLOR OF CIE COORDINATE	WHITE	X	0.290	0.310	0.330	—	—
		Y	0.321	0.341	0.361		
	RED	X	0.635	0.655	0.675		
		Y	0.309	0.329	0.349		
	GREEN	X	0.292	0.312	0.332		
		Y	0.555	0.575	0.595		
	BLUE	X	0.114	0.134	0.154		
		Y	0.115	0.135	0.155		

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT	REMARK
VIEWING ANGLE	HOR.	0x+	70	75	—	deg.	(3)
		0x-	65	70	—		
	VER.	0y+	70	75	—		
		0y-	50	55	—		
CONTRAST RATIO	CR	VIEWING NORMAL AUNLE 0x = 0° 0y = 0°	400	500	—	—	(4)
RESPONSE TIME		tr (rise)	—	10	20	ms	(5)
		tf (fall)	—	15	30		
THE BRIGHTNESS OF MODULE	B	NTSC : 60% VIEWING NORMAL AUNLE 0x = 0° 0y = 0°	300	350	—	cd/m²	(6)
COLOR OF CIE COORDINATE	WHITE	Wx	0.290	0.310	0.330	—	(7)
		Wy	0.321	0.341	0.361		
	RED	Rx	0.635	0.655	0.675		
		Ry	0.309	0.329	0.349		
	GREEN	Gx	0.292	0.312	0.332		
		Gy	0.555	0.575	0.595		
	BLUE	Bx	0.114	0.134	0.154		
		By	0.115	0.135	0.155		

ADD NOTE (2)~(7)

ADD 5.2 THE TEST METHOD OF BRIGHTNESS AND UNIFORMITY

ADD 5.3 THE CALCULATING METHOD OF UNIFORMITY

12

7. BLOCK DIMENSIONS

MODIFY IC GATE NO.

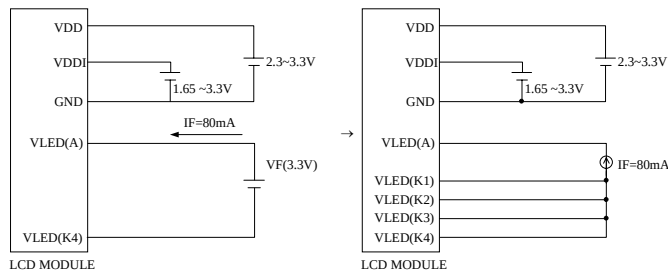
14, 15

9. INTERFACE SIGNAL

UPDATE PIN 17~PIN 34 FUNCTION

16

10. POWER SUPPLY



—

DELETE 12.3 DEFINITION OF OPTICAL CHARACTERISTICS

DELETE 12.4 OUTLINE OF OPTICAL MEASURING SYSTEM

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12.4.1 STANDARD SPECIFICATIONS FOR RELIABILITY OF LCD MODULE

NO. 4 : 40°C → 50°C, NO. 5 : 40°C → 60°C

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1. GENERAL SPECIFICATIONS

1.1 APPLICATION NOTES FOR CONTROLLER/DRIVER PLEASE REFER TO :

HIMAX HX8347-A

1.2 MATERIAL SAFETY DESCRIPTION

ASSEMBLIES SHALL COMPLY WITH EUROPEAN ROHS REQUIREMENTS, INCLUDING PROHIBITED MATERIALS/COMPONENTS CONTAINING LEAD, MERCURY, CADMIUM, HEXAVALENT CHROMIUM, POLYBROMINATED BIPHENYLS (PBB) AND POLYBROMINATED DIPHENYL ETHERS (PBDE)

2. MECHANICAL SPECIFICATIONS

(1) DIAGONALS	2.8 inch
(2) NUMBER OF DOTS	240W * (RGB) * 320H DOTS
(3) MODULE SIZE	50W * 69.2H * 3(D) mm (WITHOUT FPC SIZE)
(4) ACTIVE AREA	43.2W * 57.6H mm (LCD)
(5) PIXEL SIZE	0.18W * 0.18H mm
(6) LCD TYPE	TFT , TRANSMISSIVE
(7) COLOR	262K (18BIT)
(8) VIEWING DIRECTION	12 O'CLOCK
(9) BACK LIGHT	LED , COLOR : WHITE
(10) INTERFACE MODE	RGB : 16/18 BIT MCU : 8/16/18 BIT PARALLEL DATA SPI DATA

3. ABSOLUTE MAXIMUM RATINGS

3.1 ELECTRICAL ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	REMARK
POWER SUPPLY FOR DIGITAL	IOVCC	-0.3	4.6	V	
POWER SUPPLY FOR ANALOG	VCI	-0.3	4.6	V	
INPUT VOLTAGE	V_{IN}	-0.3	$V_{CI}+0.3$	V	

3.2 ENVIRONMENTAL ABSOLUTE MAXIMUM RATINGS.

I T E M	OPERATING		STORAGE		REMARK
	MIN.	MAX.	MIN.	MAX.	
AMBIENT TEMPERATURE	-20°C	70°C	-30°C	80°C	NOTE (2), (3)
HUMIDITY	—	—	—	—	WITHOUT CONDENSATION NOTE (4)
VIBRATION	—	2.45m/S ² (0.25G)	—	11.76m/S ² (1.2 G)	5~20Hz , 1HR 20~500Hz(20Hz) , 1HR 20~500Hz(500Hz) , 1HR X,Y,Z,TOTAL 3HR
SHOCK	—	29.4 m/S ² (3G)	—	490m/S ² (50 G)	10 m SECONDS XYZ DIRECTIONS 1 TIME EACH
CORROSIVE GAS	NOT ACCEPTABLE		NOT ACCEPTABLE		

NOTE (2) : Ta AT -30°C : 48HR MAX .

80°C : 168HR MAX .

NOTE (3) : BACKGROUND COLOR CHANGES SLIGHTLY DEPENDING ON AMBIENT
TEMPERATURE THIS PHENOMENON IS REVERSIBLE.

NOTE (4) : Ta ≤ 60°C : 90%HR (96RH MAX .)

Ta > 60°C : ABSOLUTE HUMIDITY MUST BE LOWER THAN THE HUMIDITY OF
90%RH AT 60°C.(96 HR MAX.)

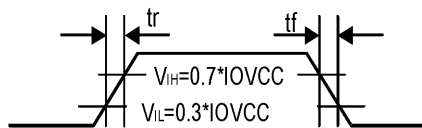
(VSSA=0V, IOVCC=1.65V to 2.50V, VCI=2.3V to 2.9V, Ta = -30 to 70°C)

SIGNAL	SYMBOL	PARAMETER	MIN.	MAX.	UNIT	DESCRIPTION
DNC_SCL	t_{AST} t_{AHT}	ADDRESS SETUP TIME ADDRESS HOLD TIME (WRITE/READ)	10 10	— —	ns	
NCS	t_{CHW} t_{CS} t_{RCSFM} t_{CSF} t_{CSH}	CHIP SELECT "H" PULSE WIDTH CHIP SELECT SETUP TIME (WRITE) CHIP SELECT SETUP TIME CHIP SELECT WAIT TIME (WRITE/READ) CHIP SELECT HOLD TIME	0 35 355 10 10	— — — — —	ns	
NWR_RNW	t_{WC} t_{WRH} t_{WRL}	WRITE CYCLE CONTROL PULSE "H" DURATION CONTROL PULSE "L" DURATION	100 35 35	— — —	ns	
NRD_E	t_{RCFM} t_{RDHFM} t_{RDLFM}	READ CYCLE CONTROL PULSE "H" DURATION CONTROL PULSE "L" DURATION	450 90 355	— — —	ns	WHEN READ FROM GRAM
D17 TO D0	t_{DST} t_{DHT} t_{RATFM} t_{ODH}	DATA SETUP TIME DATA HOLD TIME READ ACCESS TIME OUTPUT DISABLE TIME	15 10 — 20	— — 340 80	ns	FOR MAXIMUM CL=30pF FOR MINIMUM CL=8pF

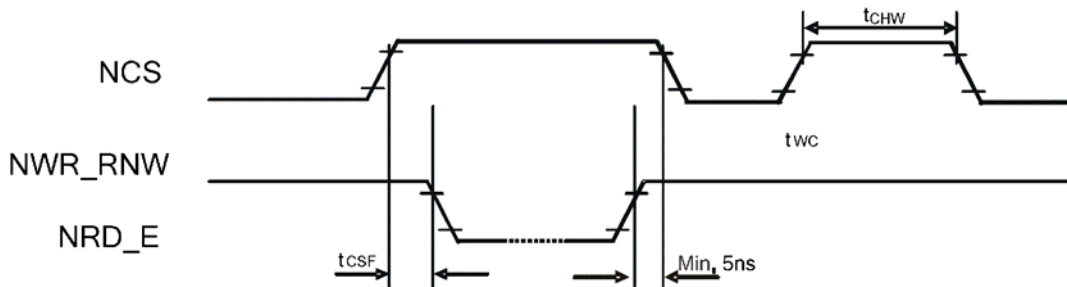
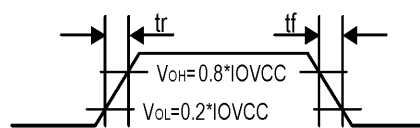
NOTE : THE INPUT SIGNAL RISE TIME AND FALL TIME (TR, TF) IS SPECIFIED AT 15 NS OR LESS.

LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF IOVCC FOR INPUT SIGNALS.

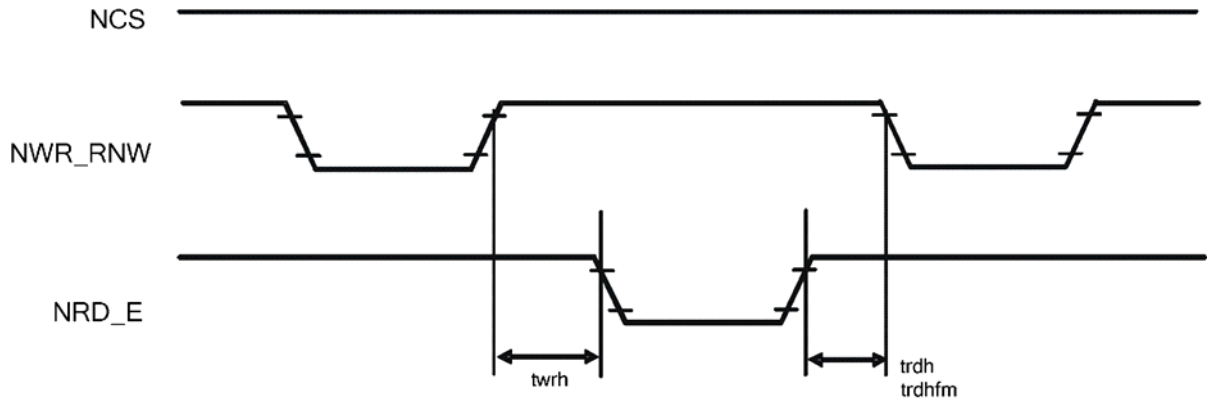
Input Signal Slope



Output Signal Slope

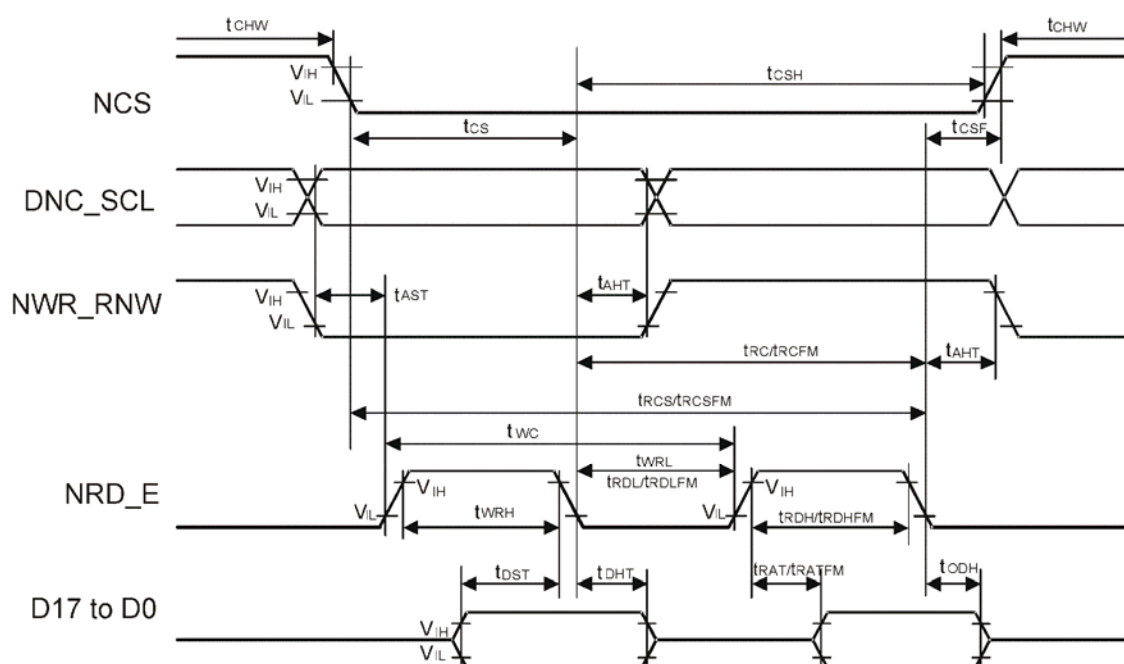


NOTE : LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF IOVCC



NOTE : LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF IOVCC

4.2.2 PARALLEL INTERFACE CHARACTERISTICS (6800-SERIES MPU)

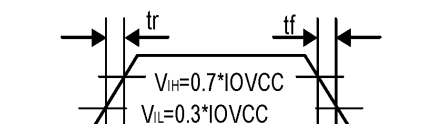


(VSSA=0V, IOVCC=1.65V to 2.50V, VCI=2.3V to 2.9V, Ta = -30 to 70°C)

SIGNAL	SYMBOL	PARAMETER	MIN.	MAX.	UNIT	DESCRIPTION
DNC_SCL	t _{AST}	ADDRESS SETUP TIME	10	—	ns	
	t _{AHT}	ADDRESS HOLD TIME (WRITE/READ)	10	—	ns	
NCS	t _{CHW}	CHIP SELECT “H” PULSE WIDTH	0	—		
	t _{CS}	CHIP SELECT SETUP TIME (WRITE)	35	—		
	t _{RCSFM}	CHIP SELECT SETUP TIME	355	—	ns	
	t _{CSF}	CHIP SELECT WAIT TIME (WRITE/READ)	10	—		
	t _{CSH}	CHIP SELECT HOLD TIME	10	—		
NWR_RNW	t _{WC}	WRITE CYCLE	100	—		
	t _{WRH}	CONTROL PULSE “H” DURATION	35	—	ns	
	t _{WRL}	CONTROL PULSE “L” DURATION	35	—		
NRD_E	t _{RCFM}	READ CYCLE	450	—		
	t _{RDHFM}	CONTROL PULSE “H” DURATION	90	—	ns	WHEN READ
	t _{RDLFM}	CONTROL PULSE “L” DURATION	355	—		FROM GRAM
D17 TO D0	T _{dst}	DATA SETUP TIME	10	—		
	t _{DHT}	DATA HOLD TIME	10	—		
	t _{RAT}	READ ACCESS TIME (ID)	—	40		
	t _{RATFM}	READ ACCESS TIME (FM)	—	340	ns	FOR MAXIMUM CL=30pF FOR MINIMUM CL=8pF
	t _{ODH}	OUTPUT DISABLE TIME	20	80		

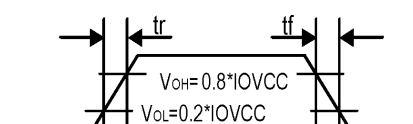
NOTE : THE INPUT SIGNAL RISE TIME AND FALL TIME (TR, TF) IS SPECIFIED AT 15 NS OR LESS.
LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF IOVCC FOR INPUT SIGNALS.

Input Signal Slope

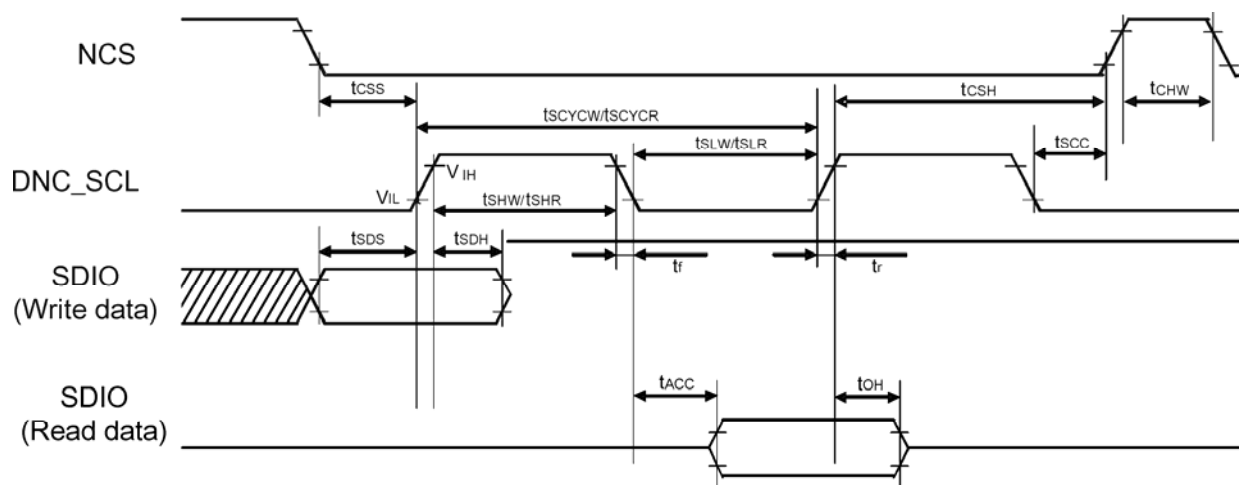


Note: VDDI means IOVCC-VSS

Output Signal Slope



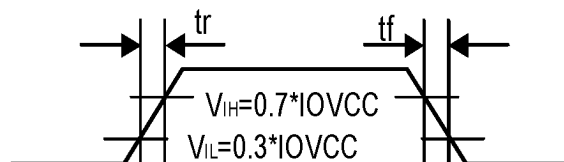
4.2.3 SERIAL INTERFACE CHARACTERISTICS



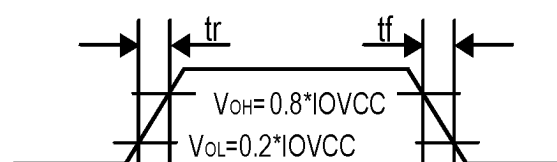
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
SERIAL CLOCK CYCLE (WRITE)	t_{SCYCW}	DNC_SCL	100	—	—	ns
DNC_SCL "H" PULSE WIDTH (WRITE)	t_{SHW}		35	—	—	
DNC_SCL "L" PULSE WIDTH (WRITE)	t_{SLW}		35	—	—	
DATA SETUP TIME (WRITE)	t_{SDS}	SDI	30	—	—	ns
DATA HOLD TIME (WRITE)	t_{SDH}		30	—	—	
SERIAL CLOCK CYCLE (READ)	t_{SCYCR}	DNC_SCL	150	—	—	ns
DNC_SCL "H" PULSE WIDTH (READ)	t_{SHR}		60	—	—	
DNC_SCL "L" PULSE WIDTH (READ)	t_{SLR}		60	—	—	
ACCESS TIME	t_{ACC}	SDO FOR MAXIMUM CL=30pF FOR MINIMUM CL=8pF	45	—	100	ns
OUTPUT DISABLE TIME	t_{OH}	SDO FOR MAXIMUM CL=30pF FOR MINIMUM CL=8pF	15	—	100	ns
DNC_SCL TO CHIP SELECT	t_{SCC}	DNC_SCL, NCS	15	—	—	ns
NCS "H" PULSE WIDTH	t_{CHW}	NCS	45	—	—	ns
CHIP SELECT SETUP TIME	t_{CSS}	NCS	60	—	—	ns
CHIP SELECT HOLD TIME	t_{CSH}		65	—	—	

NOTE : THE INPUT SIGNAL RISE TIME AND FALL TIME (t_r , t_f) IS SPECIFIED AT 15 NS OR LESS.
LOGIC HIGH AND LOW LEVELS ARE SPECIFIED AS 30% AND 70% OF IOVCC FOR INPUT SIGNALS.

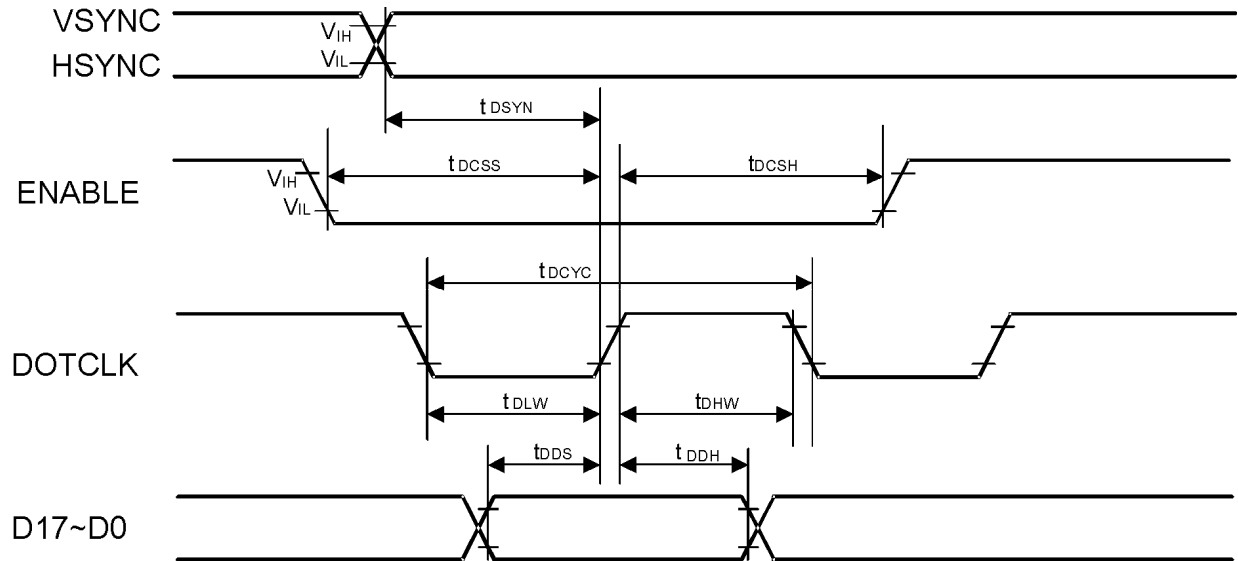
Input Signal Slope



Output Signal Slope



4.2.4 RGB INTERFACE CHARACTERISTICS



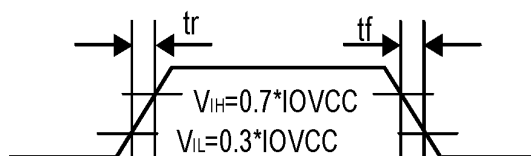
SYMBOL	PARAMETER	CONDITIONS	RELATED PINS	MIN.	TYP.	MAX.	UNIT
t_{DCYC}	DOTCLK CYCLE TIME	VRR = Min. 50 Hz Max. 65 Hz	DOTCLK	60 (NOTE2)	—	226 (NOTE3)	ns
t_{DLW} t_{CHW}	DOTCLK LOW TIME DOTCLK HIGH TIME			15 15	— —	— —	ns
t_{DDS} t_{DDH}	RGB DATA SETUP TIME RGB DATA HOLD TIME		DOTCLK, D17-D0	15 15	— —	— —	ns
t_{DCSS} t_{DCSH}	ENABLE SETUP TIME ENABLE HOLD TIME		ENABLE	15 15	— —	— —	ns
t_{DSYN}	SYNC SETUP TIME		DOTCLK, HSYNC, VSYNC	15	—	—	ns

NOTE : (1) THE INPUT SIGNAL RISE TIME AND FALL TIME (t_r , t_f) IS SPECIFIED AT 15 NS OR LESS.

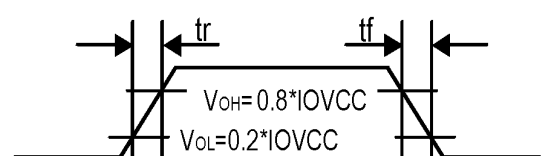
(2) 16.6MHz

(3) 4.4MHz

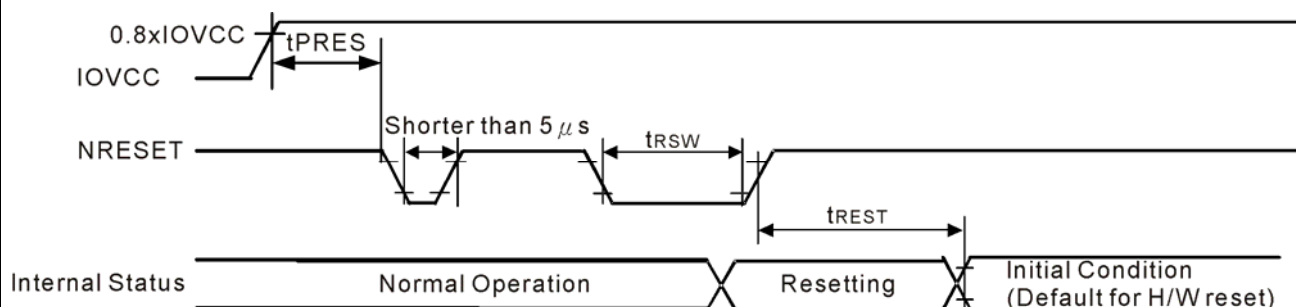
Input Signal Slope



Output Signal Slope



4.2.5 RESET INPUT TIMING



SYMBOL	PARAMETER	RELATED PINS	MIN.	TYP.	MAX.	NOTE	UNIT
t_{RESW}	RESET LOW PULSE WIDTH ⁽¹⁾	NRESET	10	—	—		μs
t_{REST}	RESET COMPLETE TIME ⁽²⁾	—	—	—	5	WHEN RESET APPLIED DURING STB MODE	ms
		—	—	—	120	WHEN RESET APPLIED DURING STB MODE	ms
t_{PRES}	RESET GOES HIGH LEVEL AFTER POWER ON TIME	NRESET & IOVCC	1	—	—	RESET GOES HIGH LEVEL AFTER POWER ON	ms

NOTE : (1) SPIKE DUE TO AN ELECTROSTATIC DISCHARGE ON NRESET LINE DOES NOT CAUSE IRREGULAR SYSTEM RESET ACCORDING TO THE TABLE BELOW.

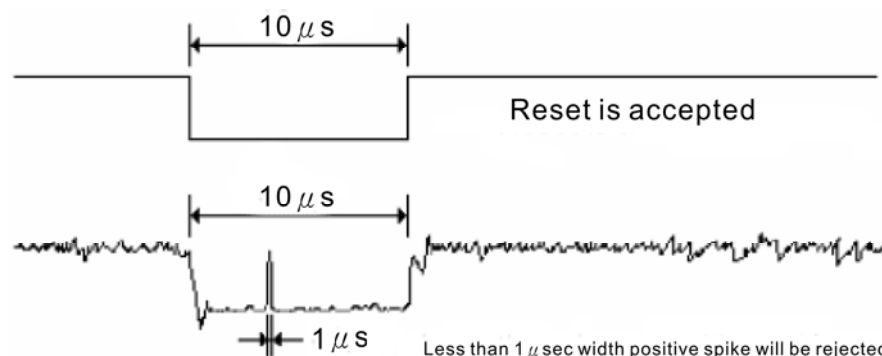
NRESET PULSE	ACTION
SHORTER THAN $5\mu s$	RESET REJECTED
LONGER THAN $10\mu s$	RESET
BETWEEN $5\mu s$ AND $10\mu s$	RESET START

NOTE : (2) DURING THE RESETTING PERIOD, THE DISPLAY WILL BE BLANKED (THE DISPLAY IS ENTERING BLANKING SEQUENCE, WHICH MAXIMUM TIME IS 120 MS, WHEN RESET STARTS

IN STB OUT -MODE. THE DISPLAY REMAINS THE BLANK STATE IN STB -MODE) AND THEN RETURN TO DEFAULT CONDITION FOR H/W RESET.

(3) DURING RESET COMPLETE TIME, ID2 AND VCOMOF VALUE IN OTP WILL BE LATCHED TO INTERNAL REGISTER DURING THIS PERIOD. THIS LOADING IS DONE EVERY TIME WHEN THERE IS H/W RESET COMPLETE TIME (TREST) WITHIN 5MS AFTER A RISING EDGE OF NRESET.

(4) SPIKE REJECTION ALSO APPLIES DURING A VALID RESET PULSE AS SHOWN BELOW :



(5) IT IS NECESSARY TO WAIT 5MSEC AFTER RELEASING! RES BEFORE SENDING COMMANDS. ALSO STB OUT COMMAND CANNOT BE SENT FOR 120MSEC.

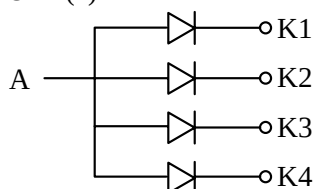
5 . OPTICAL CHARACTERISTICS NOTE (2)

5 . 1 OPTICAL CHARACTERISTICS

Ta = 25 °C

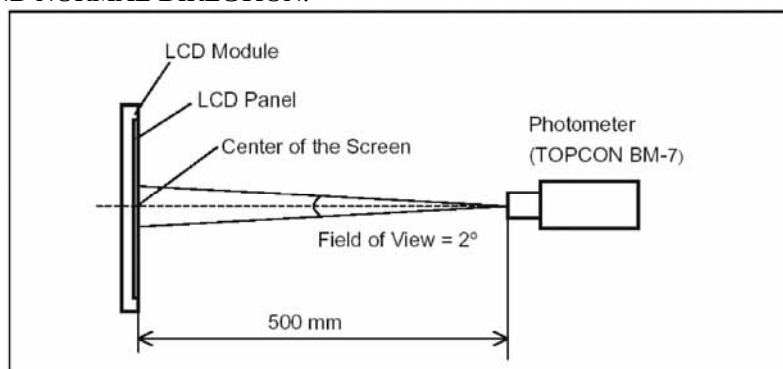
I T E M		SYMBOL	CONDITION		MIN.	TYP.	MAX.	UNIT	REMARK
VIEWING ANGLE	HOR.	θ_{x+}	CENTER CR≥10	$\theta_{y=0^{\circ}}$	70	75	—	deg .	(3)
		θ_{x-}			65	70	—		
	VER.	θ_{y+}		$\theta_{x=0^{\circ}}$	70	75	—		
		θ_{y-}			50	55	—		
CONTRAST RATIO		CR	NTSC : 60% VIEWING NORMAL AUNLE $\theta_x = 0^{\circ}$ $\theta_y = 0^{\circ}$		400	500	—		(4)
RESPONSE TIME		t r (rise)			—	10	20	ms	(5)
		t f (fall)			—	15	30		
THE BRIGHTNESS OF MODULE		B					300	350	—
COLOR OF CIE COORDINATE	WHITE	W _x			0.260	0.310	0.360	—	(7)
		W _y			0.291	0.341	0.391		
	RED	R _x			0.605	0.655	0.705	—	
		R _y			0.279	0.329	0.379		
	GREEN	G _x			0.262	0.312	0.362	—	
		G _y			0.525	0.575	0.625		
	BLUE	B _x			0.084	0.134	0.184	—	
		B _y			0.085	0.135	0.185		
THE BRIGHTNESS OF UNIFORMITY		—	—		75	80	—	%	—
CURRENT FOR LED BACKLIGHT		V _F	I _F = 80mA		—	3.3	—	V	NOTE (1)

NOTE (1) :

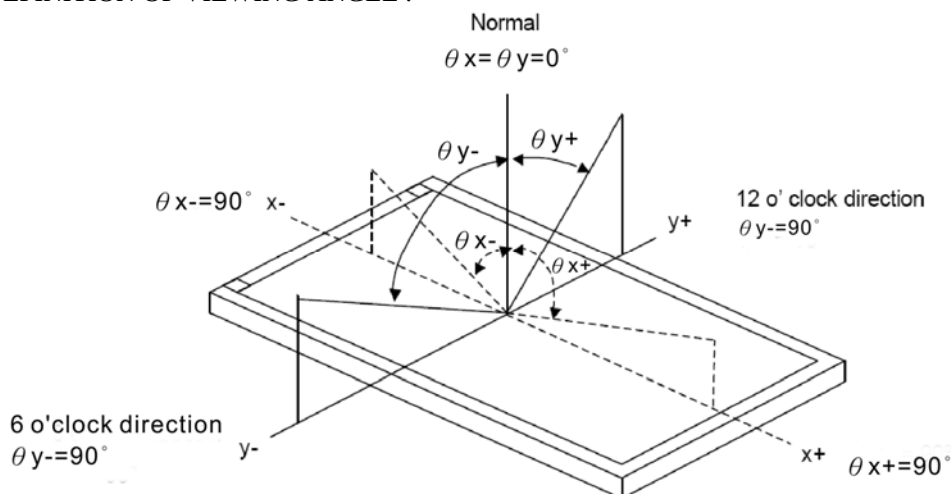


NOTE (2) : TEST EQUIPMENT SETUP :

AFTER STABILIZING AND LEAVING THE PANEL ALONE AT A GIVEN TEMPERATURE FOR 30 MINUTES , THE MEASUREMENT SHOULD BE EXECUTED. MEASUREMENT SHOULD BE EXECUTED IN A STABLE , WINDLESS , AND DARK ROOM. OPTICAL SPECIFICATIONS ARE MEASURED BY TOPCON BM-7 (FAST) WITH A VIEWING ANGLE OF 2° AT A DISTANCE OF 50cm AND NORMAL DIRECTION.



NOTE (3) : DEFINITION OF VIEWING ANGLE :

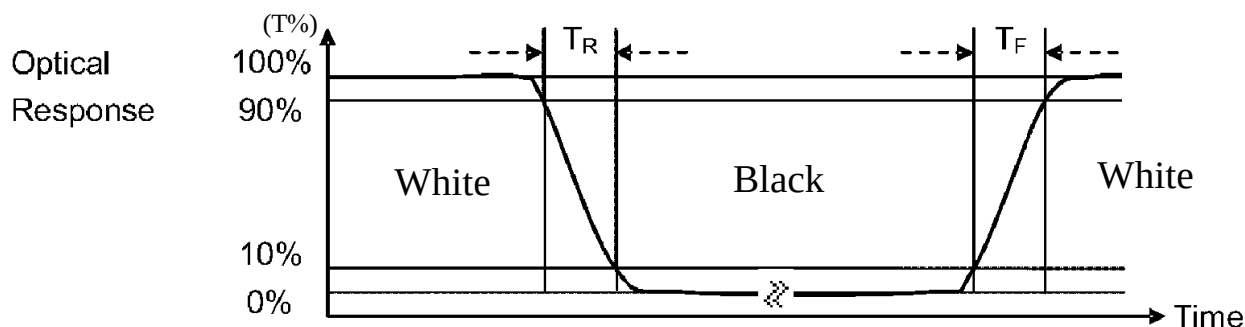


NOTE (4) : DEFINITION OF CONTRAST RATIO :

$$\text{CONTRAST RATIO (CR)} = \frac{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "WHITE STATE"}}{\text{BRIGHTNESS MEASURED WHEN LCD IS AT "BLACK STATE"}}$$

NOTE (5) : DEFINITION OF RESPONSE TIME : TR AND TF

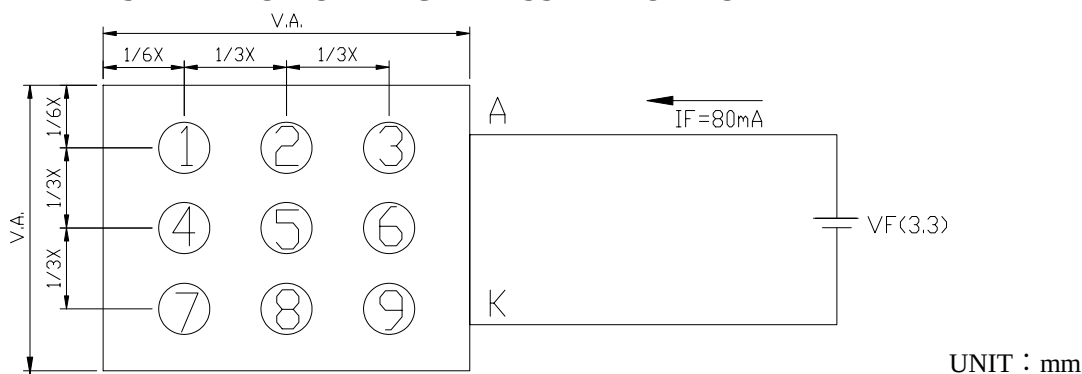
THE FIGURE BELOW IS THE OUTPUT SIGNAL OF THE PHOTO DETECTOR.



NOTE (6) : BRIGHTNESS MEASURED WHEN LCD IS AT "WHITE STATE"

NOTE (7) : THE 100% TRANSMISSION IS DEFINED AS THE TRANSMISSION OF LCD PANEL WHEN ALL THE INPUT TERMINALS OF MODULE ARE ELECTRICALLY OPENED.

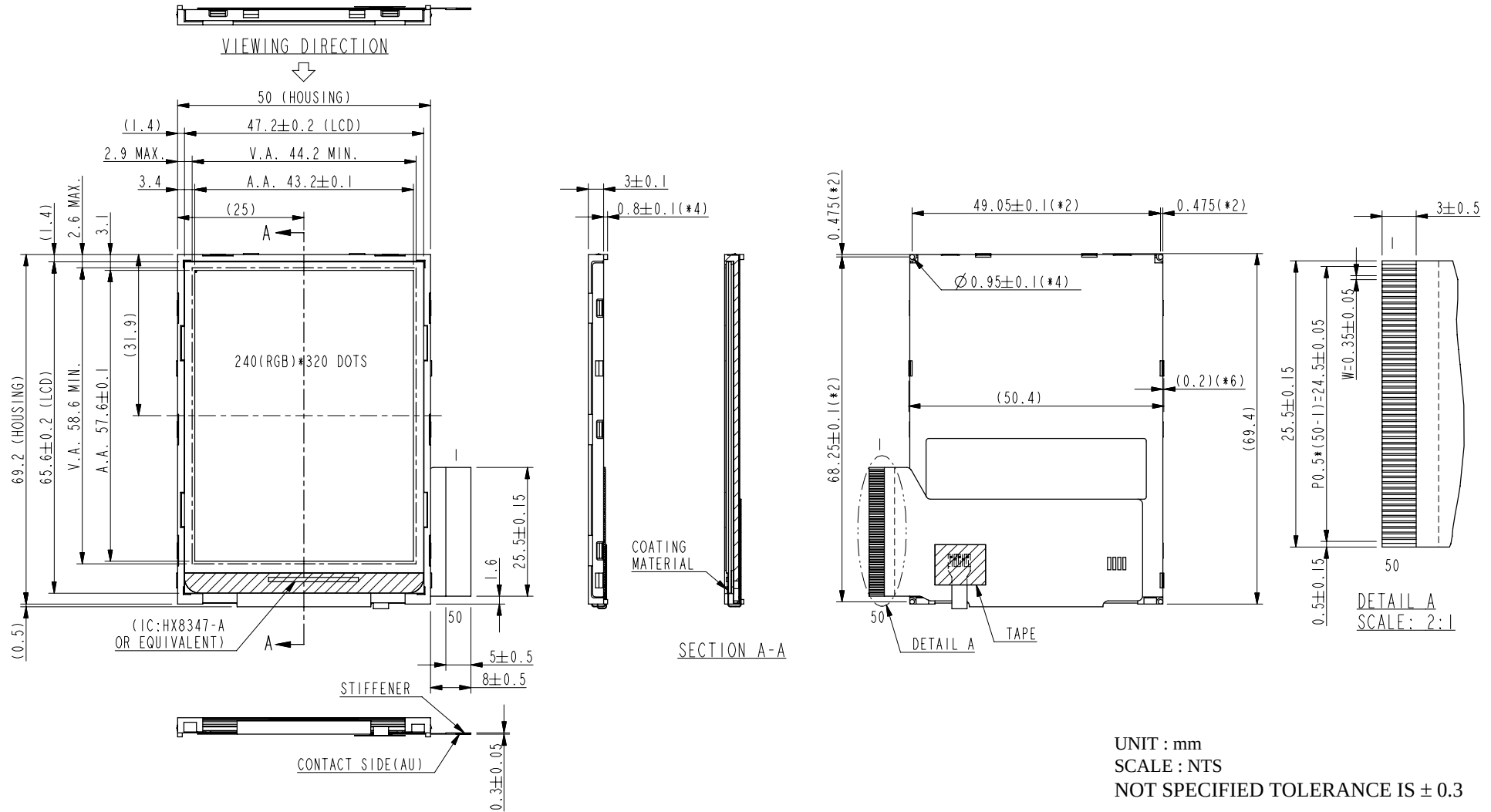
5.2 THE TEST METHOD OF BRIGHTNESS AND UNIFORMITY



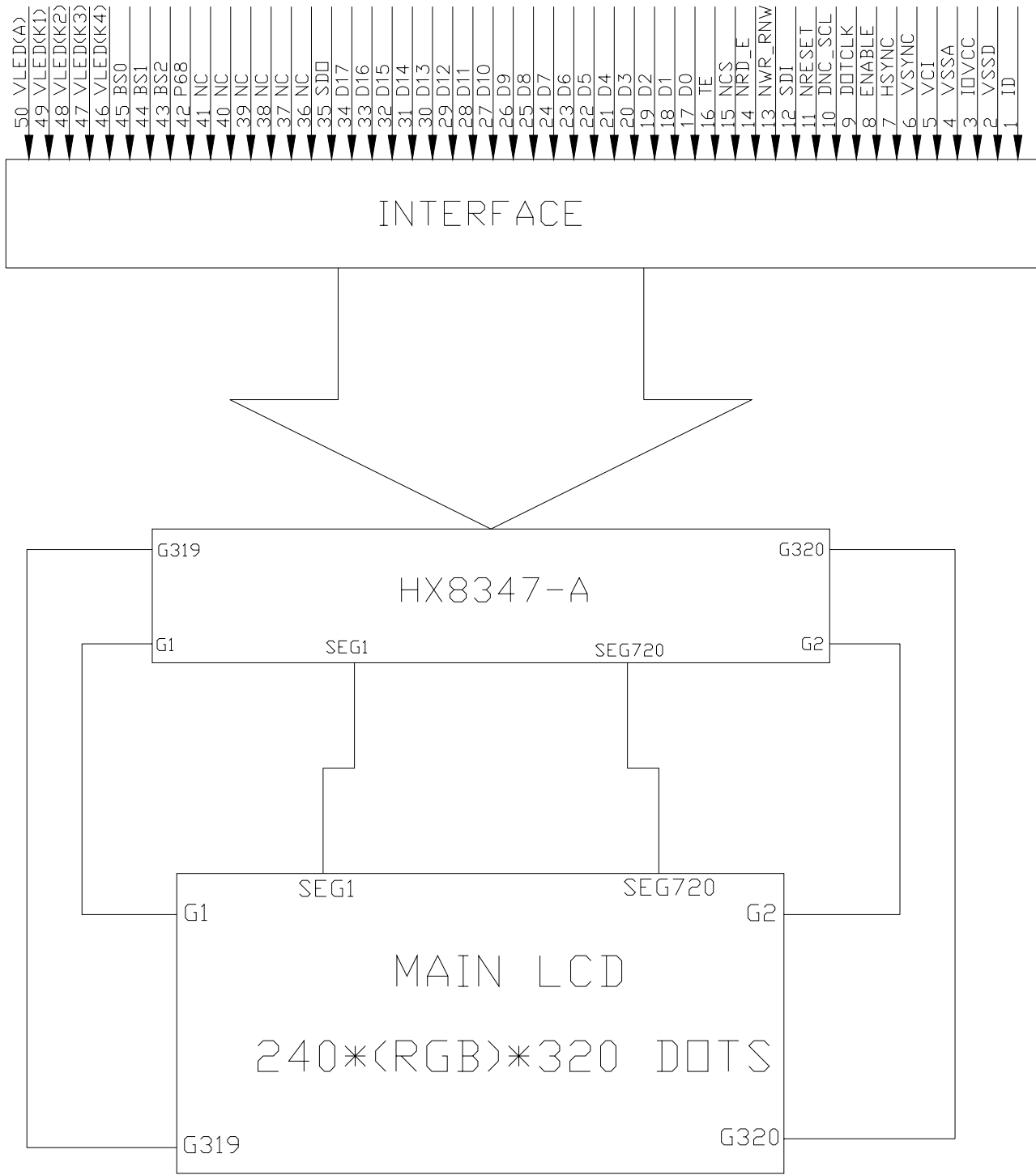
5.3 THE CALCULATING METHOD OF UNIFORMITY

$$\text{UNIFORMITY} = \left[1 - \frac{\text{MAXIMUM BRIGHTNESS} - \text{MINIMUM BRIGHTNESS}}{\text{AVERAGE BRIGHTNESS}} \right] \times 100\%$$

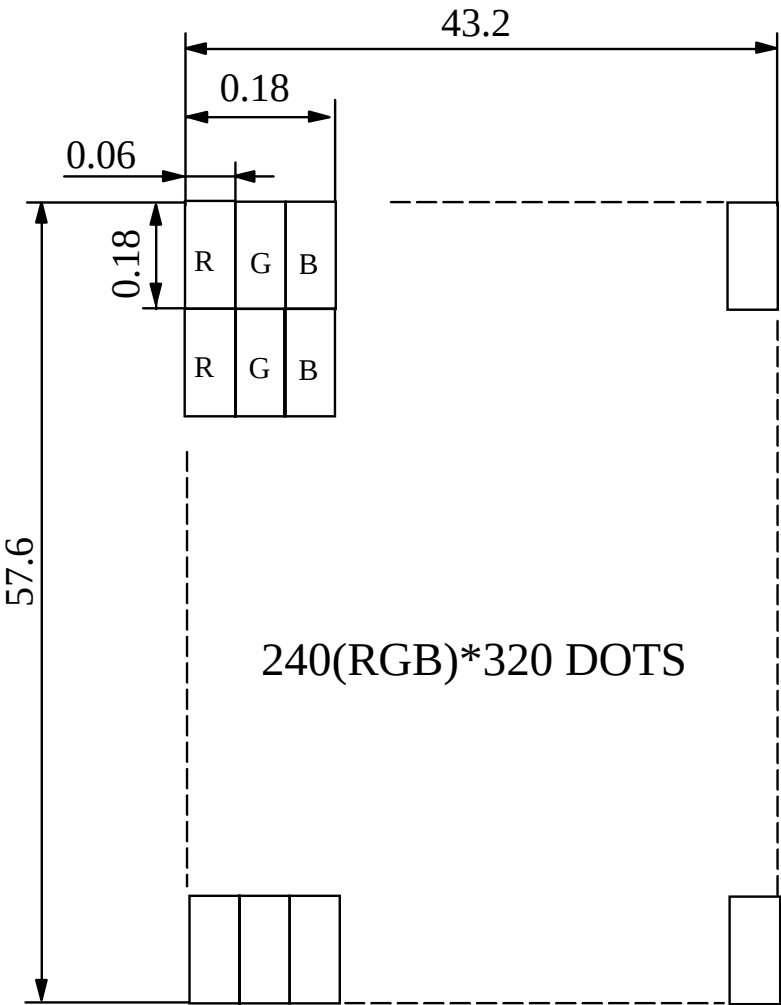
6. OUTLINE DIMENSIONS



7. BLOCK DIMENSION



8. DETAIL DRAWING OF DOT MATRIX



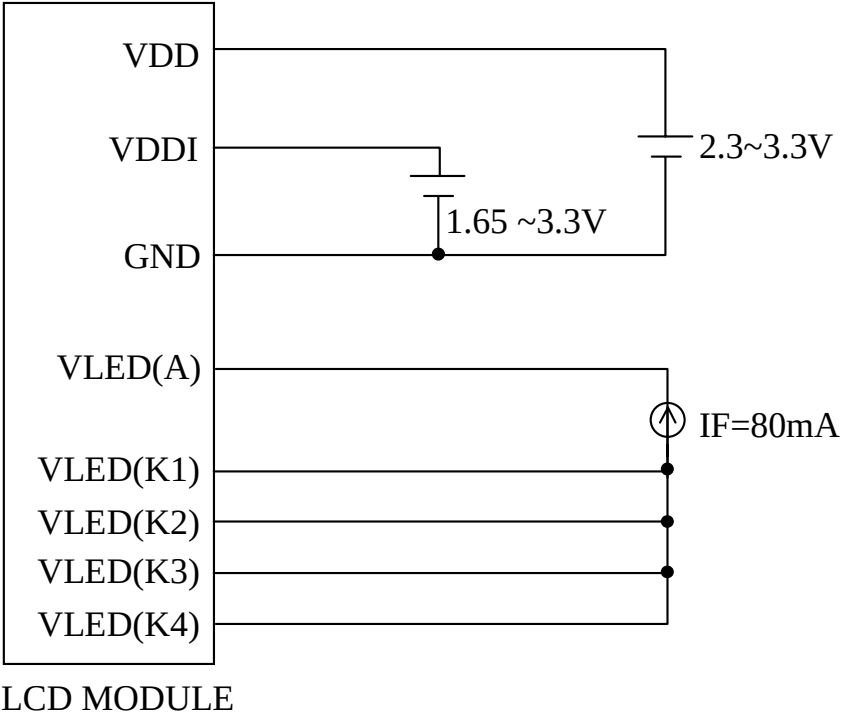
UNIT : mm
SCALE : NTS
NOT SPECIFIED TOLERANCE IS ± 0.1
DOTS MATRIX TOLERANCE IS ± 0.01

9. INTERFACE SIGNALS
9.1 LCD MODULE CONNECTOR

PIN NO	SYMBOL	REMARK	FUNCTION
1	ID	O	MAKER'S IDENTIFICATION (MAY ESTABLISH "H", "L" OR "NC") IF THE CUSTOMER HAS MORE THAN TWO MAKERS WHO APPLIED DIFFERENT S/W, CAN USE THIS PIN TO DETECT THE CODE BY THE MPU AND DECIDE THE MAKER'S ID. MOST IMPORTANTLY, THE CUSTOMER MUST DESIGN THIS PIN ON THE MAIN BOARD AS WELL AND LEAVE IT OPEN AS NOT USED. NOTE : EDT MODULE'S SETTING IS "H".
2	VSSD	I	DIGITAL GROUND
3	IOVCC	I	DIGITAL IO PAD POWER SUPPLY
4	VSSA	I	ANALOG GROUND
5	VCI	I	ANALOG POWER SUPPLY
6	VSYN	I	FRAME SYNCHRONIZING SIGNAL. HAS TO BE FIXED TO IOVCC LEVEL IF IS NOT USED.
7	HSYN	I	FRAME SYNCHRONIZING SIGNAL. HAS TO BE FIXED TO IOVCC LEVEL IF IS NOT USED.
8	ENABLE	I	A DATA ENABLE SIGNAL IN RGB I/F MODE. HAS TO BE FIXED TO VSSD LEVEL IF UNUSED (HIGH ACTIVE, IF EPL=0).
9	DOTCLK	I	DOT CLOCK SIGNAL. HAS TO BE FIXED TO VSSD LEVEL IF IS NOT USED.
10	DNC_SCL	I	THE SIGNAL FOR COMMAND OR PARAMETER SELECT UNDER PARALLEL MODE (I.E. NOT SERIAL INTERFACE): LOW : COMMAND. HIGH : PARAMETER. WHEN UNDER SERIAL INTERFACE, IT SERVERS AS SCL.
11	NRESET	I	RESET PIN. SETTING EITHER PIN LOW INITIALIZES THE LSI. MUST BE RESET AFTER POWER IS SUPPLIED.
12	SDI	I	SERIAL DATA PIN. WHEN IFSEL0=0, IT IS SERIAL DATA INPUT/OUTPUT PIN (SDA). WHEN IFSEL0=1, IT IS SERIAL DATA INPUT PIN. IF NOT USED, PLEASE LET IT CONNECTED TO IOVCC OR VSSD.
13	NWR_RNW	I	I80 SYSTEM: SERVES AS A WRITE SIGNAL AND WRITES DATA AT THE RISING EDGE. M68 SYSTEM: 0: WRITE, 1: READ. FIX IT TO IOVCC OR VSSD LEVEL WHEN USING SERIAL BUSS INTERFACE.
14	NRD_E	I	I80 SYSTEM: SERVES AS A READ SIGNAL AND READ DATA AT THE LOW LEVEL. M68 SYSTEM: 0: READ/WRITE DISABLE, 1: READ/WRITE ENABLE. FIX IT TO IOVCC OR VSSD LEVEL WHEN USING SERIAL BUSS INTERFACE.
15	NCS	I	CHIP SELECT SIGNAL. LOW : CHIP CAN BE ACCESSED; HIGH : CHIP CANNOT BE ACCESSED. MUST BE CONNECTED TO VSSD IF NOT IN USE.
16	TE	O	TEARING EFFECT OUTPUT, IF NOT USED, PLEASE OPEN THIS PIN.

PIN NO	SYMBOL	REMARK	FUNCTION																								
17	D0	I/O	1. 18-BIT BI-DIRECTIONAL DATA BUS FOR SYSTEM INTERFACE. 8-BIT BUS: USE D7-D0 AND D17-D8 UNUSED. 16-BIT BUS: USE D15-D0 AND D17-D16 UNUSED. 18-BIT BUS: USE D17-D0 2. 18-BIT DATA BUS FOR RGB INTERFACE 16-BIT BUS: USE D15-D0 AND D17-D16 UNUSED. 18-BIT BUS: USE D17-D0 CONNECTED UNUSED PINS TO THE VSSD LEVEL. NOTICE: WHEN REGISTER RGB_EN=1 AND PIN ENABLE=1, D[17:0] IS USED AS STREAM IMAGE DATA FOR DISPLAY. IT MEANS MPU DATA BUS AND RGB DATA BUS IS SHARED.																								
18	D1	I/O																									
19	D2	I/O																									
20	D3	I/O																									
21	D4	I/O																									
22	D5	I/O																									
23	D6	I/O																									
24	D7	I/O																									
25	D8	I/O																									
26	D9	I/O																									
27	D10	I/O																									
28	D11	I/O																									
29	D12	I/O																									
30	D13	I/O																									
31	D14	I/O																									
32	D15	I/O																									
33	D16	I/O																									
34	D17	I/O																									
35	SDO	O	SERIAL DATA OUTPUT. IF NOT USE, LET IT TO OPEN.																								
36	NC	NC	NO USE, LET IT OPEN																								
37	NC	NC	NO USE, LET IT OPEN																								
38	NC	NC	NO USE, LET IT OPEN																								
39	NC	NC	NO USE, LET IT OPEN																								
40	NC	NC	NO USE, LET IT OPEN																								
41	NC	NC	NO USE, LET IT OPEN																								
42	P68	I	<table><tr><td>P68</td><td>BS2</td><td>BS1</td><td>BS0</td><td>16-BIT BUS INTERFACE, 80-SYSTEM, 65K-COLOR</td><td>D17-D16 : UNUSED, D15-D0 : DATA</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>16-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR</td><td>D17-D16: UNUSED, D15-D0: DATA</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>18-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR</td><td>D17-D0: DATA</td></tr></table>	P68	BS2	BS1	BS0	16-BIT BUS INTERFACE, 80-SYSTEM, 65K-COLOR	D17-D16 : UNUSED, D15-D0 : DATA	0	0	0	0	16-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR	D17-D16: UNUSED, D15-D0: DATA	0	0	1	0	18-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR	D17-D0: DATA						
			P68	BS2	BS1	BS0	16-BIT BUS INTERFACE, 80-SYSTEM, 65K-COLOR	D17-D16 : UNUSED, D15-D0 : DATA																			
			0	0	0	0	16-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR	D17-D16: UNUSED, D15-D0: DATA																			
			0	0	1	0	18-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR	D17-D0: DATA																			
43	BS2	I	<table><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>8-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR</td><td>D17-D8: UNUSED D7-D0: DATA</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>16-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR</td><td>D17-D8: UNUSED D7-D0: DATA</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>18-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR</td><td>D17-D0: DATA</td></tr></table>	0	0	1	1	8-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR	D17-D8: UNUSED D7-D0: DATA	0	1	0	0	16-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR	D17-D8: UNUSED D7-D0: DATA	0	1	0	1	18-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR	D17-D0: DATA						
			0	0	1	1	8-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR	D17-D8: UNUSED D7-D0: DATA																			
			0	1	0	0	16-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR	D17-D8: UNUSED D7-D0: DATA																			
0	1	0	1	18-BIT BUS INTERFACE, 80-SYSTEM, 262K-COLOR	D17-D0: DATA																						
44	BS1	I	<table><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>16-BIT BUS INTERFACE, 68-SYSTEM, 65K-COLOR</td><td>D17-D16: UNUSED, D15-D0: DATA</td></tr><tr><td>1</td><td>0</td><td>0</td><td>1</td><td>16-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR</td><td>D17-D16: UNUSED, D15-D0: DATA</td></tr><tr><td>1</td><td>0</td><td>1</td><td>0</td><td>18-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR</td><td>D17-D0: DATA</td></tr></table>	1	0	0	0	16-BIT BUS INTERFACE, 68-SYSTEM, 65K-COLOR	D17-D16: UNUSED, D15-D0: DATA	1	0	0	1	16-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR	D17-D16: UNUSED, D15-D0: DATA	1	0	1	0	18-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR	D17-D0: DATA						
			1	0	0	0	16-BIT BUS INTERFACE, 68-SYSTEM, 65K-COLOR	D17-D16: UNUSED, D15-D0: DATA																			
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1	0	1	0	18-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR	D17-D0: DATA																						
45	BS0	I	<table><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>8-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR</td><td>D17-D8:UNUSED D7-D0: DATA</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>16-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR</td><td>D17-D8: UNUSED D7-D0: DATA</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>18-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR</td><td>D17-D0: DATA</td></tr><tr><td>×</td><td>1</td><td>1</td><td>0</td><td>SERIAL BUS IF</td><td>DNC_SCL, SDO,SDI</td></tr></table>	1	0	1	1	8-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR	D17-D8:UNUSED D7-D0: DATA	1	1	0	0	16-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR	D17-D8: UNUSED D7-D0: DATA	1	1	0	1	18-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR	D17-D0: DATA	×	1	1	0	SERIAL BUS IF	DNC_SCL, SDO,SDI
			1	0	1	1	8-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR	D17-D8:UNUSED D7-D0: DATA																			
			1	1	0	0	16-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR	D17-D8: UNUSED D7-D0: DATA																			
			1	1	0	1	18-BIT BUS INTERFACE, 68-SYSTEM, 262K-COLOR	D17-D0: DATA																			
×	1	1	0	SERIAL BUS IF	DNC_SCL, SDO,SDI																						
46	VLED(K4)	I	POWER SUPPLY FOR LED(-)																								
47	VLED(K3)	I	POWER SUPPLY FOR LED(-)																								
48	VLED(K2)	I	POWER SUPPLY FOR LED(-)																								
49	VLED(K1)	I	POWER SUPPLY FOR LED(-)																								
50	VLED(A)	I	POWER SUPPLY FOR LED(+)																								

10. POWER SUPPLY
10.1 POWER SUPPLY FOR LCM



11. SPECIFICATION OF AUDACITY ASSURANCE

11.1 APPLICATION

This inspection standard is to be applied to the LCD module delivered from EMERGING DISPLAY TECHNOLOGIES CORP.(E.D.T) to customers

11.2 INSPECTION CONDITIONS

11.2.1 Environmental conditions

Room temperature : $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$

Humidity : $50 \pm 10\% \text{ RH}$

11.2.2 DISPLAY-ON inspection, visual appearance inspection on screen

The distance between the module and the inspector's eyes shall be at least 30cm under illumination of one fluorescent lamp of 20W.

11.2.3 Inspection lot

Quantity per delivery lot for each model

11.2.4 Inspection method

A sampling inspection shall be made according to the following provisions to judge the acceptability

(a)Applicable standard : MIL-STD-105E

Normal inspection, single sampling

Level II

(b)AQL : Major defect : AQL 0.65

Minor defect : AQL 2.5

TOTAL DEFECTS : AQL 2.5

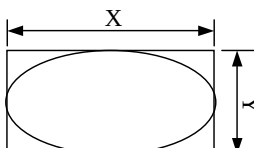
11.3 INSPECTION STANDARDS

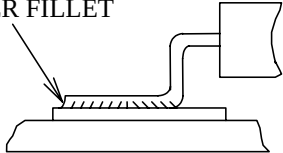
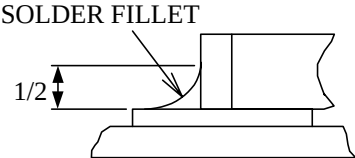
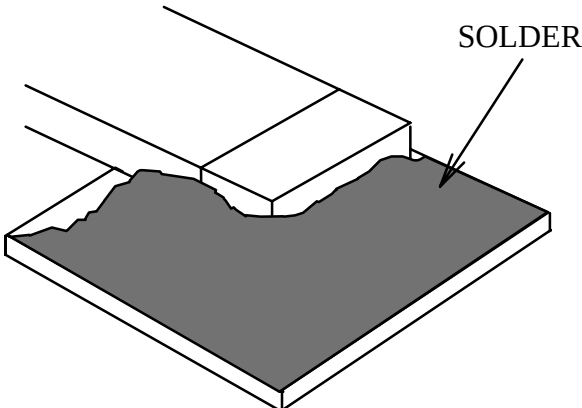
11.3.1 VISUAL DEFECTS CLASSIFICATION

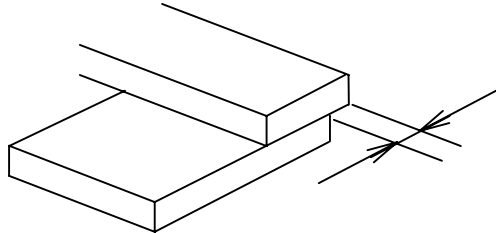
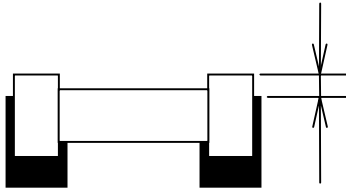
TYPE OF DEFECT	INSPECTION ITEM	DEFECT FEATURE	AQL
MAJOR DEFECT	1.DISPLAY ON	• DEFECT TO MISS SPECIFIED DISPLAY FUNCTION, FOR ALL AND SPECIFIED DOTS - EX : DISCONNECTION , SHORT CIRCUIT ETC	0.65
	2.BACKLIGHT	• NO LIGHT • FLICKERING AND OTHER ABNORMAL ILLUMINATION	
	3.DIMENSIONS	• SUBJECT TO INDIVIDUAL ACCEPTANCE SPECIFICATIONS	
MINOR DEFECT	1.DISPLAY ZONE	• BLACK/WHITE SPOT • BUBBLES ON POLARIZER • BLACK/WHITE LINE • SCRATCH • CONTAMINATION • LEVER COLOR SPREED	2.5
	2.BEZEL ZONE	• STAINS • SCRATCHES • FOREIGN MATTER	
	3.PCB	• CRACKS • SCRATCHES • STAINS	
	4.SOLDERING	• INSUFFICIENT SOLDER • SOLDERED IN INCORRECT POSITION • CONVEX SOLDERING SPOT • SOLDER BALLS • SOLDER SCRAPS	
	5.DISPLAY ON (ALL ON)	• LIGHT LINE	

11.3.2 INSPECTION CRITERION

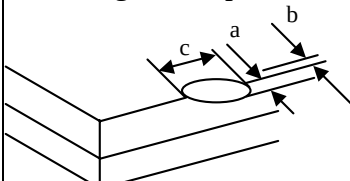
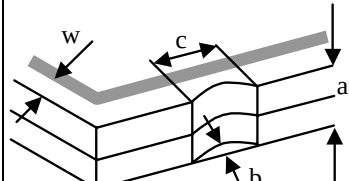
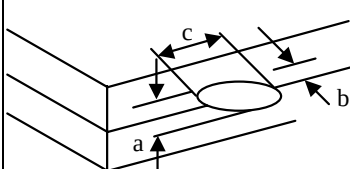
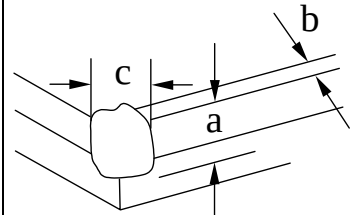
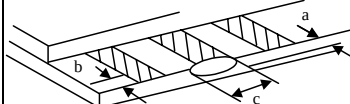
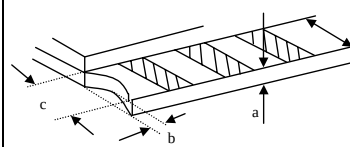
NO.	ITEM	CRITERIA													
1.	DISPLAY ON INSPECTION	(1)INCORRECT PATTERN (2)MISSING SEGMENT (3)DIM SEGMENT (4)OPERATING VOLTAGE BEYOND SPEC													
2.	OVERALL DIMENSIONS	(1)OVERALL DIMENSION BEYOND SPEC													
3.	BLACK SPOT I WHITE SPOT I ON-DISPLAY	(1)INSPECTION PATTERN : FULL WHITE,FULL BLACK, RED, GREEN AND BLUE SCREENS. (2) <table> <tr> <td rowspan="6">DOT DEFECT</td><td>BRIGHT DOT</td><td>$N \leq 3$</td></tr> <tr> <td>DARK DOT</td><td>$N \leq 3$</td></tr> <tr> <td>TOTAL DOT</td><td>$N \leq 3$</td></tr> <tr> <td>MINIMUM DISTANCE BETWEEN BRIGHT DOTS</td><td>$L \geq 5\text{mm}$</td></tr> <tr> <td>MINIMUM DISTANCE BETWEEN BRIGHT DOTS AND DARK DOTS</td><td>$L \geq 5\text{mm}$</td></tr> <tr> <td>MINIMUM DISTANCE BETWEEN DARK DOTS</td><td>$L \geq 5\text{mm}$</td></tr> </table> NOTE : THE DEFINITION OF DOT DEFECT:THE DOT DEFECT WAS JUDGED AFTER REPAIR AND THE SIZE OF A DEFECTIVE DOT OVER 1/2 OF WHOLE DOT IS REGARDED AS ONE DEFECTIVE DOT.	DOT DEFECT	BRIGHT DOT	$N \leq 3$	DARK DOT	$N \leq 3$	TOTAL DOT	$N \leq 3$	MINIMUM DISTANCE BETWEEN BRIGHT DOTS	$L \geq 5\text{mm}$	MINIMUM DISTANCE BETWEEN BRIGHT DOTS AND DARK DOTS	$L \geq 5\text{mm}$	MINIMUM DISTANCE BETWEEN DARK DOTS	$L \geq 5\text{mm}$
DOT DEFECT	BRIGHT DOT	$N \leq 3$													
	DARK DOT	$N \leq 3$													
	TOTAL DOT	$N \leq 3$													
	MINIMUM DISTANCE BETWEEN BRIGHT DOTS	$L \geq 5\text{mm}$													
	MINIMUM DISTANCE BETWEEN BRIGHT DOTS AND DARK DOTS	$L \geq 5\text{mm}$													
	MINIMUM DISTANCE BETWEEN DARK DOTS	$L \geq 5\text{mm}$													
4.	BLACK LINE WHITE LINE ON-DISPLAY	(1)THE FOLLOWING BLACK LINE, WHITE LINE ARE WITHIN THE VIEWING AREA. WIDTH : Wmm , LENGH : Lmm <table> <tr> <th>LENGTH : L</th><th>WIDTH : W</th><th>PERMISSIBLE NO.</th></tr> <tr> <td>$L \leq 0.5$</td><td>$W \leq 0.1$</td><td>IGNORE</td></tr> <tr> <td>$0.5 < L \leq 3$</td><td>$0.1 < W \leq 0.5$</td><td>2</td></tr> <tr> <td>$3 < L$</td><td>$0.5 \leq W$</td><td>NONE</td></tr> </table>	LENGTH : L	WIDTH : W	PERMISSIBLE NO.	$L \leq 0.5$	$W \leq 0.1$	IGNORE	$0.5 < L \leq 3$	$0.1 < W \leq 0.5$	2	$3 < L$	$0.5 \leq W$	NONE	
LENGTH : L	WIDTH : W	PERMISSIBLE NO.													
$L \leq 0.5$	$W \leq 0.1$	IGNORE													
$0.5 < L \leq 3$	$0.1 < W \leq 0.5$	2													
$3 < L$	$0.5 \leq W$	NONE													

NO.	ITEM	CRITERIA			
5.	BUBBLES OF POLARIZER /SURFACE STAINS /DIRT/CF FAIL /SPOT	BUBBLE ON THE POLARIZER	LINE SHAPE L:LENGTH(mm)	$L \leq 0.5, W \leq 0.1$	LGNORE
				$0.5 < L \leq 3$ $0.1 < W \leq 0.5$	$N \leq 1$
			DOT SHAPE D:AVERAGE DIAMETER(mm)	$D \leq 0.25$	LGNORE
				$0.25 < D \leq 0.5$	$N \leq 0.5$
				$0.5 < D$	NOTE
		SURFACE STATNS		$D < 0.1 \text{ mm}$	IGNORE
				$0.1 < D \leq 0.3\text{mm}$	$N \leq 2$
		CF FAIL / SPOT		$D < 0.1 \text{ mm}$	IGNORE
				$0.1 < D \leq 0.3\text{mm}$	$N \leq 2$
		NOTE : (1)POLARIZER BUBBLE IS DEFINED AS THE BUBBLE APPEARS ON ACTIVE DISPLAY AREA. THE DEFECT OF POLARIZER BUBBLE SHALL BE IGNORED IF THE POLARIZER BUBBLE APPEARS ON THE OUTSIDE OF ACTIVE DISPLAY AREA. (2)THE EXTRANEIOUS SUBSTANCE IS DEFINED AS IT CAN BE OBSERVED WHEN THE MODULE IS POWER ON. (3)THE DEFINITION OF AVERAGE DIAMETER, D IS DEFINED AS FOLLOWING. AVERAGE DIAMETER(D)=(X+Y)/2 , WHERE			
					
6.	SCRATCHES AND DENT ON GLASS POLARIZER	(1) PLS REFER TO THE ABOVE NO.3 AND 4 TO DETERMINE SCRATCHES AND DENT ON POLARIZER OR GLASS			
7.	UNEVEN COLOR SPREAD, COLORATION	(1)TO BE DETERMINED BASED UPON THE STANDARD SAMPLE.			
8.	BEZEL APPEARANCE	(1)BEZEL MAY NOT HAVE RUST, BE DEFORMED OR HAVE FINGER PRINTS STAINS OF OTHER CONTAMINATION. (2)BEZEL MUST COMPLY WITH JOB SPECIFICATIONS.			

NO.	ITEM	CRITERIA
9.	SOLDERING	(1)NO SOLDERING FOUND ON THE SPECIFIED PLACE (2)INSUFFICIENT SOLDER (a)LSI, IC A POOR WETTING OF SOLDER IS BETWEEN LOWER BEND OR “HEEL” OF LEAD AND PAD SOLDER FILLET  (b)CHIP COMPONENT SOLDER IS LESS THAN 50% OF SIDES AND FRONT FACE WETTING SOLDER FILLET  1/2 SOLDER WETS 3 SIDES OF TERMINAL, BUT LESS THAN 25% OF SIDES AND FRONT SURFACE AREA ARE COVERED  SOLDER

NO.	ITEM	CRITERIA
9.	SOLDERING	(3)PARTS ALIGMENT (a)LSI, IC LEAD WIDTH IS MORE THAN 50% BEYOND PAD OUTLINE  (b)CHIP COMPONENT COMPONENT IS OFF CENTER, AND MORE THAN 50% OF THE LEADS IS OFF THE PAD OUTLINE  (4)NO UNMELTED SOLDER PASTE MAY BE PRESENT ON THE PCB. (5)NO COLD SOLDER JOINTS, MISSING SOLDER CONNECTIONS, OXIDATION OR ICICLE. (6)NO RESIDUE OR SOLDER BALLS ON PCB. (7)NO SHORT CIRCUITS IN COMPONENTS ON PCB.
10.	BACKLIGHT	(1)NO LIGHT (2)FLICKERING AND OTHER ABNORMAL ILLUMINATION (3)SPOTS OR SCRATCHES THAT APPEAR WHEN LIT MUST BE JUDGED USING LCD SPOT, LINES AND CONTAMINATION STANDARDS. (4)BACKLIGHT DOESN'T LIGHT OR COLOR IS WRONG.

NO.	ITEM	CRITERIA
11.	PCB , COB	(1)COB SEAL MAY NOT HAVE PINHOLES LARGER THAN 0.2mm OR CONTAMINATION. (2)COB SEAL SURFACE MAY NOT HAVE PINHOLES THROUGH TO THE IC. (3)THE HEIGHT OF THE COB SHOULD NOT EXCEED THE HEIGHT INDICATED IN THE ASSEMBLY DIAGRAM. (4)THERE MAY NOT BE MORE THAN 2mm OF SEALANT OUTSIDE THE SEAL AREA ON THE PCB, AND THERE SHOULD BE NO MORE THAN THREE PLACES. (5)NO OXIDATION OR CONTAMINATION PCB TERMINALS (6)PARTS ON PCB MUST BE THE SAME AS ON THE PRODUCTION CHARACTERISTIC CHART. THERE SHOULD BE NO WRONG PARTS, MISSING PARTS OR EXCESS PARTS. (7)THE JUMPER ON THE PCB SHOULD CONFORM TO THE PRODUCT CHARACTERISTIC CHART. (8)IF SOLDER GETS ON BEZEL TAB PADS, LED PAD, ZEBRA PAD OR SCREW HOLD PAD, MAKE SURE IT IS SMOOTHED DOWN.
12.	GENERAL APPEARANCE	(1)NO OXIDATION, CONTAMINATION, CURVES OR, BENDS ON INTERFACE PIN (OLB) OF TCP. (2)NO CRACKS ON INTERFACE PIN (OLB) OF TCP. (3)NO CONTAMINATION, SOLDER RESIDUE OR SOLDER BALLS ON PRODUCT. (4)THE IC ON THE TCP MAY NOT BE DAMAGED, CIRCUITS. (5)THE UPPERMOST EDGE OF THE PROTECTIVE STRIP ON THE INTERFACE PIN MUST BE PRESENT OR LOOK AS IF IT CAUSE THE INTERFACE PIN TO SEVER. (6)THE RESIDUAL ROSIN OR TIN OIL OF SOLDERING (COMPONENT OR CHIP COMPONENT) IS NOT BURNED INTO BROWN OR BLACK COLOR. (7)SEALANT ON TOP OF THE ITO CIRCUIT HAS NOT HARDENED. (8)PIN TYPE MUST MATCH TYPE IN SPECIFICATION SHEET. (9)LCD PIN LOOSE OR MISSING PINS. (10)PRODUCT PACKAGING MUST THE SAME AS SPECIFIED ON PACKAGING SPECIFICATION SHEET. (11)PRODUCT DIMENSION AND STRUCTURE MUST CONFORM TO PRODUCT SPECIFICATION SHEET. (12)THE APPEARANCE OF HEAT SEAL SHOULD NOT ADMIT ANY DIRT AND BREAK.

NO.	ITEM	CRITERIA											
13.	CRACKED GLASS	THE LCD WITH EXTENSIVE CRACK IS NOT ACCEPTABLE											
		General glass chip :											
			<table><tr><td>a</td><td>b</td><td>c</td></tr><tr><td>$\leq t/2$</td><td>< VIEWING AREA</td><td>$\leq 1/8X$</td></tr><tr><td>$t/2 >, \leq 2t$</td><td>$\leq W/3$</td><td>$\leq 1/8X$</td></tr></table>	a	b	c	$\leq t/2$	< VIEWING AREA	$\leq 1/8X$	$t/2 >, \leq 2t$	$\leq W/3$	$\leq 1/8X$	
		a	b	c									
		$\leq t/2$	< VIEWING AREA	$\leq 1/8X$									
		$t/2 >, \leq 2t$	$\leq W/3$	$\leq 1/8X$									
*W=EFFECTIVE SEAL WIDTH X = LCD SIDE LENGTH t = GLASS THICKNESS													
													
													
	Corner part :		<table><tr><td>a</td><td>b</td><td>c</td></tr><tr><td>$\leq t/2$</td><td>< VIEWING AREA</td><td>$\leq 1/8X$</td></tr><tr><td>$> t/2, \leq 2t$</td><td>$\leq W/3$</td><td>$\leq 1/8X$</td></tr></table>	a	b	c	$\leq t/2$	< VIEWING AREA	$\leq 1/8X$	$> t/2, \leq 2t$	$\leq W/3$	$\leq 1/8X$	
a	b	c											
$\leq t/2$	< VIEWING AREA	$\leq 1/8X$											
$> t/2, \leq 2t$	$\leq W/3$	$\leq 1/8X$											
			*W=EFFECTIVE SEAL WIDTH X=LCD SIDE LENGTH Y=GLASS THICKNESS										
	CHIP ON ELECTRODE PAD		<table><tr><td>a</td><td>b</td><td>c</td></tr><tr><td>$\leq t$</td><td>$\leq 0.5\text{mm}$</td><td>$\leq 1/8X$</td></tr></table>	a	b	c	$\leq t$	$\leq 0.5\text{mm}$	$\leq 1/8X$				
a	b	c											
$\leq t$	$\leq 0.5\text{mm}$	$\leq 1/8X$											
			* X=LCD SIDE WIDTH t =GLASS THICKNESS										
			<table><tr><td>a</td><td>b</td><td>c</td></tr><tr><td>$\leq t$</td><td>$\leq 1/8X$</td><td>$\leq L$</td></tr></table>	a	b	c	$\leq t$	$\leq 1/8X$	$\leq L$				
a	b	c											
$\leq t$	$\leq 1/8X$	$\leq L$											
			*X=LCD SIDE WIDTH t = GLASS THICKNESS L=ELECTRODE PAD LENGTH ①IF GLASS CHIPPING THE ITO TERMINAL, OVER 2/3 OF THE ITO MUST REMAIN AND BE , INSPECTED ACCORDING TO ELECTRODE TERMINAL SPECIFICATIONS ②IF THE PRODUCT WILL BE HEAT SEALED BY THE CUSTOMER, THE ALIGNMENT MARK MUST NOT BE DAMAGED										

11.4 RELIABILITY TEST

11.4.1 STANDARD SPECIFICATIONS FOR RELIABILITY OF LCD MODULE

NO	ITEM	DESCRIPTION
1	High temperature operation	The sample should be allowed to stand at +70°C for 240 hrs
2	Low temperature operation	The sample should be allowed to stand at -20°C for 240 hrs
3	High temperature storage	The sample should be allowed to stand at +80°C for 240 hrs
4	Low temperature storage	The sample should be allowed to stand at -30°C for 240 hrs
5	High temperature / humidity test	The sample should be allowed to stand at 50°C, 90% RH 240 hrs
6	High temperature / high humidity storage	The sample should be allowed to stand at 60°C, 90% RH 240 hrs
7	Thermal shock (not operated)	The sample should be allowed to stand the following 10 cycles of operation : -30°C for 30 minutes +80°C for 30 minutes
8	ESD (Electrostatic Discharge)	AIR DISCHARGE ± 4KV CONTACT DISCHARGE ± 2KV
9	Drop test (1 Box)	6 FACES, 2 CORNERS HEIGHT : 750mm

11.4.2 TESTING CONDITIONS AND INSPECTION CRITERIA

For the final test the testing sample must be stored at room temperature for 24 hours, after the tests listed in table 6.2 , standard specifications for reliability have been executed in order to ensure stability .

NO	ITEM	TEST MODEL	INSPECTION CRITERIA
1	Current consumption	Refer To Specification	The current consumption should conform to the product specification.
2	Contrast	Refer TO Specification	After the tests have been executed, the contrast must be larger than half of its initial value prior to the tests.
3	Appearance	Visual inspection	Defect free

11.4.3LIFE TIME

LIFE TIME	Functions, performance, appearance , etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions room temperature ($25\pm 10^{\circ}\text{C}$) , normal humidity ($45\pm 20\%$ RH) , and in area not exposed to direct sun light. (life time of backlight , please refer to data about backlight .)
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Note : from our experience the life time of high humidity operation and high temperature operation as above mentioned could be achieved .

11.5 OPERATION

- 11.5.1 Do not connect or disconnect modules to or from the main system while power is being supplied .
- 11.5.2 Use the module within specified temperature ; lower temperature causes the retardation of blinking speed of the display ; higher temperature makes overall display discolor . When the temperature returns to normality , the display will operate normally .
- 11.5.3 Adjust the LC driving voltage to obtain the optimum contrast .
- 11.5.4 Power On Sequence input signals should not be supplied to LCD module before power supply voltage is applied and reaches the specified value ($5 \pm 0.25\text{v}$) .
If above sequence is not followed , CMOS LSIs of LCD modules may be damaged due to latch - up problem .

11.6 NOTICE

- 11.6.1 Use a grounded soldering iron when soldering connector I/O terminals . For soldering or repairing , take precaution against the temperature of the soldering iron and the soldering time to prevent peeling off the through-hole-pad .
- 11.6.2 Do not disassemble . EDT shall not be held responsible if the module is disassembled and upon the reassembly the module failed .
- 11.6.3 Do not charge static electricity , as the circuit of this module contains CMOS LSIs. A workman's body should always be static-protected by use of an ESD STRAP . Working clothes for such personnel should be of static-protected material .
- 11.6.4 Always ground the electrically-powered driver before using it to install the LCD module. While cleaning the work station by vacuum cleaner, do not bring the sucking mouth near the module ; static electricity of the electrically-powered driver or the vacuum cleaner may destroy the module .
- 11.6.5 Don't give external shock.
- 11.6.6 Don't apply excessive force on the surface.
- 11.6.7 Liquid in LCD is hazardous substance .Must not lick and swallow.
When the liquid is attach to your,skin,cloth etc.wash it out thoroughly and immediately.
- 11.6.8 Don't operate it above the absolute maximum rating.
- 11.6.9 Storage in a clean environment, free from dust,active gas,and solvent.
- 11.6.10 Store without any physical load.
- 11.6.11 Rewiring : no more than 3 times .