

TFT Evaluation Kit

User manual

CUSTOMER		
PRODUCT NUMBER	TFT-I-Kit-001	
CUSTOMER APPROVAL		Date

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Elijah Ebo	Anthony Perkins	Bazile Peter
Date: 04/09/07	Date: 04/09/07	Date: 04/09/07

TABLE OF CONTENTS

1	INTRODUCTION.....	4
2	SETTING UP THE KIT.....	5
3	TFT PANEL	6
3.1	TFT MECHANICAL PARAMETERS	6
3.2	ELECTRICAL PARAMETERS.....	7
4	EDD50200/IB520 SBC	10
4.1	INTRODUCTION.....	10
4.2	SPECIFICATIONS	11
4.3	BOARD DIMENSIONS	12
4.4	INSTALLATIONS	13
4.5	SETTING THE JUMPERS	14
4.6	CONNECTORS ON THE IB520.....	16
4.7	BIOS SETUP	24
4.8	DRIVERS INSTALLATION	35
5	TECHNICAL SUPPORT	47

Product No.	TFT-I-Kit-001	REV. A

Page	2 / 47
------	--------

REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	04/09/07			First revision	



1 Introduction

This user manual contains the instructions on setting up and using the Densitron Kyocera TFT evaluation kit.

The evaluation kit contains:

- 1 x Kyocera TCG104VG2AA 10.4" TFT panel
 - o Anti glare treatment
 - o (640 x R.G.B) x 480 dots
 - o COG LCD with side edge type CFL Backlight (2 tubes).
 - o Recommended inverter TDK CXA-0308
 - o Dimensions: 243 x 185.1 x 10.5 mm
 - o Effective Viewing Area: 213.2 x 160.4 mm
 - o Dot Pitch: 0.11 x 0.33 mm
 - o 3.3V/5.0V supply
 (Please refer to datasheet for full specifications).
- 1 x AMD Geode LX SBC with cable set
- CCFL Inverter and cables
- Display cable
- 12V 5A Power supply
- Documentation CD with chipset drivers and flash memory utility.

The documentation CD contains the manual for the parts that make up the kit.

WARNING: THE INVERTER SHOULD NEVER BE EXPOSED TO THE TOUCH WHILST THE SYSTEM IS POWERED, AS IT PRODUCES HIGH VOLTAGES AND IS A SHOCK HAZZARD.

Product No.	TFT-I-Kit-001	REV. A

Page	4 / 47
------	--------

2 Setting up the kit

The kit should be unpacked in a static-free environment, with adequate anti-static precautions being observed.

The cables are all keyed and only one cable from the kit will fit each of the connection steps described below:

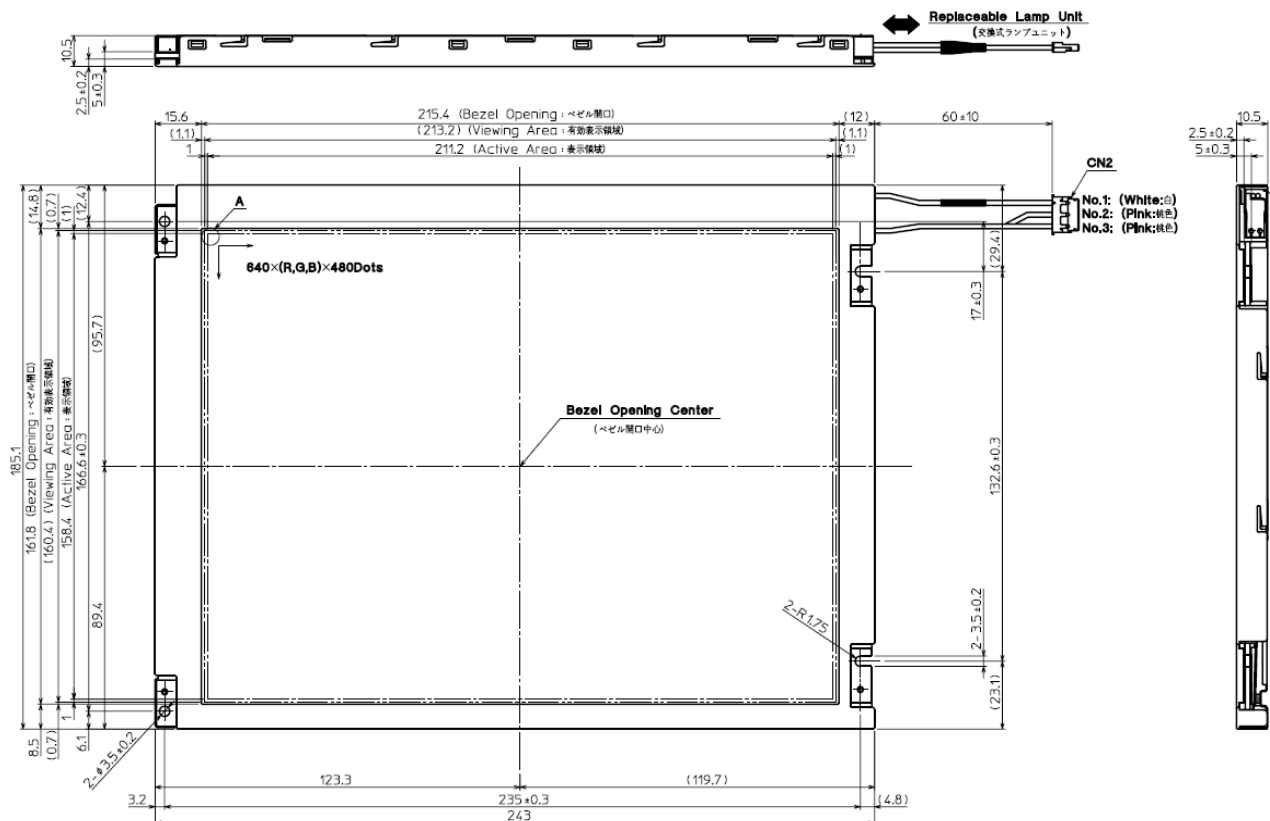
- 1) Connect the display to the inverter by connecting the pink and white cables protruding from the display to CN2 on the inverter.
- 2) Connect the other end of the inverter (CN1) to the inverter cables and connect the other end of the inverter cable to the 12V power supply.
- 3) Check that a CF card (preloaded with an operating system) is plugged into the SBC (CN1).
- 4) Connect the display cable into the display and the other end to the TFT interface J6 on the SBC.
- 5) Connect a keyboard and a mouse to CN4.
- 6) Check the jumper settings on the SBC according to the latter sections of this document and confirm that they are correctly set.**
- 7) Ensure that the inverter is safely located, away from any metal objects and protected from being touched.**
- 8) Consult the SBC section of this document for the SBC set-up procedure.
- 9) Connect the 12V power supply to J3 on the SBC and plug the power supply into the mains.
- 10) The SBC should boot up immediately.

Product No.	TFT-I-Kit-001	REV. A

Page	5 / 47
------	--------

3 TFT PANEL

3.1 TFT mechanical parameters



Note (注記)

- 1 Connector (コネクタ) CN1: DF9C-31P-1V(32) (HIROSE)
CN2: BHR-03VS-1 (JST)
- 2 Matching Connector (適合コネクタ) CN1: DF9W-31S-1V (HIROSE)
DF9W-31S-1V(32) (HIROSE)
CN2: SM03(4.0)B-BHS-1-TB (JST)
SM03(4.0)B-BHS-1-TB-ILF(SNI) (JST)
3. The information of LCD is displayed starting at the lower right hand corner, moving left then up to the upper left hand corner.
(LCDにおいて、画像データの表示は右下コーナーから始まり、左へ進み上へ進み左上コーナーへ向かう。)
- 4 Tolerance without indication: ± 0.5
(指示無し公差)

Product No.	TFT-I-Kit-001	REV. A
-------------	---------------	--------

Page	6 / 47
------	--------

3.2 Electrical parameters

3.2.1 A
b
s
o
l

Item	Symbol	Min.	Max.	Unit
Power input voltage	VDD	-0.3	6.0	V
Input signal voltage	Vin	-0.3	VDD + 0.3	V

ute maximum

3.2.2 Electrical Characteristics

Temp = 25°C

Item		Symbol	Min.	Typ.	Max.	Unit
Power supply voltage		VDD	3.0	3.3/5.0	5.25	V
Power supply current	White (a)	-	-	(495)	-	mA
	Black (b)	-	-	(450)	-	
	Vertical Stripe (C)	-	-	(563)	-	
Permissive input ripple voltage		VRP	-	-	100	mVp-p
Rush Current		IRUSH	-	-	(1)	A
Input signal voltage (Low)		VIL	-	-	0.3VDD	V
Input signal voltage (High)		VIH	0.7VDD	-	VDD	V

Product No.	TFT-I-Kit-001	REV. A

Page	7 / 47
------	--------

3.2.3 Interface Signals

PIN NO.	SYMBOL	DESCRIPTION	I/O	Note
1	GND	GND	–	
2	CK	Clock signal for sampling each data signal	I	
3	Hsync	Horizontal synchronous signal (negative)	I	
4	Vsync	Vertical synchronous signal (negative)	I	
5	GND	GND	–	
6	R0	RED data signal (LSB)	I	
7	R1	RED data signal	I	
8	R2	RED data signal	I	
9	R3	RED data signal	I	
10	R4	RED data signal	I	
11	R5	RED data signal (MSB)	I	
12	GND	GND	–	
13	G0	GREEN data signal (LSB)	I	
14	G1	GREEN data signal	I	
15	G2	GREEN data signal	I	
16	G3	GREEN data signal	I	
17	G4	GREEN data signal	I	
18	G5	GREEN data signal (MSB)	I	
19	GND	GND	–	
20	B0	BLUE data signal (LSB)	I	
21	B1	BLUE data signal	I	
22	B2	BLUE data signal	I	
23	B3	BLUE data signal	I	
24	B4	BLUE data signal	I	
25	B5	BLUE data signal (MSB)	I	
26	GND	GND	–	
27	DE	Signal to settle the horizontal display position(positive)	I	
28	VDD	power supply(+3.3V/+5.0V)	–	
29	VDD	power supply(+3.3V/+5.0V)	–	
30	NC	No connect	I	*1
31	SC	Scan direction control (GND or Open : normal, High : Reverse)	I	*2

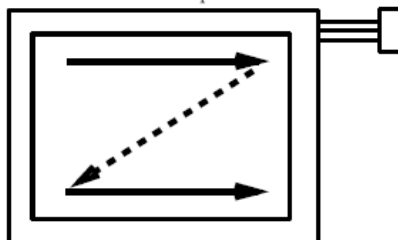
LCD side connector : DF9C-31P-1V(32) (HIROSE)
Recommended matching connector : DF9-31S-1V, DF9A-31S-1V(32) (HIROSE)
DF9B-31S-1V(32), DF9C-31S-1V(32) (HIROSE)

* The shield case is connected with GND.

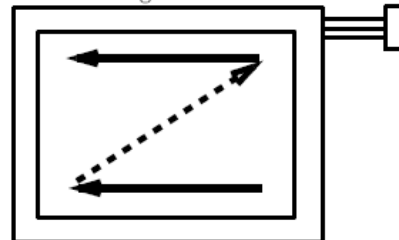
*1 Do not input any signal at Pin No.30(Open state). It might happen LCD has a trouble.

*2 Scanning Direction

SC : GND or Open



SC : High



3.2.4 CFL Backlight pin descriptions

Pin No.	Symbol	Description
1	COLD	Inverter output low voltage side
2	HOT	Inverter output high voltage side
3	HOT	Inverter output high voltage side

LCD side connector: BHR-03VS-1

Recommended matching connector: SM03-(4.0)B-BHS-1 (JST)

SM03-(4.0)B-BHS-1-TB(LF) (SN) (JST)

3.2.5 Backlight Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Note
Starting discharge Voltage *1	VS	-	-	1,325	Vrms	-10
		-	-	830		25
Discharging tube current *2	IL	2.0	5.0	6.0	mArms	-
Discharging tube voltage	VL	-	490	-	Vrms	IL = 5.0 mArms
Operating frequency*3	F	40	-	100	kHz	-
Operating Life*4	T	36,000	50,000	-	hours	IL = 5.0 mArms

*1 The Non-load output voltage (VS) of the inverter should be designed to have some margin, because VS may increase due to the leak current which may be caused by wiring of CFL cables.

(Reference value: (1,720) Vrms Min.)

*2 We recommend that you should set the discharging tube current at lower than typical value so as to prevent the heat accumulation of CFL tube from deteriorating the performance of the LCD.

*3 The driving frequency of the CFL may interfere with the horizontal synchronous signal, leaving interference of stripes on the display. So please evaluate LCD panels beforehand. To avoid interference stripes, we recommend to separate as far as possible the CFL frequency from the horizontal synchronous signal and its high harmonic frequency.

*4 End of life is defined as when the luminance or quality of light has decreased to 50% of the initial value. Luminance of light will drastically decrease when LCD is operated at lower temperature for long hours.

*There may be cases where interference noise on LCD PCB, generated by high-voltage products such as inverters, may leave stripes on the display. Please be careful when designing a mould to take into consideration that the inverter shall be located as far as possible from PCB. Shield protection may be effective.

Product No.	TFT-I-Kit-001	REV. A

Page	9 / 47
------	--------

4 EDD50200/IB520 SBC

Acknowledgments

Award is a registered trademark of Award Software International, Inc.

PS/2 is a trademark of International Business Machines Corporation.

AMD, AMD Geode, and combinations thereof, are trademarks of Advanced Micro Devices, Inc.

Microsoft Windows is a registered trademark of Microsoft Corporation.

All other product names or trademarks are properties of their respective owners.

4.1 Introduction

The IB520 3.5-inch disk size SBC incorporates the AMD Geode LX processor with speeds of 433MHz (LX700) or 500MHz (LX800). It comes with one DDR SO-DIMM socket that has a capacity of 1GB system memory. The board supports one 10/100Mbps Ethernet, using a Realtek RTL8100C controller. A 2D graphics controller comes integrated on the board that supports CRT and TFT LCD displays. Useful interface includes four USB 2.0 ports, 2 COM ports, and one PCI-104 expansion slot. Other expansion options are available with the Compact Flash socket and PCMCIA connector.

IB520 FEATURES:

- Embedded AMD Geode LX processor, 433MHz (LX700) / 500MHz (LX800)
- DDR SO-DIMM x 1, Max. 1GB
- Realtek RTL8100C 10/100Mbps Ethernet
- Integrated LX800/LX700 2D VGA controller, supports CRT and TFT LCD display
- 4 x USB 2.0, 2 x COM, CF socket, Watchdog timer, Digital I/O
- PCI-104 expansion, optional PCMCIA connector
- Dimensions: 145mm x 102mm (5.7" x 4")

Product No.	TFT-I-Kit-001	REV. A

Page	10 / 47
------	---------



4.2 Specifications

CPU	AMD Geode LX CPU, 481-ball BGA
CPU Internal Speed	LX800 @500MHz LX700 @433MHz
Power Management	APM
BIOS	Award BIOS
Chipset	AMD CS5536 I/O companion multi-function south bridge
Memory	One DDR SO-DIMM socket, Max. up to 1GB
Graphic	LX800/LX700 built-in high performance 2D graphic controller, supports TFT, LVDS LCD & CRT display
LVDS	24-bit single channel LVDS
Ethernet	Realtek RTL8100C-LF 10/100Mbps Ethernet chip
IDE	CS5536 built-in one channel UDMA100 IDE - 44-pin header x1 - Compact Flash (type II) connector x1
Audio	Realtek ALC203 AC97 audio codec, supports 2-CH Line-Out, Line-In & MIC
USB	CS5536 built-in USB2.0 controller, support 4 ports
PCMCIA	TI PCI1510 Card bus controller (IB520F only)
LPC I/O	Winbond W83627HF: KB/Mouse controller, Parallel, IrDA, Floppy, COM1, COM2 (RS232) & Hardware monitor (3 thermal inputs, 4 voltage monitor inputs, VID0-4 & 2 Fan Headers)
PCI Arbiter	AT209S PCI arbiter/clock buffer, extend PCI devices (master) from 1 to 3
RTC	CS5536 built-in, with on board Lithium battery
Edge Connectors	DB-9 connector x1 for COM1 (RS232 only) 6-pins Mini-DIN connector x1 for PS/2 KB & Mouse (Y cable) USB connector x1 for USB0 DB-15 connector x1 for CRT RJ-45 connector x1 for LAN
Onboard Headers	PCMCIA connector x1 for Card Bus (IB520F only) DF13-20 header x1 for LVDS channel Compact Flash Socket x1 for CF card 10-pin header x1 for COM2 (RS232 only) 4-pin header for USB1 10-pin header x1 for USB2, 3 26-pin header x1 for LPT port 44-pin header x1 for IDE 34-pin header x1 for FDD 12-pin header x1 for Audio 4-pin header x1 for IrDA 10-pin header x1 for Digital I/O 44-pin header x1 for TFT LCD panel
Expansion Slot	PCI-104 w/ 4 mounting holes
Digital I/O	Supports 4 In / 4 Out
Power	+12V DC-in
Watchdog	Software programmable, supports 1~255 sec. system reset
Timer	
RoHS	Yes
Compliant	
Board Size	145 x 102mm

Product No.	TFT-I-Kit-001	REV. A

Page	11 / 47
------	---------



4.4 Installations

This section provides information on how to use the jumpers and connectors on the IB520 in order to set up a workable system. The topics covered are:

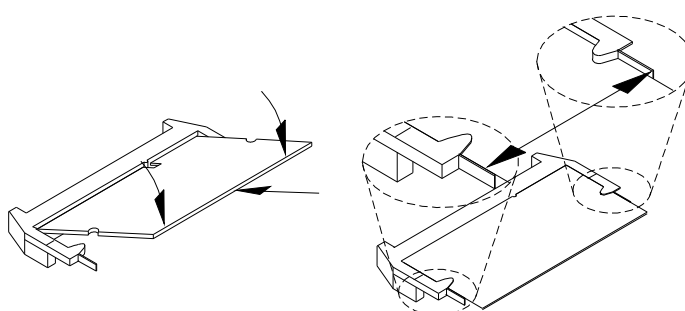
4.4.1 Installing the Memory

The IB520 board supports one SODIMM DDR memory socket for a maximum total memory. The memory module capacities supported are 128MB, 256MB, 512MB and 1GB.

Installing and Removing Memory Modules

To install the DDR modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR module so that the key of the DDR module align with those on the memory slot. Insert the module into the socket at a slight angle (approximately 30 degrees). Note that the socket and module are both keyed, which means that the module can be installed only in one direction.
2. To seat the memory module into the socket, apply firm and even pressure to each end of the module until you feel it slip down into the socket.
3. With the module properly seated in the socket, rotate the module downward. Continue pressing downward until the clips at each end lock into position.
4. To remove the DDR module, press the clips with both hands.



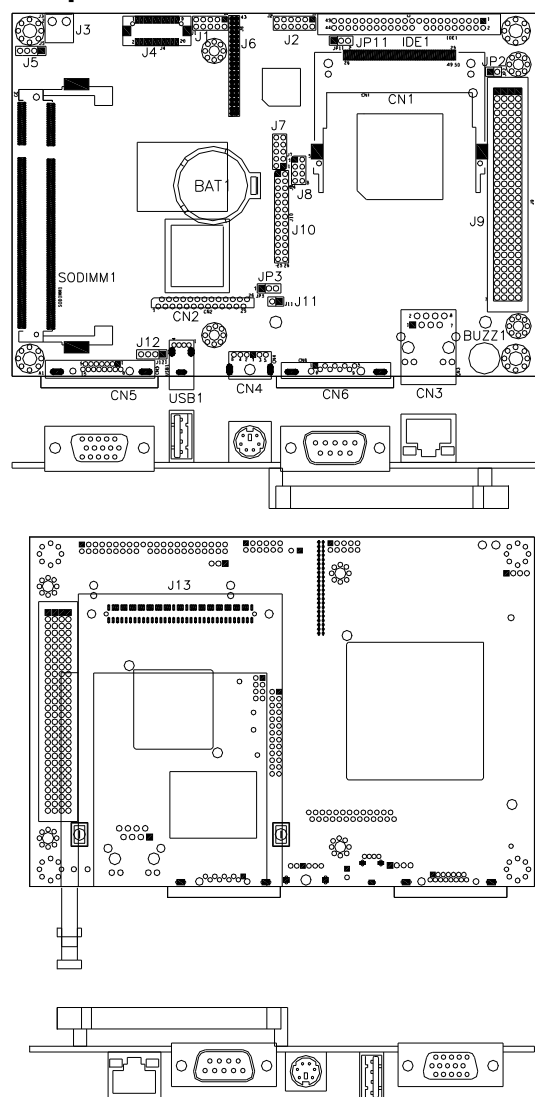
Product No.	TFT-I-Kit-001	REV. A

Page	13 / 47

4.5 Setting the Jumpers

Jumpers are used on IB520 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following section lists the connectors on IB520 and their respective functions.



Jumper Locations on IB520





Product No.	TFT-I-Kit-001	REV. A

Page	14 / 47
------	---------

JP1: LVDS VDD Select (5V / 3.3V)



JP1	VDD Setting
 1 2 3	3.3V
 1 2 3	5V

JP2: CF Connector master/Slave Setting

JP2	Setting	Function
 1 2	Short/Closed	Master
 1 2	Open	Slave

JP3: Clear CMOS Setting

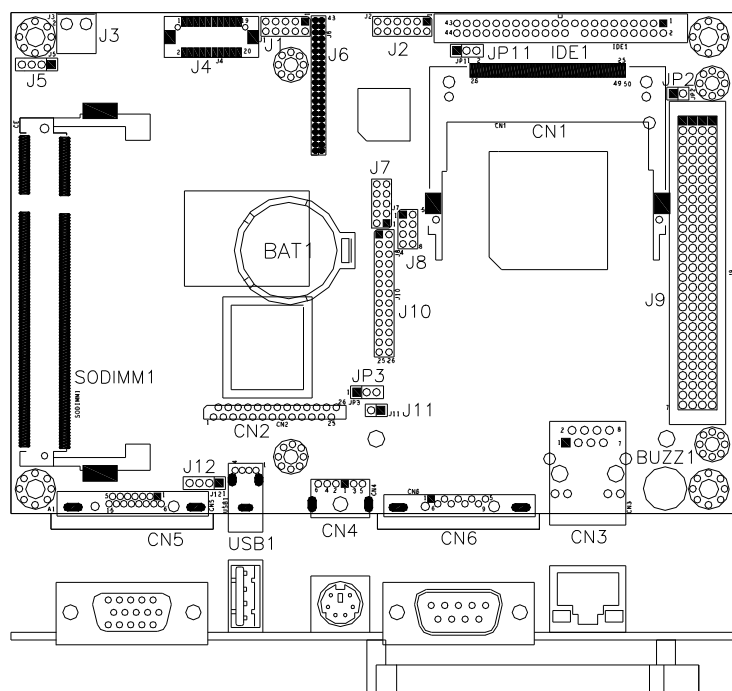
Use JP3 to clear the CMOS contents. *Note that the power connector should be disconnected from the board before clearing CMOS.*

JP3	Function
 1 2 3	Normal (default)
 1 2 3	Clear CMOS

4.6 Connectors on the IB520

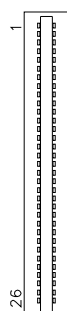
The connectors on the IB520 allow you to connect external devices such as keyboard, floppy disk drives, hard disk drives, printers, etc. The following section lists the connectors on the IB520 and their respective functions.

Connector Locations on IB520



CN1: Compact Flash Card Socket - Standard compact flash specification.

CN2: FDD Connector

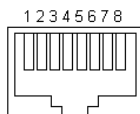


Signal Name	Pin #	Pin #	Signal Name
VCC	1	2	INDEX
VCC	3	4	DRV_SEL
VCC	5	6	DSK_CH
NC	7	8	NC
NC	9	10	MOTOR
DINST	11	12	DIR
NC	13	14	STEP
GND	15	16	WDATA
GND	17	18	WGATE
GND	19	20	TRACK
NC	21	22	WPROT
GND	23	24	RDATA
GND	25	26	SIDE

Product No.	TFT-I-Kit-001	REV. A
-------------	---------------	--------

Page	16 / 47
------	---------

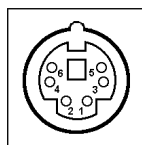
CN3:RJ45 Connector



Pin #	Signal Name
1	TD+
2	TD-
3	RD+
4	RJ45-4A
5	RJ45-5A
6	RD-
7	RJ45-7A
8	RJ45-8A

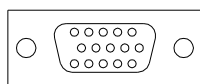
CN4: PS/2 Keyboard and Mouse Connector

CN4 uses a Y-cable with dual D-connectors for a PS/2 keyboard and a PS/2 mouse.



Pin #	Signal Name
1	Keyboard data
2	Mouse data
3	Ground
4	Vcc
5	Keyboard Clock
6	Mouse Clock

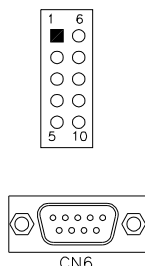
CN5: VGA CRT Connector



Signal Name	Pin	Pin	Signal Name
Red	1	2	Green
Blue	3	4	NC
GND	5	6	GND
GND	7	8	GND
Vcc	9	10	GND
N.C.	11	12	DDCDA
HSYNC	13	14	VSYNC
DDCCLK	15		

Product No.	TFT-I-Kit-001	REV. A	Page	17 / 47
-------------	---------------	--------	------	---------

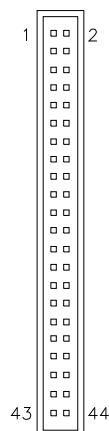
CN6, J7: Serial Ports



Pin #	Signal Name (RS-232)
1	DCD, Data carrier detect
2	RXD, Receive data
3	TXD, Transmit data
4	DTR, Data terminal ready
5	Ground
6	DSR, Data set ready
7	RTS, Request to send
8	CTS, Clear to send
9	RI, Ring indicator
10	No Connect.

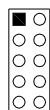
CN6 is the D-sub type COM1 serial port connector, while J7 (COM2) is a pin header type COM2 serial port connector.

IDE1: IDE Connector



Signal Name	Pin #	Pin #	Signal Name
Reset IDE	1	2	Ground
Host data 7	3	4	Host data 8
Host data 6	5	6	Host data 9
Host data 5	7	8	Host data 10
Host data 4	9	10	Host data 11
Host data 3	11	12	Host data 12
Host data 2	13	14	Host data 13
Host data 1	15	16	Host data 14
Host data 0	17	18	Host data 15
Ground	19	20	Key
DRQ0	21	22	Ground
Host IOW	23	24	Ground
Host IOR	25	26	Ground
IOCHRDY	27	28	Host ALE
DACK0	29	30	Ground
IRQ14	31	32	No connect
Address 1	33	34	No connect
Address 0	35	36	Address 2
Chip select 0	37	38	Chip select 1
Activity	39	40	Ground
Vcc	41	42	Vcc
Ground	43	44	N.C.

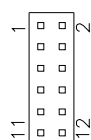
J1: Digital 4-in 4-out Connector



Signal Name	Pin	Pin	Signal Name
Ground	1	2	Vcc
Out3	3	4	Out1
Out2	5	6	Out0
IN3	7	8	IN1
IN2	9	10	IN0

J2: External Audio Connector

J2 is a 12-pin header that is used to connect to the optional audio cable card that integrates jacks for Line In, Line Out and Mic.



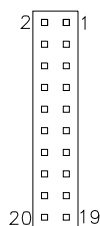
Signal Name	Pin #	Pin #	Signal Name
LINEOUT_R	1	2	LINEOUT_L
Ground	3	4	Ground
LINEIN_R	5	6	LINEIN_L
Ground	7	8	Ground
Mic-In	9	10	VREFOUT
Ground	11	12	Protect pin

J3: Power DC-In



Pin #	Signal Name
1	DC In (12v only)
2	Ground

J4: LVDS Connectors



Signal Name	Pin #	Pin #	Signal Name
TX0-	2	1	TX0+
Ground	4	3	Ground
TX1-	6	5	TX1+
5V/3.3V	8	7	Ground
TX3-	10	9	TX3+
TX2-	12	11	TX2+
Ground	14	13	Ground
TXC-	16	15	TXC+
*5V/3.3V	18	17	ENABKL
+12V	20	19	+12V

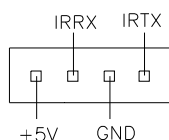
*Depends on JP1 setting (1-2 for 3.3V/default, 2-3 for 5V).

Product No.	TFT-I-Kit-001	REV. A
-------------	---------------	--------

Page	19 / 47
------	---------

J5: IrDA Connector

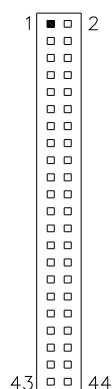
J5 is used for an optional IrDA connector for wireless communication.



Pin #	Signal Name
1	+5V
2	Ir RX
3	Ground
4	Ir TX

J6: TFT Panel Connector

J6 is the pin header for TFT flat panel LCD displays.



Signal Name	Pin #	Pin #	Signal Name
+12V	1	2	+12V
Ground	3	4	Ground
5V/3.3V	5	6	5V/3.3V
N.C.	7	8	Ground
R0	9	10	R1
R2	11	12	R3
R4	13	14	R5
R6	15	16	R7
G0	17	18	G1
G2	19	20	G3
G4	21	22	G5
G6	23	24	G7
B0	25	26	B1
B2	27	28	B3
B4	29	30	B5
B6	31	32	B7
Ground	33	34	Ground
SHFCLK	35	36	FLM(VSYNC)
DISPENA(MDE)	37	38	LP(HSYNC)
Ground	39	40	ENABKL
Ground	41	42	N.C.
ENAVDD	43	44	* 5V/3.3V

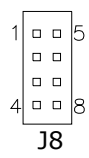
***Depends on JP1 setting (1-2 for 3.3V/default, 2-3 for 5V).**

Product No.	TFT-I-Kit-001	REV. A
-------------	---------------	--------


Page	20 / 47
------	---------

USB1, J8, J12: USB Connectors

The J8, J12 USB pin header connectors support three USB 2.0 ports via optional USB cables. The IB520 also supports an embedded USB connector, USB1, which supports another USB 2.0 port.

 J8	Signal Name	Pin	Pin	Signal Name
	+5V	1	5	Ground
	USB0-	2	6	USB1+
	USB0+	3	7	USB1-
	Ground	4	8	+5V

Pin #	Signal Name
1	+5V
2	USB-
3	USB+
4	Ground



J12



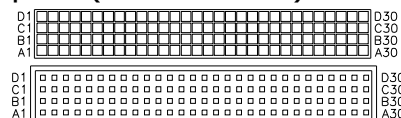
J9: PCI-104 Connector

4.6.1.1 PCI-104 Bus Signal Assignments

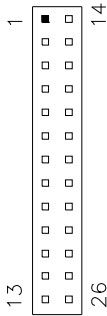
J3/P3				
Pin	A	B	C	D
1	GND/5.0V KEY ²	Reserved	+5	AD00
2	VI/O	AD02	AD01	+5V
3	AD05	GND	AD04	AD03
4	C/BE0*	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3V	C/BE1*	AD15	+3.3V
9	SERR*	GND	SB0*	PAR
10	GND	PERR*	+3.3V	SDONE
11	STOP*	+3.3V	LOCK*	GND
12	+3.3V	TRDY*	GND	DEVSEL*
13	FRAME*	GND	IRDY*	+3.3V
14	GND	AD16	+3.3V	C/BE2*
15	AD18	+3.3V	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3V	AD23	AD22	+3.3V
18	IDSEL0	GND	IDSEL1	IDSEL2
19	AD24	C/BE3*	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5V	AD28	AD27
22	+5V	AD30	GND	AD31
23	REQ0*	GND	REQ1*	VI/O
24	GND	REQ2*	+5V	GNT0*
25	GNT1*	VI/O	GNT2*	GND
26	+5V	CLK0	GND	CLK1
27	CLK2	+5V	CLK3	GND
28	GND	INTD*	+5V	RST*
29	+12V	INTA*	INTB*	INTC*
30	-12V	Reserved	Reserved	GND/3.3V KEY ²

* The shaded area denotes power or ground signals.

* The KEY pins are to guarantee proper module installation. Pin-A1 will be removed and the female side plugged for 5.0V I/O signals and Pin-D30 will be modified in the same manner for 3.3V I/O. It is recommended that both KEY pins (A1 and D30) be electrically connected for GND for shielding.



J10: Parallel Port Connector

	Signal Name	Pin #	Pin #	Signal Name
	Line printer strobe	1	14	AutoFeed
	PD0, parallel data 0	2	15	Error
	PD1, parallel data 1	3	16	Initialize
	PD2, parallel data 2	4	17	Select
	PD3, parallel data 3	5	18	Ground
	PD4, parallel data 4	6	19	Ground
	PD5, parallel data 5	7	20	Ground
	PD6, parallel data 6	8	21	Ground
	PD7, parallel data 7	9	22	Ground
	ACK, acknowledge	10	23	Ground
	Busy	11	24	Ground
	Paper empty	12	25	Ground
	Select	13	N/A	N/A

J11: Reset Switch



Pin #	Signal Name
1	Reset
2	Ground

J13: Cardbus Connector

SODIMM1: SO DIMM Socket

Product No.	TFT-I-Kit-001	REV. A

Page	23 / 47
------	---------

4.7 BIOS Setup

This chapter describes the different settings available in the Award BIOS that comes with the board.

BIOS Introduction

The Award BIOS (Basic Input/Output System) installed in your computer system's ROM supports various processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also adds virus and password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The Award BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the Award BIOS is immediately activated. Pressing the key immediately allows you to enter the Setup utility. If you are a little bit late pressing the key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

Press to Enter Setup

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Phoenix - AwardBIOS CMOS Setup Utility	
Standard CMOS Features	Load Fail-Safe Defaults
Advanced BIOS Features	Load Optimized Defaults
Advanced Chipset Features	Set Supervisor
Integrated Peripherals	Set User Password
Power Management Setup	Save & Exit Setup
PnP/PCI Configurations	Exit Without Saving
PC Health Status	
ESC : Quit	↑ ↓ → ← : Select Item
F10 : Save & Exit Setup	
Time, Date, Hard Disk Type...	

The section below the setup items of the Main Menu displays the control keys for this menu. At the bottom of the Main Menu just below the control keys section, there is another section, which displays information on the currently highlighted item in the list.

Product No.	TFT-I-Kit-001	REV. A

Page	24 / 47

Note: *If the system cannot boot after making and saving system changes with Setup, the Award BIOS supports an override to the CMOS settings that resets your system to its default.*

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both Award and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

Product No.	TFT-I-Kit-001	REV. A

Page	25 / 47
------	---------



Standard CMOS Setup

"Standard CMOS Setup" choice allows you to record some basic hardware configurations in your computer system and set the system clock and error handling. If the motherboard is already installed in a working system, you will not need to select this option. You will need to run the Standard CMOS option, however, if you change your system hardware configurations, the onboard battery fails, or the configuration stored in the CMOS memory was lost or damaged.

Phoenix - AwardBIOS CMOS Setup Utility Standard CMOS Features		
Date (mm:dd:yy)	Fri, Jun 30, 2006	Item Help
Time (hh:mm:ss)	00 : 00 : 00	Menu Level >
IDE Primary Master	None	Change the day, month, Year and century
IDE Primary Slave	None	
Drive A	1.44M, 3.5 in.	
Drive B	None	
Video	EGA/VGA	
Halt On	All, But keyboard	
Base Memory	640K	
Extended Memory	514816K	
Total Memory	515584K	

At the bottom of the menu are the control keys for use on this menu. If you need any help in each item field, you can press the <F1> key. It will display the relevant information to help you. The memory display at the lower right-hand side of the menu is read-only. It will adjust automatically according to the memory changed. The following describes each item of this menu.

Date

The date format is:

Day : Sun to Sat
Month : 1 to 12
Date : 1 to 31
Year : 1999 to 2099

To set the date, highlight the "Date" field and use the PageUp/ PageDown or +/- keys to set the current time.

Product No.	TFT-I-Kit-001	REV. A

Page	26 / 47

Time

The time format is: **Hour** : 00 to 23
Minute : 00 to 59
Second : 00 to 59

To set the time, highlight the "Time" field and use the <PgUp>/ <PgDn> or +/- keys to set the current time.

IDE Primary HDDs / IDE Secondary HDDs

The onboard PCI IDE connectors provide Primary and Secondary channels for connecting up to four IDE hard disks or other IDE devices. Each channel can support up to two hard disks; the first is the "Master" and the second is the "Slave".

Press <Enter> to configure the hard disk. The selections include Auto, Manual, and None. Select 'Manual' to define the drive information manually. You will be asked to enter the following items.

CYLS : Number of cylinders
HEAD : Number of read/write heads
PRECOMP : Write precompensation
LANDING ZONE : Landing zone
SECTOR : Number of sectors

The Access Mode selections are as follows:

CHS (HD < 528MB)
LBA (HD > 528MB and supports Logical Block Addressing)
Large (for MS-DOS only)
Auto

Remarks: The main board supports two serial ATA ports and are represented in this setting as IDE Channel 2 / 3 Master.

Drive A / Drive B

These fields identify the types of floppy disk drive A or drive B that has been installed in the computer. The available specifications are:

360KB 1.2MB 720KB 1.44MB 2.88MB
5.25 5.25 3.5 in. 3.5 in. 3.5 in.
in. in.

Product No.	TFT-I-Kit-001	REV. A

Page	27 / 47



Video

This field selects the type of video display card installed in your system. You can choose the following video display cards:

EGA/VGA	For EGA, VGA, SEGA, SVGA or PGA monitor adapters. (default)
CGA 40	Power up in 40 column mode.
CGA 80	Power up in 80 column mode.
MONO	For Hercules or MDA adapters.

Halt On

This field determines whether or not the system will halt if an error is detected during power up.

No errors	The system boot will not be halted for any error that may be detected.
All errors	Whenever the BIOS detects a non-fatal error, the system will stop and you will be prompted.
All, But Keyboard	The system boot will not be halted for a keyboard error; it will stop for all other errors
All, But Diskette	The system boot will not be halted for a disk error; it will stop for all other errors.
All, But Disk/Key	The system boot will not be halted for a key- board or disk error; it will stop for all others.

Product No.	TFT-I-Kit-001	REV. A

Page	28 / 47
------	---------



Advanced BIOS Features

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Phoenix - AwardBIOS CMOS Setup Utility Advanced BIOS Features		
Virus Warning	Disabled	ITEM HELP
CPU Internal Cache	Enabled	Menu Level >
First Boot Device	Floppy	
Second Boot Device	HDD-0	
Third Boot Device	CDROM	
Boot Other Device	Enabled	
Swap Floppy Drive	Disabled	
Boot Up Floppy Seek	Enabled	
Boot Up NumLock Status	On	
Gate A20 Option	Fast	
Typematic Rate Setting	Disabled	
Typematic Rate (Chars/Sec)	6	
Typematic Delay (Msec)	250	
Security Option	Setup	
OS Select For DRAM>64MB	Non-OS2	
Small Logo (EPA) Show	Disabled	

Virus Warning

If this option is enabled, an alarm message will be displayed when trying to write on the boot sector or on the partition table on the disk, which is typical of the virus.

CPU Internal Cache

Cache memory is additional memory that is much faster than conventional DRAM (system memory). CPUs from 486-type on up contain internal cache memory, and most, but not all, modern PCs have additional (external) cache memory. When the CPU requests data, the system transfers the requested data from the main DRAM into cache memory, for even faster access by the CPU.

First/Second/Third Boot Device

These fields determine the drive that the system searches first for an operating system. The options available include *Floppy*, *LS120*, *HDD-0*, *SCSI*, *CDROM*, *HDD-1*, *HDD-2*, *HDD-3*, *ZIP100*, *USB-FDD*, *LAN*, *USB-CDROM*, *USB-HDD* and *Disable*.

Boot Other Device

These fields allow the system to search for an OS from other devices other than the ones selected in the First/Second/Third Boot Device.

Swap Floppy Drive

This item allows you to determine whether or not to enable Swap Floppy Drive. When enabled, the BIOS swaps floppy drive assignments so that Drive A becomes Drive B, and Drive B becomes Drive A. By default, this field is set to **Disabled**.

Boot Up Floppy Seek

This feature controls whether the BIOS checks for a floppy drive while booting up. If it cannot detect one (either due to improper configuration or its absence), it will flash an error message.

Boot Up NumLock Status

This allows you to activate the NumLock function after you power up the system.

Gate A20 Option

This field allows you to select how Gate A20 is worked. Gate A20 is a device used to address memory above 1 MB.

Product No.	TFT-I-Kit-001	REV. A

Page	29 / 47
------	---------

Typematic Rate Setting

When disabled, continually holding down a key on your keyboard will generate only one instance. When enabled, you can set the two typematic controls listed next. By default, this field is set to **Disabled**.

Typematic Rate (Chars/Sec)

When the typematic rate is enabled, the system registers repeated keystrokes speeds. Settings are from 6 to 30 characters per second.

Typematic Delay (Msec)

When the typematic rate is enabled, this item allows you to set the time interval for displaying the first and second characters. By default, this item is set to **250msec**.

Security Option

This field allows you to limit access to the System and Setup. The default value is **Setup**. When you select *System*, the system prompts for the User Password every time you boot up. When you select *Setup*, the system always boots up and prompts for the Supervisor Password only when the Setup utility is called up.

OS Select for DRAM > 64MB

This option allows the system to access greater than 64MB of DRAM memory when used with OS/2 that depends on certain BIOS calls to access memory. The default setting is **Non-OS/2**.

Small Logo (EPA) Show

The EPA logo appears at the right side of the monitor screen when the system is boot up.

Advanced Chipset Features

This Setup menu controls the configuration of the chipset.

Phoenix - AwardBIOS CMOS Setup Utility Advanced Chipset Features		
CPU Frequency	Auto	ITEM HELP
Memory Frequency	133 MHz	Menu Level >
CAS Latency	Auto	
Video Memory Size	8M	
Output Display	Panel & CRT	
Flat Panel Configuration	Press Enter	
Onboard Audio	Enabled	
Overcurrent Reporting	Disabled	
Port 4 Assignment	Host	

CPU Frequency

This options for this field are **Auto**, **433MHz** and **500MHz**.

Memory Frequency

This default setting for this field is **133MHz**.

CAS Latency Time

You can configure CAS latency time in HCLKs as **1.5**, **2**, **2.5**, **3** or **3.5**. The system board designer should set the values in this field, depending on the DRAM installed. Do not change the values in this field unless you change specifications of the installed DRAM or the installed CPU.

Product No.	TFT-I-Kit-001	REV. A

Page	30 / 47
------	---------

Video Memory Size

The default setting for this field is **8M**. The options are from **8M** to **254M**.

Flat Panel Configuration

This options for this field are **Flat Panel**, **CRT** and **Panel & CRT**. For flat panel, configuration settings include Flat Panel Type, Resolution (320x240 up to 1600x1200), Data Bus Type, Refresh Rate (60~100Hz), HSYNC Polarity, VSYNC Polarity, SHFCLK Active Period and LP Active Period.

Integrated Peripherals

This section sets configurations for your hard disk and other integrated peripherals. The first screen shows three main items for user to select. Once an item selected, a submenu appears. Details follow.

Phoenix - AwardBIOS CMOS Setup Utility		
Integrated Peripherals		
OnChip IDE Channel 1	Enabled	ITEM HELP
Master Drive PIO Mode	Auto	Menu Level >
Slave Drive PIO Mode	Auto	
IDE Primary Master UDMA	Disabled	
IDE Primary Slave UDMA	Disabled	
IDE DMA transfer access	Enabled	
IDE HDD Block Mode	Enabled	
Onboard LAN Boot ROM	Disabled	
Onboard FDC Controller	Enabled	
Onboard Serial Port 1	3F8/IRQ4	
Onboard Serial Port 2	2F8/IRQ3	
UART Mode Select	Normal	
Onboard Parallel Port	387/IRQ7	
Parallel Port Mode	SPP	

OnChip IDE Channel 1

The integrated peripheral controller contains an IDE interface with support for IDE channels. Select *Enabled* to activate the channel.

IDE Primary/Secondary Master/Slave PIO

These fields allow your system hard disk controller to work faster. Rather than have the BIOS issue a series of commands that transfer to or from the disk drive, PIO (Programmed Input/Output) allows the BIOS to communicate with the controller and CPU directly.

The system supports five modes, numbered from 0 (default) to 4, which primarily differ in timing. When Auto is selected, the BIOS will select the best available mode.

IDE Primary/Secondary Master/Slave UDMA

These fields allow your system to improve disk I/O throughput to 33Mb/sec with the Ultra DMA/33 feature. The options are *Auto* and *Disabled*.

IDE HDD Block Mode

This field allows your hard disk controller to use the fast block mode to transfer data to and from your hard disk drive.

Onboard LAN Boot ROM

This feature allows users to enable or disable the onboard LAN boot ROM. The default setting is *Disabled*

Product No.	TFT-I-Kit-001	REV. A

Page	31 / 47

Onboard FDC Controller

Select *Enabled* if your system has a floppy disk controller (FDC) installed on the motherboard and you wish to use it. If you install an add-in FDC or the system has no floppy drive, select Disabled in this field. This option allows you to select the onboard FDD port.

Onboard Serial/Parallel Port

These fields allow you to select the onboard serial and parallel ports and their addresses. The default values for these ports are:

Serial Port 1	3F8/IRQ4
Serial Port 2	2F8/IRQ3
Parallel Port	378H/IRQ7

UART Mode Select

This field determines the UART 2 mode in your computer. The default value is **Normal**. Other options include *IrDA* and *ASKIR*.

Parallel Port Mode

This field allows you to determine parallel port mode function.

SPP	Standard Printer Port
EPP	Enhanced Parallel Port
ECP	Extended Capabilities Port

Power Management Setup

The Power Management Setup allows you to save energy of your system effectively.

Phoenix - AwardBIOS CMOS Setup Utility
Power Management Setup

Power Management	Disabled	ITEM HELP
** PM Timers **		Menu Level >
Standby Mode	Disabled	
Suspend Mode	Disabled	
Power-On by Alarm	Disabled	
Time (hh:mm:ss) Alarm	0	
IRQ Wakeup Events	Press Enter	

Power Management

The options for the power management setting are **Disabled**, **Legacy** and **APM**.

PM Timers and IRQ Wakeup Events

The HDD, FDD, COM, LPT Ports, and PCI PIRQ are I/O events that can prevent the system from entering a power saving mode or can awaken the system from such a mode. When an I/O device wants to gain the attention of the operating system, it signals this by causing an IRQ to occur. When the operating system is ready to respond to the request, it interrupts itself and performs the service.

PNP/PCI Configurations

This option configures the PCI bus system. All PCI bus systems on the system use INT#, thus all installed PCI cards must be set to this value.

Phoenix - AwardBIOS CMOS Setup Utility PnP/PCI Configurations		
PNP OS Installed	No	ITEM HELP
Init Display First	PCI Slot	Menu Level
Reset Configuration Data	Disabled	
Resources Controlled By	Auto (ESCD)	Default is Disabled. Select Enabled to reset Extended System
IRQ Resources	Press Enter	Configuration Data
Memory Resources	Press Enter	ESCD) when you exit Setup if you have installed a new add-on and the system
PCI/VGA Palette Snoop	Disabled	reconfiguration has caused such a serious conflict that the OS cannot boot.

PNP OS Installed

If your OS supports Plug & Play (PnP), select **Yes** so that it can take over the management of device resources. If you are using a non-PnP-aware OS or not all of the operating systems you are using support PnP, select **No** to let the BIOS handle it instead.

Init Display First

This field refers to the primary video or primary video adapter. The default setting is **PCI Slot**.

Reset Configuration Data

This field allows you to determine whether to reset the configuration data or not. The default value is **Disabled**.

Resources Controlled by

This PnP BIOS can configure all of the boot and compatible devices automatically with the use of a use a PnP OS system such as Windows 95.

PCI/VGA Palette Snoop

Some non-standard VGA display cards may not show colors properly. This field allows you to set whether or not MPEG ISA/VESA VGA cards can work with PCI/VGA. When this field is enabled, a PCI/VGA can work with an MPEG ISA/VESA VGA card. When this field is disabled, a PCI/VGA cannot work with an MPEG ISA/VESA card.

Product No.	TFT-I-Kit-001	REV. A

Page	33 / 47
------	---------

PC Health Status

This section shows the parameters in determining the PC Health Status. These parameters include temperatures, fan speeds and voltages.

Phoenix - AwardBIOS CMOS Setup Utility		
PC Health Status		
CPU Warning Temperature	Disabled	ITEM HELP
Current System Temp.	45°C/113°F	Menu Level >
Current CPU Temp	30°C/86°F	
Vcore(V)	1.18 V	
Vmem	2.57V	
Vcc3(V)	3.39V	
+5V	5.13 V	
+12V	11.12 V	
-12V	-12.19 V	
VBAT	3.21 V	

CPU Warning Temperature

This field allows the user to set the temperature so that when the temperature is reached, the system sounds a warning. This function can help prevent damage to the system that is caused by overheating.

Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

Load Fail-Safe Defaults

This option allows you to load the troubleshooting default values permanently stored in the BIOS ROM. These default settings are non-optimal and disable all high-performance features.

Load Optimized Defaults

This option allows you to load the default values to your system configuration. These default settings are optimal and enable all high performance features.

Set Supervisor/User Password

These two options set the system password. Supervisor Password sets a password that will be used to protect the system and Setup utility. User Password sets a password that will be used exclusively on the system. To specify a password, highlight the type you want and press <Enter>. The Enter Password: message prompts on the screen. Type the password, up to eight characters in length, and press <Enter>. The system confirms your password by asking you to type it again. After setting a password, the screen automatically returns to the main screen.

To disable a password, just press the <Enter> key when you are prompted to enter the password. A message will confirm the password to be disabled. Once the password is disabled, the system will boot and you can enter Setup freely.

Save & Exit Setup

This option allows you to determine whether or not to accept the modifications. If you type "Y", you will quit the setup utility and save all changes into the CMOS memory. If you type "N", you will return to Setup utility.

Product No.	TFT-I-Kit-001	REV. A

Page	34 / 47
------	---------

Exit Without Saving

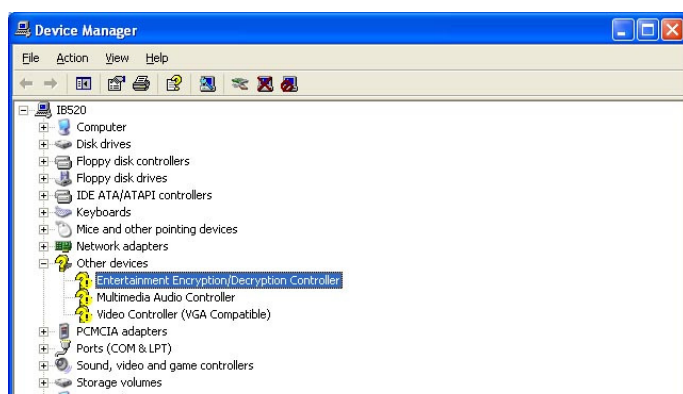
Select this option to exit the Setup utility without saving the changes you have made in this session. Typing "Y" will quit the Setup utility without saving the modifications. Typing "N" will return you to Setup utility.

4.8 Drivers Installation

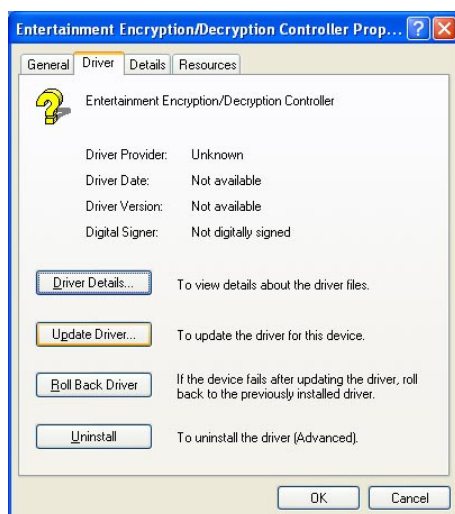
This section describes the installation procedures for software and drivers under the Windows 2000 and Windows XP. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase.

4.8.1 Entertainment Encryption/Decryption Controller Driver

1. In the Windows operating system, go to the Device Manager.
2. As shown below, click the **Entertainment Encryption/Decryption Controller** under **Other devices**.



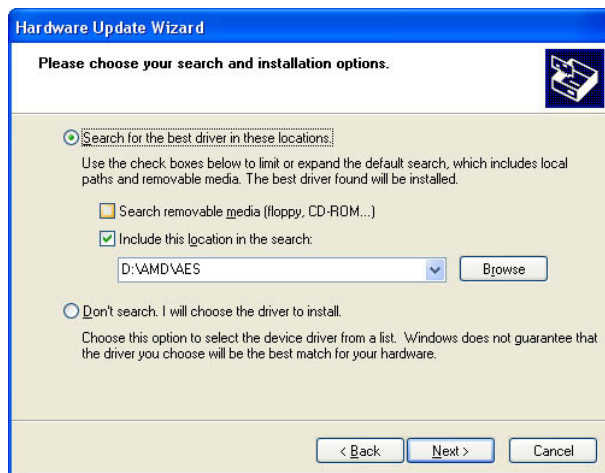
3. In the following window, click the **Driver** tab and click **OK** to continue.



Product No.	TFT-I-Kit-001	REV. A

Page	35 / 47
------	---------

4. In the Hardware Update Wizard, select **No, not this time** and click **Next** to continue. Then select **Install from a list of specific location (Advanced)**. Click **Browse** to find the driver's path in the CD provided - **\AMD\AES**. Then, click **Next** to start the drivers installation. Then click **Finish** after the wizard has finished installing the software for **Geode LX AES Crypto Driver**.

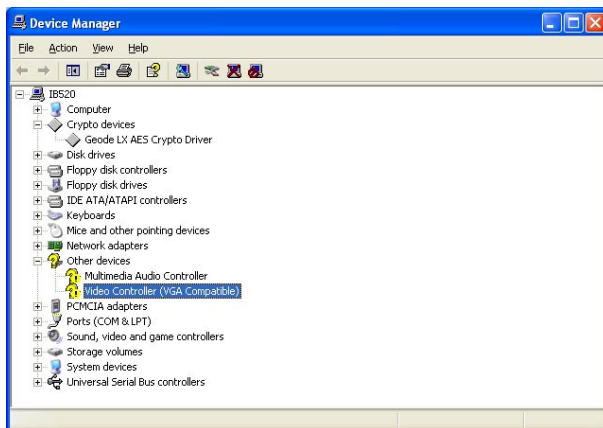


Product No.	TFT-I-Kit-001	REV. A

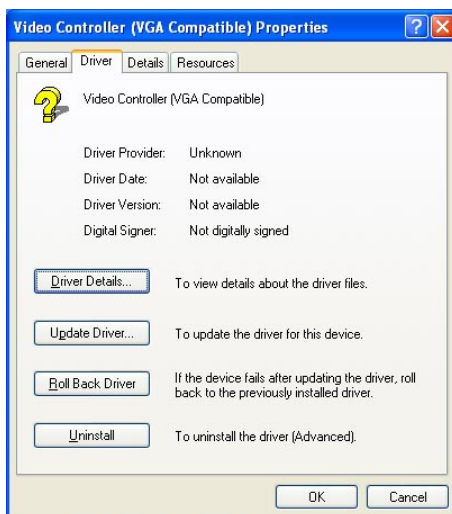
Page	36 / 47
------	---------

4.8.2 VGA Drivers Installation

1. In the Windows operating system, go to the Device Manager.
2. As shown below, click the **Video Controller (VGA Compatible)** under **Other devices**.



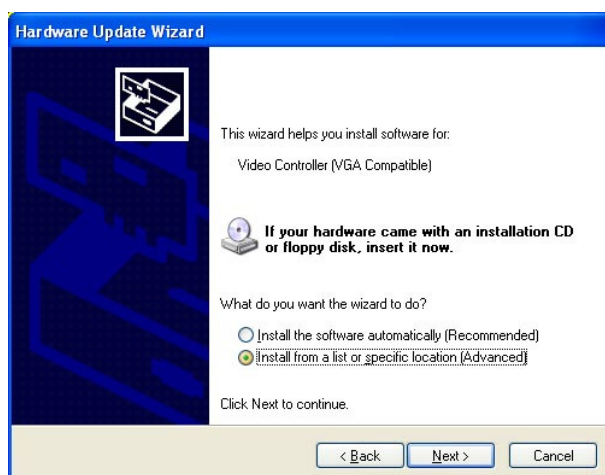
3. In the following window, click the **Driver** tab and click **OK** to continue.



Product No.	TFT-I-Kit-001	REV. A

Page	37 / 47
------	---------

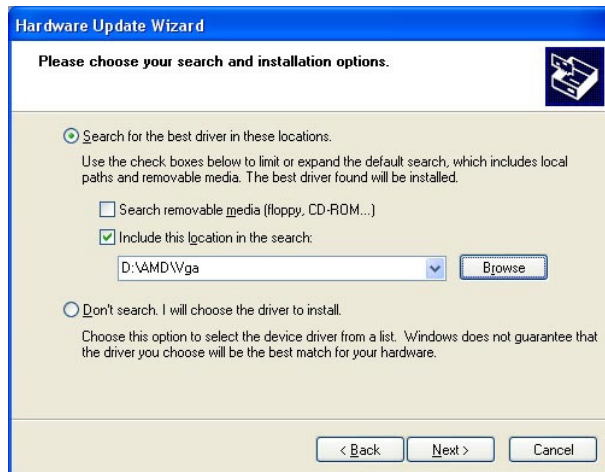
4. In the Hardware Update Wizard, select **No, not this time** and click **Next** to continue. Then select **Install from a list of specific location (Advanced)**.



Product No.	TFT-I-Kit-001	REV. A

Page	38 / 47
------	---------

5. In the next screen, click **Search for the best driver in these locations**. Check **Include this location in the search**. Click **Browse** to find the driver's path in the CD provided or enter the path directly - **\AMD\Vga**. Then, click **Next** to start the drivers installation. Then click **Finish** after the wizard has finished installing the software for **Advanced Micro Devices Win XP Graphics Driver**.

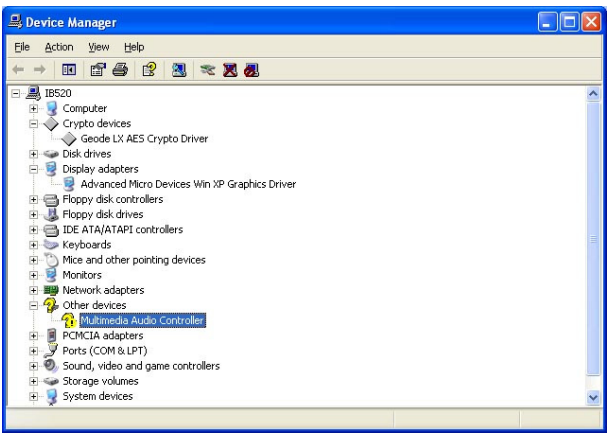


Product No.	TFT-I-Kit-001	REV. A

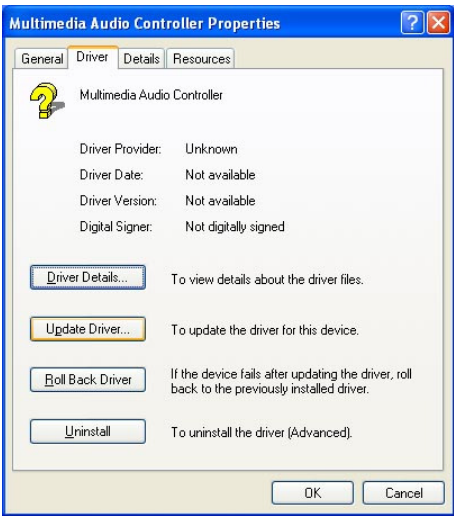
Page	39 / 47
------	---------

4.8.3 **Audio Driver Installation**

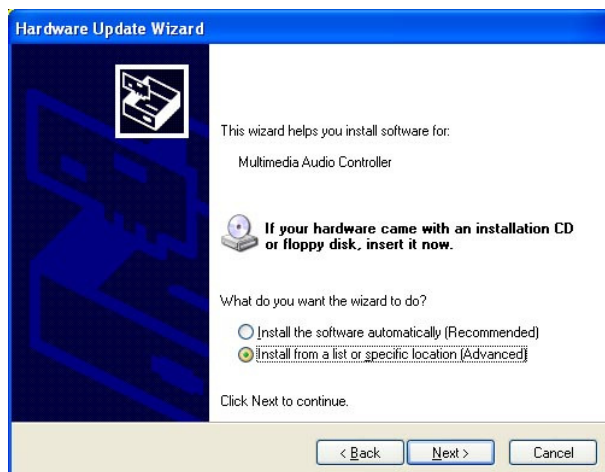
- 1. In the Windows operating system, go to the Device Manager.
- 2. As shown below, click the **Multimedia Audio Controller** under **Other devices**.



- 3. In the following window, click the **Driver** tab and click **OK** to continue.



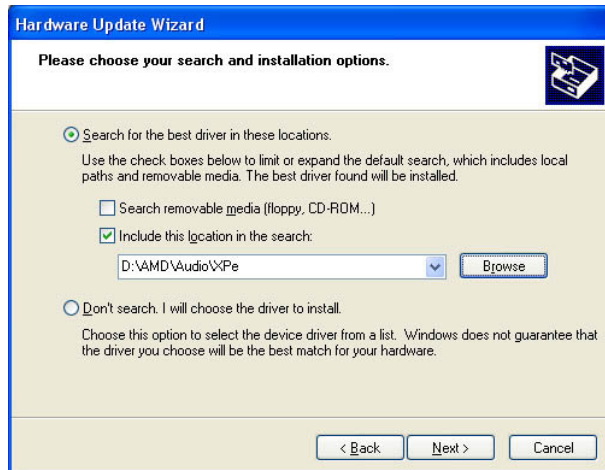
4. In the Hardware Update Wizard, select **No, not this time** and click **Next** to continue. Then select **Install from a list of specific location (Advanced)**.



Product No.	TFT-I-Kit-001	REV. A

Page	41 / 47
------	---------

5. In the next screen, click **Search for the best driver in these locations**. Check **Include this location in the search**. Click **Browse** to find the driver's path in the CD provided or enter the path directly - **\\AMD\\Audio\\XPe**. Then, click **Next** to start the drivers installation. Then click **Finish** after the wizard has finished installing the software for **GeodeLX Audio Driver (WDM)**.



Product No.	TFT-I-Kit-001	REV. A

Page	42 / 47
------	---------

Appendices

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h	Keyboard Controller (1)
0601h	Control Port
064h	Real Time Clock
070h - 07Fh	Keyboard Controller (2)
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h - 00FFh	Coprocessor
01F0h - 01F7h 03F6h	IDE (Primary)
02F8h - 02FFh	Serial Port #2(COM2)
0378h - 037Ah	Parallel Port #1(LPT1)
03C0h - 03DFh	Reserved for VGA
03F0h - 03F5h 03F7h	FDD Controller
03F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	PIC2 (IRQ8-15)
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	For PCI
IRQ6	Floppy Disk Controller
IRQ7	Parallel Port #1
IRQ8	Real Time Clock
IRQ9	For PCI
IRQ10	For PCI
IRQ11	For PCI
IRQ12	PS/2 Mouse
IRQ13	Coprocessor
IRQ14	Primary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sort of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

This code and information is provided "as is" without warranty of any kind, either expressed or implied, including but not limited to the implied warranties of merchantability and/or fitness for a particular purpose.

```

;[]=====
; Name : Enable_And_Set_Watchdog
; IN    : AL - 1sec ~ 255sec
; OUT   : None
;[]=====
Enable_And_Set_Watchdog      Proc      Near
    push    ax                ;save time interval
    call    Unlock_Chip

    mov     cl, 2Bh
    call    Read_Reg
    and     al, NOT 10h
    call    Write_Reg         ;set GP24 as WDTO

    mov     cl, 07h
    mov     al, 08h
    call    Write_Reg         ;switch to LD8
    mov     cl, 0F5h
    call    Read_Reg
    and     al, NOT 08h
    call    Write_Reg         ;set count mode as second

    pop     ax
    mov     cl, 0F6h
    call    Write_Reg         ;set watchdog timer

    mov     al, 01h
    mov     cl, 30h
    call    Write_Reg         ;watchdog enabled

```

Product No.	TFT-I-Kit-001	REV. A

Page	45 / 47
------	---------

```

        call    Lock_Chip
        ret
Enable_And_Set_Watchdog      Endp

;[=====
; Name  : Disable_Watchdog
; IN    : None
; OUT   : None
;[=====
Disable_Watchdog      Proc    Near
        call    Unlock_Chip

        mov     cl, 07h
        mov     al, 08h
        call    Write_Reg          ;switch to LD8

        xor     al, al
        mov     cl, 0F6h
        call    Write_Reg          ;clear watchdog timer

        xor     al, al
        mov     cl, 30h
        call    Write_Reg          ;watchdog disabled

        call    Lock_Chip
        ret
Disable_Watchdog      Endp
;[=====
; Name  : Unlock_Chip
; IN    : None
; OUT   : None
;[=====
Unlock_Chip      Proc    Near
        mov     dx, 4Eh
        mov     al, 87h
        out     dx, al
        out     dx, al
        ret
Unlock_Chip      Endp
;[=====
; Name  : Lock_Chip
; IN    : None
; OUT   : None

```

```

;[=====
Unlock_Chip      Proc      Near
                  mov      dx, 4Eh
                  mov      al, 0Aah

                  out      dx, al
                  ret
Unlock_Chip      Endp
;[=====
; Name : Write_Reg
; IN      : CL - register index
;          : AL - Value to write
; OUT     : None
;[=====
Write_Reg        Proc      Near
                  push     ax
                  mov      dx, 4Eh
                  mov      al, cl
                  out      dx, al
                  pop      ax
                  inc      dx
                  out      dx, al
                  ret
Write_Reg        Endp
;[=====
; Name : Read_Reg
; IN      : CL - register index
; OUT     : AL - Value to read
;[=====
Read_Reg         Proc      Near
                  mov      al, cl
                  mov      dx, 4Eh
                  out      dx, al
                  inc      dx
                  in       al, dx
                  ret
Read_Reg         Endp
;[=====

```

5 Technical support

For technical support, please contact us at sales@densitron.co.uk or visit our website: www.densitron.co.uk.

Product No.	TFT-I-Kit-001	REV. A

Page	47 / 47
------	---------