OLED DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-25664BE-1A**	
CUSTOMER APPROVAL		**Date**

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bruno Recaldini	**Anthony Perkins**	**Bazile Peter**
Date: 11 August 2006		

☐ **Approval for Specification only**

☐ **Approval for Specification and Sample**

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REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	03-Feb-06	--	--	Initial DCA Release	E3004
B	22-Mar-06	5		Remove pin out details from Drawing	
C	11-Aug-06	8 19	3.2 7.2.1	Addition of current consumption Removed AQL refernces	

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1 MAIN FEATURES

ITEM	CONTENTS
Display Format	256 x 64 Dots
Colour	Blue Monochrome
Overall Dimensions	88.00 (W) × 27.80 (H) × 2.20 (D) mm
Viewing Area	78.78 (W) x 21.18 (H) mm
Screen Size	3.12”
Mode	Passive Matrix, with 16 grey scales
Duty ratio	1/64
Driver IC	STV8105
Operating temperature	-20°C ~ +70°C
Storage temperature	-30°C ~ +80°C

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2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	256 x 64 Dots	
Overall Dimensions	88.00 (W) × 27.80 (H) × 2.20 (D)	mm
Viewing Area	78.78 (W) x 21.18 (H) mm	mm
Active Area	76.78 (W) x 19.18 (H)	mm
Dot Size	0.28 (W) 0.28 (H)	mm
Dot Pitch	0.30 (W) x 0.30 (H)	mm
Weight	9.6	g
IC Controller/Driver	STV8105	

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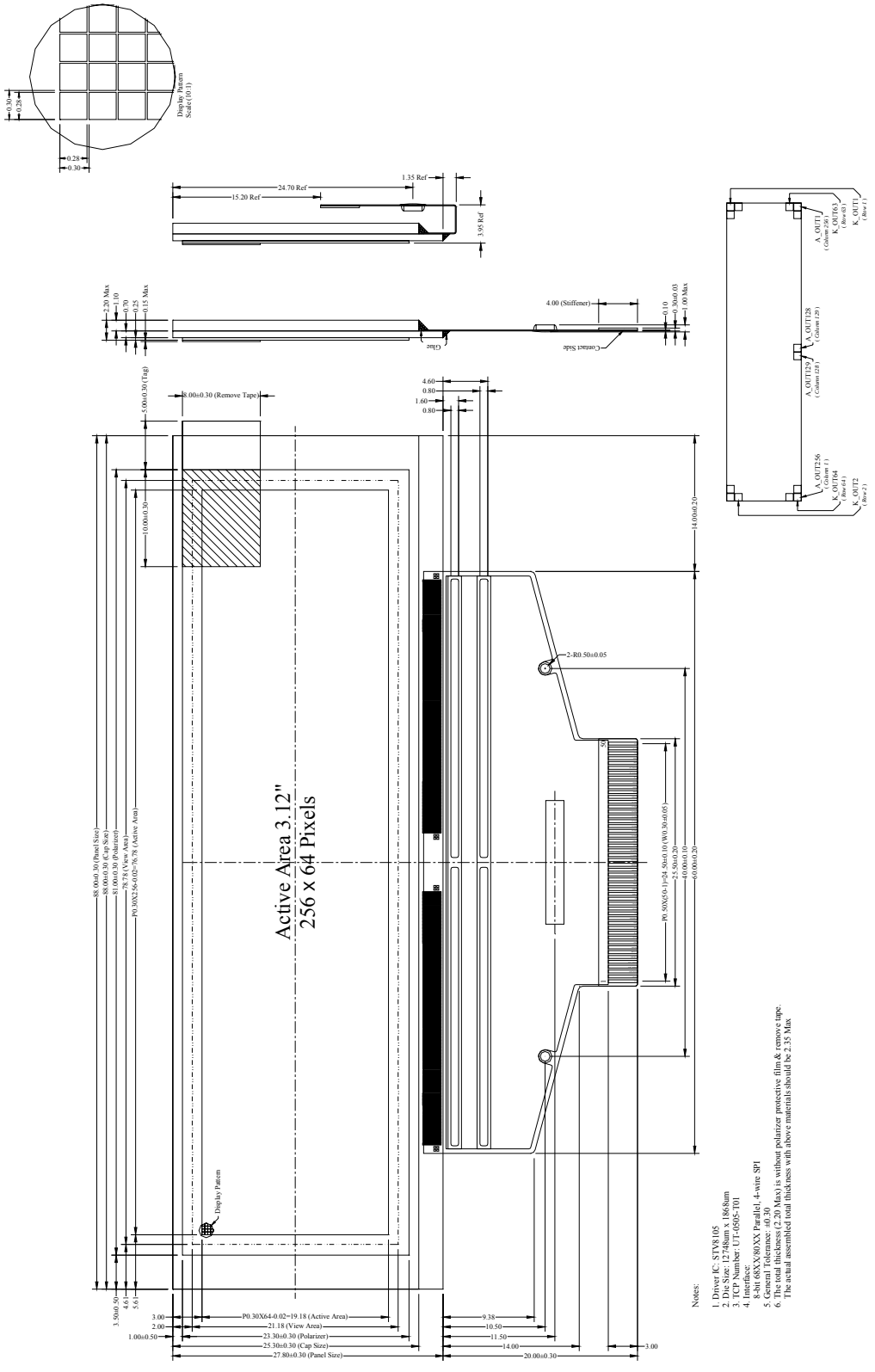
2.2 MECHANICAL DRAWING



Product No.	DD-25664BE-1A	REV. C

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3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Supply Voltage	V_{DD}	-0.3	4.6	V	1, 2
DC/DC Supply Voltage	V_{DC}	-0.3	12	V	1, 2
Driver Supply Voltage	V_{PP}	-0.3	27	V	1, 2
Program Voltage	V_{PRG}	-0.3	20	V	1, 2
Operating Temperature	Top	-20	+70	°C	
Storage Temperature	Tst	-30	+80	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3.2 "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3.2 ELECTRICAL CHARACTERISTICS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	Ta = 25°C	3.0	3.3	3.6	V
DC/DC Supply Voltage	V_{DC}	Ta = 25°C	3.0	5.0	10.0	V
Driver Supply Voltage	V_{PP}	Ta = 25°C	13	14	15	V
Program Voltage	V_{PRG}	Ta = 25°C	14	--	18	V
High Level Input	V_{IH}	Logic	$0.8xV_{DD}$	--	--	V
Low Level Input	V_{IL}	Logic	--	--	$0.2xV_{DD}$	V

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3.3 INTERFACE PIN ASSIGNMENT

No.	Symbol	I/O	Function
1	N.C.	--	*Reserved Pin (Supporting Pin).* The supporting pins can reduce the influences from stresses on the function pins.
2	VROWOFF2	I	*Power Supply for Odd (1) & Even (2) Row Driver.* These are the constant voltage supply pins. When display is not active, the row output pins are pulled-up to the voltage supplied on the two pins. They are supplied externally.
3	SCLKOUT	O	*System Clock Output.* This pin is outputted to slave device and/or the specified row driver. It should be left open individually.
4	VSYNCOUT	O	*Vertical/Horizontal SYNC Input/Output.* The "VSYNC" and "HSYNC" pins, both inputs and outputs, are connected for synchronous operation. These should be left open individually.
5	HSYNCOUT	O	
6	VSENSE	I	*Feedback Signal* This pin is the feedback signal for voltage regulation loop. It is used to adjust the booster output voltage level (VPP). In case of VSENSE feedback disconnection the Driver is switched off.
7	VCOMP	I/O	*Compensation Pin* The output of the amplifier VCOMP is externally available for compensation. It is necessary when the DC/DC converter works in PWM constant frequency mode. PFM constant ton mode does not need a compensation network.
8	ISENSE	I	*Over Current Sense Signal for External Switching FET* This pin is the feedback signal for current sense. It is used for over current protection on the external FET.
9	VDC	I	*Power Supply for Gate Drive Output Buffer* This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be floated when the converter is not used.
10	VDRIVE	O	*Gate Drive Signal for External Switching FET* This output pin drives the gate of external power FET.
11	VSS	I	*Ground* It also acts as the reference for the logic pins. It must be connected to external ground.
12	VPRG	I	*Power Supply for Non-Volatile OTP Memory Programming* This is the NVM programming voltage supply pin. It is supplied externally.
13	VPP2	I	*Power Supply for Odd (1) & Even (2) Column Driver* These are the constant current supply pins. They are supplied externally.
14	VHSENSE	I	*VPP Sense Input* This pin is the feedback signal for voltage regulation loop. It is used to adjust the booster output voltage level (VPP). In case of VHSENSE feedback disconnection, VPP voltage rises up to the value fixed by the external resistor divider.

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No.	Symbol	I/O	Function
15	VPP1	I	*Power Supply for Odd (1) & Even (2) Column Driver* These are the constant current supply pins They are supplied externally.
16	VCOLPRE2	I	*Power Supply for Odd (1) & Even (2) Column Pre-Charge* These are the constant voltage supply pins. They are supplied externally.
17	VCOLPRE1	I	
18	VFDET	I/O	*Pin for VF Detection* This pin is the detection of voltage difference between C1 and C256.
19	VREF2	I/O	*Reference Voltage* These are the current reference pins. It is possible to set two different reference current values for the odd (1) and even (2) outputs by connecting two different resistor values. With input CMODE, it is also to use only the reference current established on pin VREF1. These are supplied externally.
20	VREF1	I/O	
21	VDD	I	*Power Supply for Logic Circuit* This is the voltage supply pins. It must be connected to external source.
22	VSS	I	*Ground* It also acts as the reference for the logic pins. It must be connected to external ground.
23	P/S	I	*Communicating Protocol Select* This pin is MCU interface selection input. The parallel interface is active when P/S is high; the serial interface activates when P/S is low.
24	TON/F	I	*DC/DC Converter Mode Select* This pin is the control schemes selection input of the embedded booster circuit. The DC/DC converter works in PFM constant ton mode while it is connected to VDD. The DC/DC converter works in PWM constant frequency mode while it is connected to ground.
25	CMODE	I	*Color Mode Select* This pin is the display colors selection input. It corresponds to "Two" color display panel. A setup of another output current value is possible for an odd number pin and the even number pins of each with two reference current.
26	SELCLK	I	*Internal/External System Clock Source Select* This pin is internal clock enable. When this pin is pulled high, an internal oscillation stable circuit is used. The internal clock will be disabled when it is pulled low, an external clock source must be connected for normal operation.
27	MSEL[1]	I	*Primary/Secondary Select* This pin is the Primary/Secondary selection input. The function is synchronous operation, which is the direction of the cathode. This pin must be pulled high to enable the chip function as primary.
28	MSEL[0]	I	*Master/Slave Select* This pin is the Master/Slave selection input. The function is synchronous operation, which is the direction of the anode. This pin must be pulled high to enable the chip function as master.

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No.	Symbol	I/O	Function
29	VDD	I	*Power Supply for Logic Circuit* This is the voltage supply pins. It must be connected to external source.
30	RST	I	*Power Reset for Controller and Driver* This pin is reset signal input. When the pin is low, initialization of the chip is executed.
31	DIN[7]	I	*Host Data Input Bus* These pins are 8-bit parallel bus to be connected to the microprocessor's data bus. When serial mode is selected, DIN[7] will be the serial data input (SIN) and DIN[6] will be the serial clock input (SCLI).
32	DIN[6]	I	
33	DIN[5]	I	
34	DIN[4]	I	
35	DIN[3]	I	
36	DIN[2]	I	
37	DIN[1]	I	
38	DIN[0]	I	
39	SD/C	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the data at DIN[7]~DIN[0] is treated as display data. When the pin is pulled low, the data at DIN[7]~DIN[0] will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
40	WR	I	*Write Pulse* This pin is MCU interface input. Data write operation is initiated when this pin is pulled low and the chip is selected.
41	CS1	I	*Chip Select* The two pins are the chip select input. The CS1 is activated for Primary/Secondary Master devices. The CS2 is activated for Primary/Secondary Slave devices.
42	CS2	I	
43	VSS	I	*Ground* It also acts as the reference for the logic pins. It must be connected to external ground.
44	VSYNCIN	I	*Vertical/Horizontal SYNC Input/Output.* The "VSYNC" and "HSYNC" pins, both inputs and outputs, are connected for synchronous operation. These should be left open individually.
45	HSYNCIN	I	

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No.	Symbol	I/O	Function
46	CLKIN	I	*External System Clock Source* This pin is activated for the external RC/Crystal connection or Clock input.
47	ROSC	O	*External System Clock Source* This pin is activated for the external RC oscillator or Crystal oscillation. A resistor would be connected.
48	COSC	O	*External System Clock Source* This pin is activated for the external RC oscillator. A capacitor would be connected.
49	VROWOFF1	I	*Power Supply for Odd (1) & Even (2) Row Driver.* These are the constant voltage supply pins. When display is not active, the row output pins are pulled-up to the voltage supplied on the two pins. They are supplied externally.
50	N.C.	--	*Reserved Pin (Supporting Pin).* The supporting pins can reduce the influences from stresses on the function pins.

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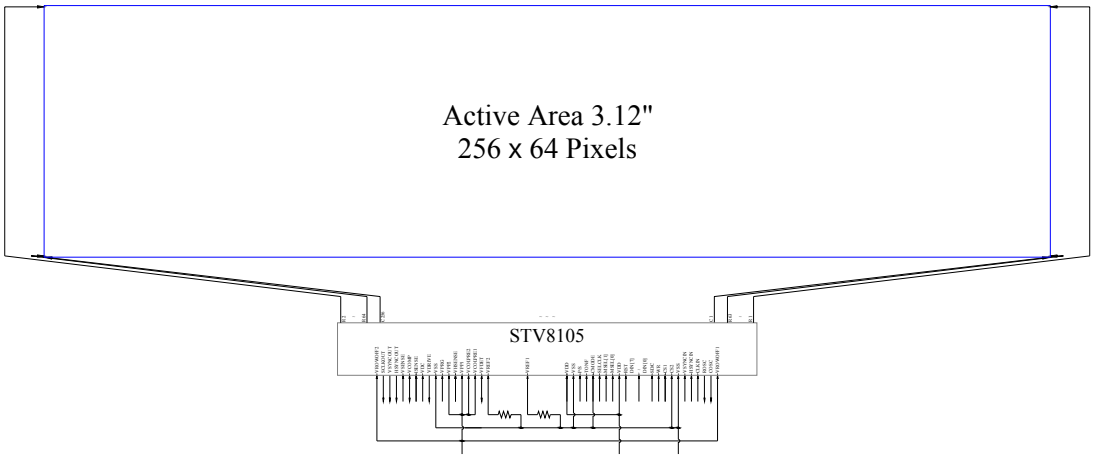
3.4 BLOCK DIAGRAM



MCU Interface Selection: P/S
Pins connected to MCU interface:
RST, DIN[7]~DIN[0], SD/C, WR, and CS1

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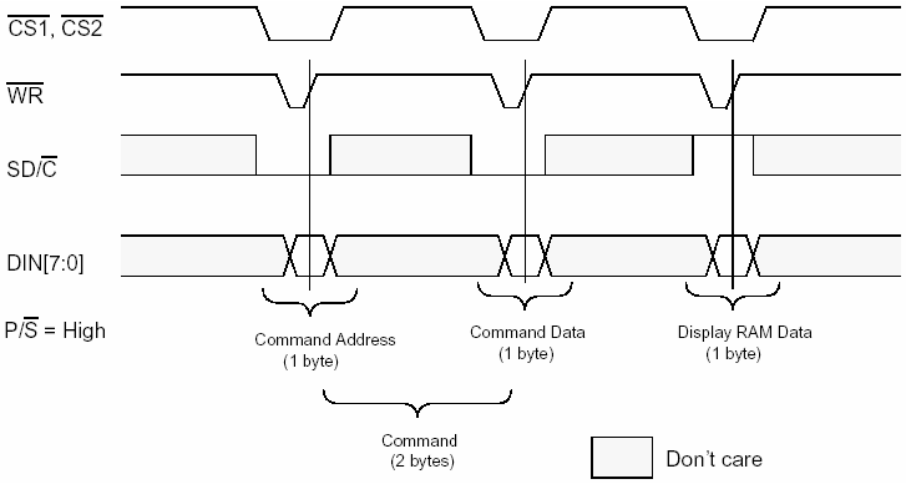
3.5 TIMING CHARACTERISTICS

3.5.1 4.2.1 Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
T_{ah}	Address Hold Time	10	-	ns
T_{aw}	Address Setup Time	0	-	ns
T_{cyc}	System Cycle Time	200	-	ns
T_{ds}	Data Setup Time	60	-	ns
T_{dh}	Data Hold Time	10	-	ns
T_{cclw}	Write Pulse Width	60	-	ns

* All the timings should be based on 30% and 70% of V_{DD}-GND.



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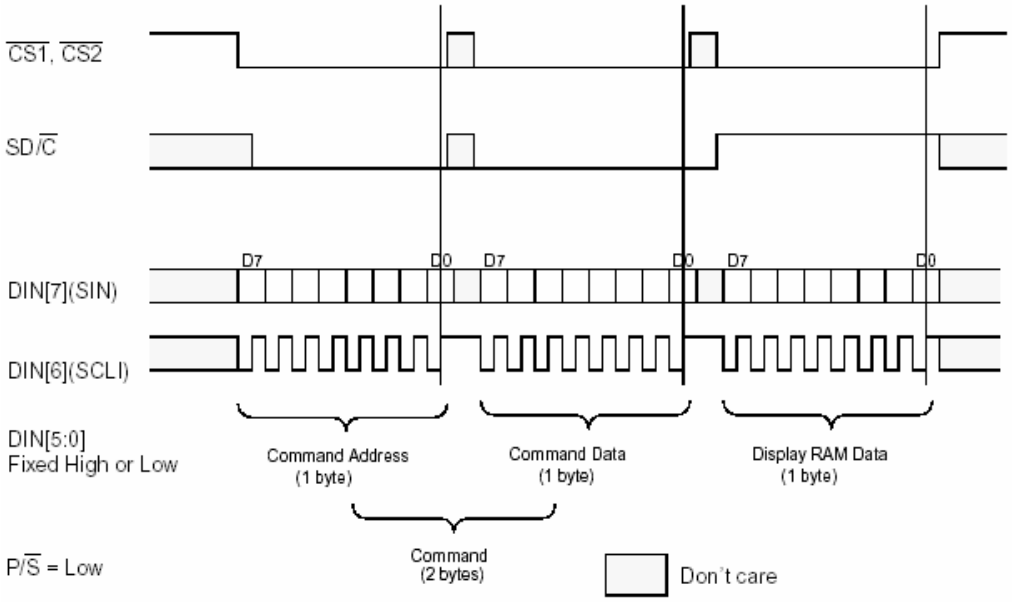
3.5.2 4.2.2 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
T_{scyc}	Serial Clock Cycle Time	200	-	ns
T_{sas}	Address Setup Time	20	-	ns
T_{sah}	Address Hold Time	20	-	ns
T_{css}	Chip Select Setup Time	20	-	ns
T_{csh}	Chip Select Hold Time	20	-	ns
T_{sds}	Data Setup Time	20	-	ns
T_{sdh}	Data Hold Time	20	-	ns
T_{slw}	Pulse Width (Low)	90	-	ns
T_{shw}	Pulse Width (High)	90	-	ns

* All the timings should be based on 30% and 70% of V_{DD}-GND.



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4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Ta = 25 °C

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer	60	80	-	cd/m^2
C.I.E. (Blue)	(x) (y)	Without Polarizer	0.12 0.22	0.16 0.26	0.20 0.30	
Dark Room Contrast	CR		-	>1:100	-	
View Angle			>160	-	-	degree

Note 3: Optical measurement taken at 1/64 duty, 100Hz Frame Rate, 7Fh Luminance Adjustment Setting.

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5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

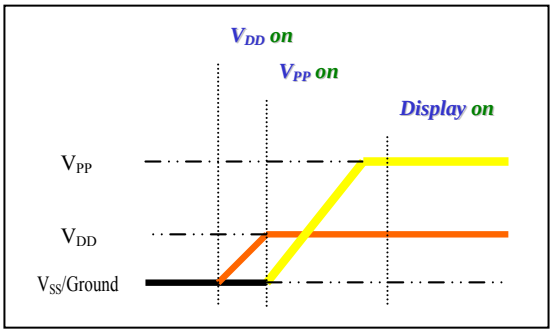
Refer to the Technical Manual for the STV8105.

5.2 POWER DOWN AND UP SEQUENCE

To protect the panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

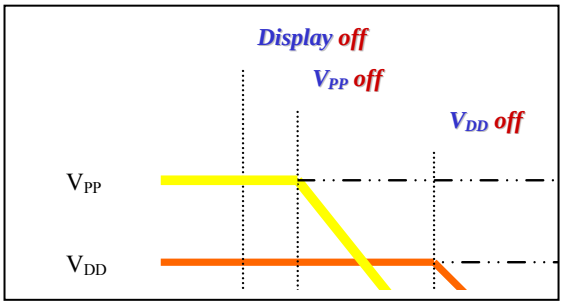
5.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Clear Screen
4. Power up V_{PP}
5. Delay 100ms (when V_{DD} is stable)
6. Send Display on command



5.2.2 Power down Sequence:

1. Send Display off command
2. Power down VPP
3. Delay 100ms (when VPP is reach 0 and panel is completely discharges)
4. Power down VDD



5.3 RESET CIRCUIT

At the time of RST signal input…

Oscillator:	Off
DC/DC Converter:	Off
Column & Row Driver:	V_{SS}
All Registers:	Default Value

At the time of RST signal release or software reset completion (200ns maximum after F2h command sending)…

Oscillator:	On
DC/DC Converter:	Off (Waiting for a Command)
Column & Row Driver:	V_{SS} (Waiting for a Command)
All Registers:	Default Value (Waiting for a Command)

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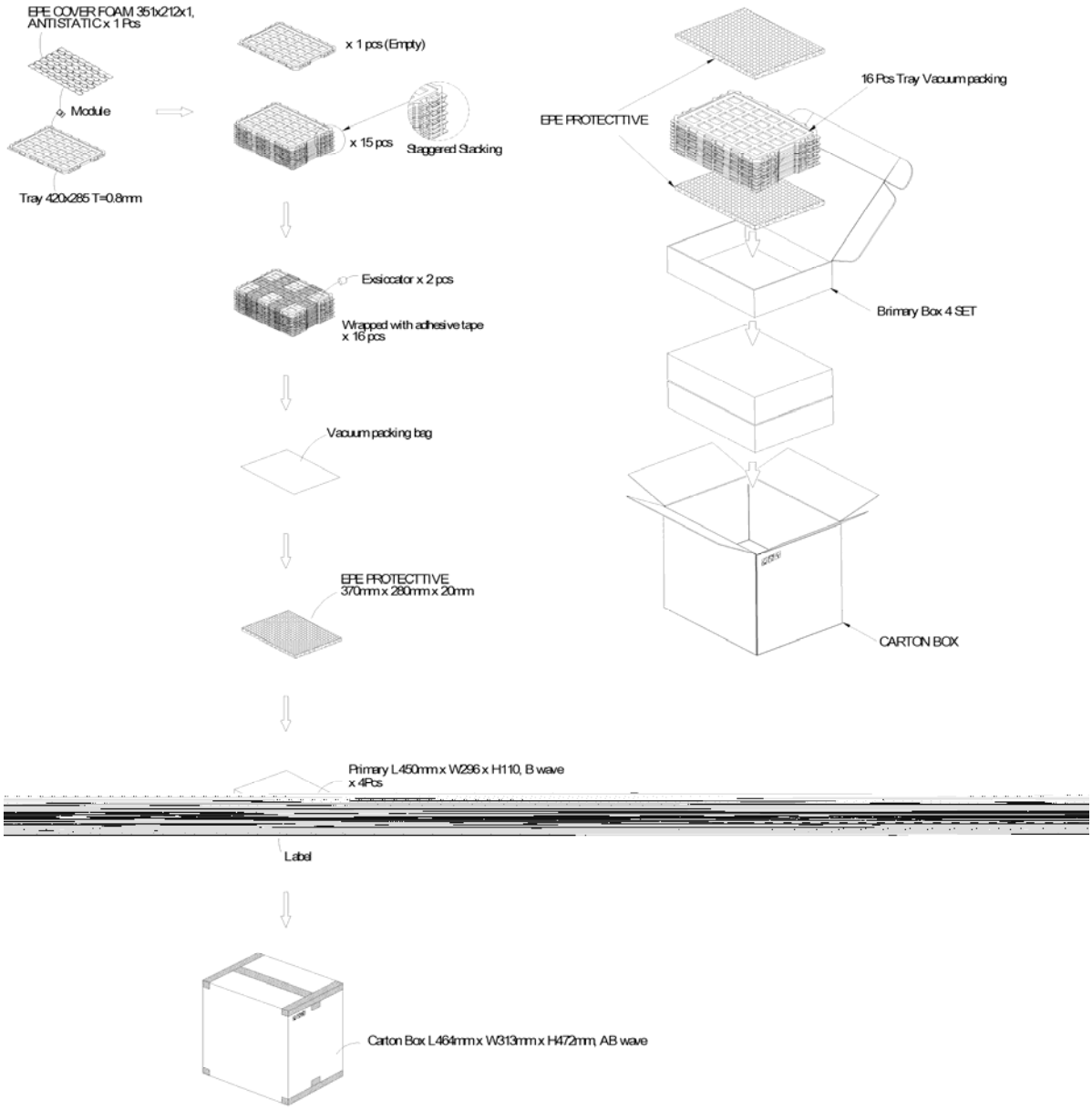
6 PACKAGING AND LABELLING SPECIFICATION

6.1 PACKAGING



6.2 LABELLING & MARKING

DENSITRON DD-25664BE-1A TW YYMM

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7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

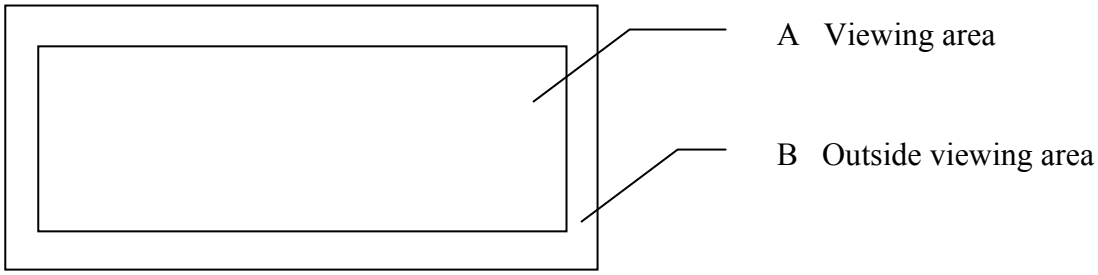
The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

7.2.1 Delivery inspection standards

- IPC-AA610 rev. C, class 2 electronic assemblies standard

7.2.2 Zone definition



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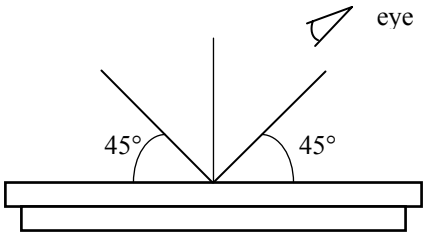
7.2.3 Visual inspection

- Inspect under 30W fluorescent lamp leaving 50 cm between the module and the lamp and 30 cm between the module and the eye (measuring position).
- Appearance is inspected at the best contrast voltage (best contrast is adjusted considering clearness and crosstalk on screen).
- Inspect the module at 45° right and left, top and bottom.
- Use the optimum viewing angle during the contrast inspection.



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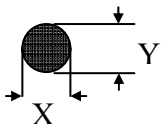
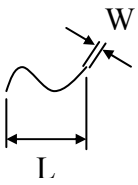
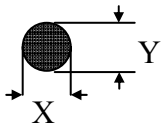
7.2.3.1 Standard of appearance inspection

Units: mm

<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td rowspan="2">Packing & Label</td><td>Outside & inside package | Presence of product no., lot no., quantity</td></tr>
<tr><td>Critical</td><td>Product must not be mixed with others and quantity must not be different from that indicated on the label</td></tr>
<tr><td>Major</td><td>Dimension</td><td>Product dimensions must be according to specification and drawing</td></tr>
<tr><td>Major</td><td>Electrical</td><td>Product electrical characteristics must be according to specification</td></tr>
<tr><td>Critical</td><td>LCD Display</td><td>Missing lines or wrong patterns on LCD display are not allowed</td></tr>
<tr><td>Minor</td><td>Black spot, white spot, dust</td><td>Round type: as per following drawing
∅ = (X+Y)/2
 

<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>0.1<∅<0.2</td><td>3</td></tr><tr><td>0.2<∅<0.25</td><td>1</td></tr><tr><td>0.25<∅</td><td>0</td></tr></table>
Line type: as per following drawing
 

<table><tr><th colspan="4">Acceptable quantity</th></tr><tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr><tr><td>- -</td><td>W≤0.05</td><td>Any number</td><td rowspan="3">Any number</td></tr><tr><td>L≤2.0</td><td>W≤0.1</td><td>3</td></tr><tr><td>L>2.0</td><td></td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
<tr><td>Minor</td><td>Polariser scratch</td><td>Scratch on protective film is permitted
Scratch on polariser: same as No. 1</td></tr>
<tr><td>Minor</td><td>Polariser bubble</td><td>∅ = (X+Y)/2
 

<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.5</td><td>Any number</td><td rowspan="2">Any number</td></tr><tr><td>∅>0.5</td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
</table>

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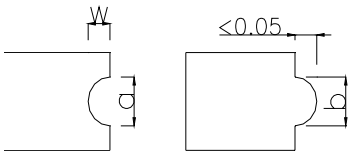
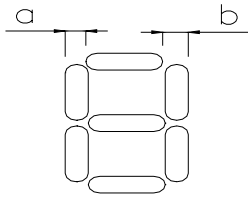
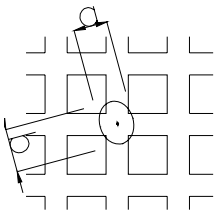
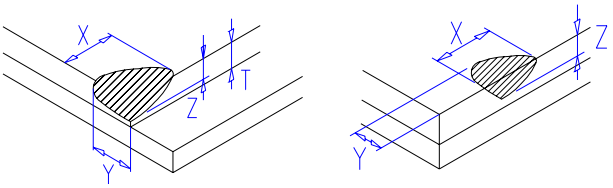
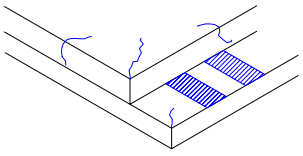
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Segment deformation</td><td>1b. Pin hole on dot matrix display
 

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>a,b<0.1</td><td>Any number</td></tr>
<tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr>
<tr><td>0.5<∅<1.0</td><td>3</td></tr>
</table>
Total acceptable quantity: 7

2. Segments / dots with different width
 

<table>
<tr><td colspan="2">Acceptable</td></tr>
<tr><td>a≥b</td><td>a/b≤4/3</td></tr>
<tr><td>a<b</td><td>a/b>4/3</td></tr>
</table>

3. Alignment layer defect
∅ = (a+b)/2
 

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>∅≤0.4</td><td>Any number</td></tr>
<tr><td>0.4<∅≤1.0</td><td>5</td></tr>
<tr><td>1.0<∅≤1.5</td><td>3</td></tr>
<tr><td>1.5<∅≤2.0</td><td>2</td></tr>
</table>
Total acceptable quantity: 7</td></tr>
<tr><td>Minor</td><td>Panel Chipping</td><td>X ≤ 1/6 Panel length
Y ≤ 1
Z ≤ T
 
</td></tr>
<tr><td>Minor</td><td>Panel Cracking</td><td>Cracks not allowed
  </td></tr>
<tr><td>Minor</td><td>Cupper exposed (pin or film)</td><td>Not allowed if visible by eye inspection</td></tr>
<tr><td>Minor</td><td>Film or Trace Damage</td><td>Not allowed if affects electrical function</td></tr>
</table>

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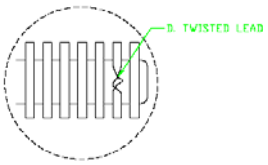
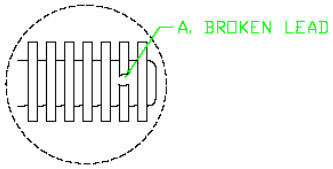
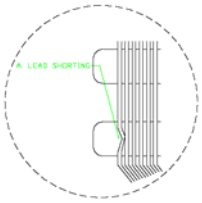
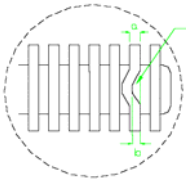
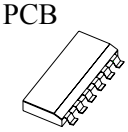
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Contact
Lead Twist</td><td>Not allowed
  </td></tr>
<tr><td>Minor</td><td>Contact
Lead
Broken</td><td>Not allowed
  </td></tr>
<tr><td rowspan="2">Minor</td><td rowspan="2">Contact
Lead Bent</td><td>Not allowed if
bent lead causes
short circuit
  </td></tr>
<tr><td>Not allowed if bent lead
extends horizontally
more than 50%
of its width
  </td></tr>
<tr><td>Minor</td><td>Colour
uniformity</td><td>Level of sample for approval set as limit sample</td></tr>
<tr><td>Major</td><td rowspan="4">PCB
  </td><td>No unmelted solder paste should be present on PCB</td></tr>
<tr><td>Critical</td><td>Cold solder joints, missing solder connections, or oxidation are not allowed</td></tr>
<tr><td>Minor</td><td>No residue or solder balls on PCB are allowed</td></tr>
<tr><td>Critical</td><td>Short circuits on components are not allowed</td></tr>
<tr><td>Minor</td><td>Tray
particles</td><td>
<table>
<tr><th></th><th>Size</th><th>Quantity</th></tr>
<tr><td rowspan="2">On tray</td><td>∅<0.2</td><td>Any number</td></tr>
<tr><td>∅>0.25</td><td>4</td></tr>
<tr><td rowspan="2">On display</td><td>∅≥0.25</td><td>2</td></tr>
<tr><td>L = 3</td><td>1</td></tr>
</table>
</td></tr>
</table>

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7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

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8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	85°C, 500 hrs	The brightness should be greater than 50% of the initial brightness. The operational functions work.
Low Temperature Operation	-30°C, 500 hrs	
High Temperature Storage	90°C, 500 hrs	
Low Temperature Storage	-40°C, 500 hrs	
High Temperature & High Humidity Storage	60°C, 90% RH, 500 hrs	
Thermal Shock Storage	-40°C ↔85°C, 100 cycles 30 min. dwell	

- All operation tests are conducted in all display on pattern.
- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C□55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration within 15,000 hours under ordinary operating and storage conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

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9 HANDLING PRECAUTIONS

Safety
If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes.
If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design
Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning
Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge
As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS}. Do not input any signals before power is turned on.
Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging
Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.
To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation
It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions
When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

Storage
Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH.
Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).

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