OLED DISPLAY MODULE

Product Specification

CUSTOMER	**Standard**	
PRODUCT NUMBER	**DD-12833BE-1A**	
CUSTOMER APPROVAL		**Date**

INTERNAL APPROVALS		
Product Mgr	Doc. Control	Electr. Eng
Bruno Recaldini	**Anthony Perkins**	**Andrea Pibiri**
Date: 01 Feb. 06	Date: 01 Feb. 06	Date: 18 Jan 06

☐ **Approval for Specification only**

☐ **Approval for Specification and Sample**

Sample no.: Date: ISIR no.:

TABLE OF CONTENTS

REVISION RECORD

Rev.	Date	Page	Chapt.	Comment	ECR no.
A	17 Jan 06			First issue	

1 MAIN FEATURES

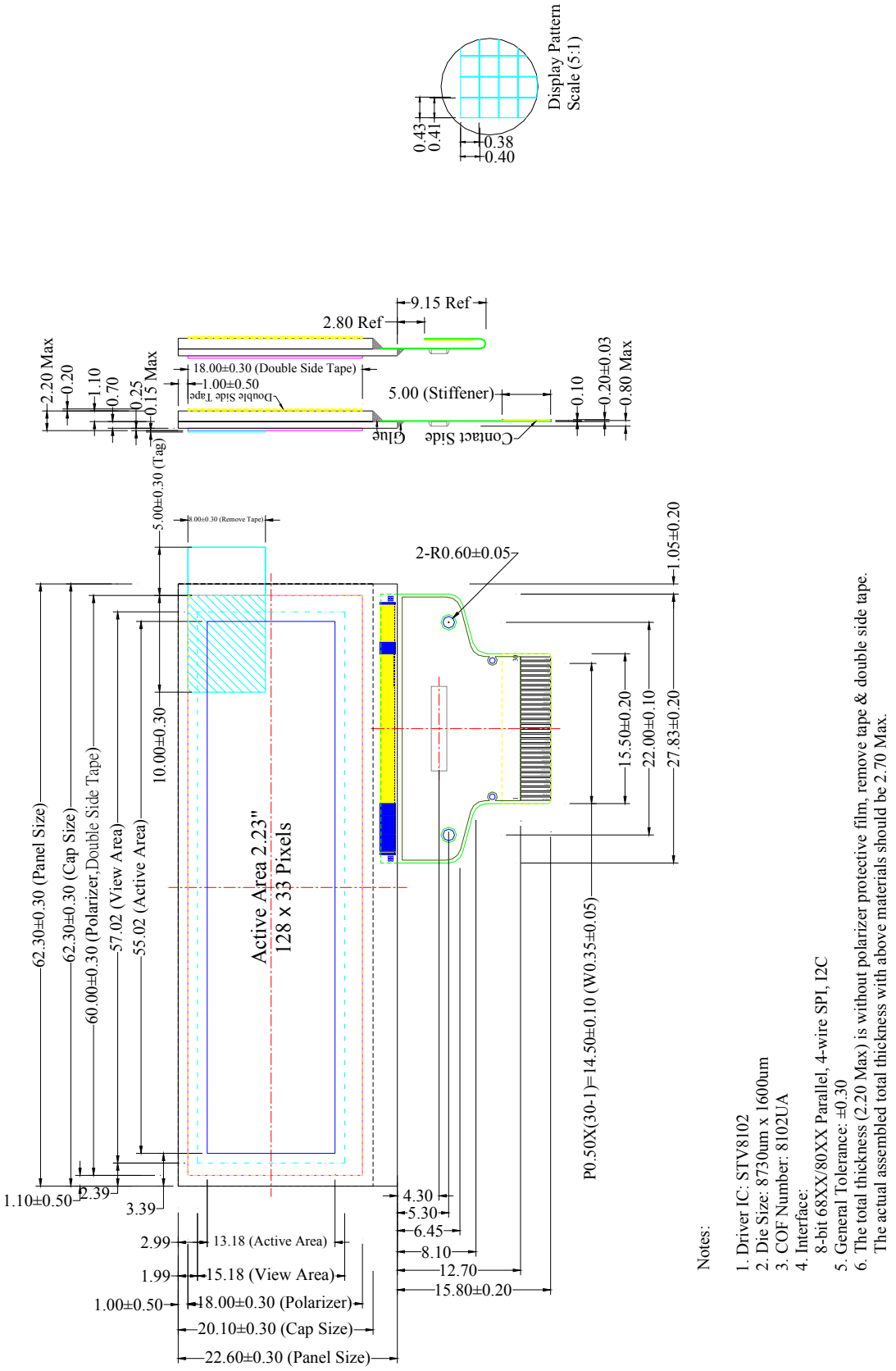
ITEM	CONTENTS
Display Format	128 x 33 dots
Colour	Blue Monochrome
Overall Dimensions	62.30 x 22.60 x 2.20 mm
Viewing Area	57.02 x 15.18 mm
Screen Size	2.23”
Mode	Passive Matrix
Duty ratio	1/33
Driver IC	STV8102
Operating temperature	-20~ 70°C
Storage temperature	-30~ 80°C

2 MECHANICAL SPECIFICATION

2.1 MECHANICAL CHARACTERISTICS

ITEM	CHARACTERISTIC	UNIT
Display Format	128 x 33	dots
Overall Dimensions	62.30 x 22.60 x 2.20	mm
Viewing Area	57.02 x 15.18	mm
Active Area	55.02 × 13.18	mm
Dot Size	0.41 x 0.38	mm
Dot Pitch	0.43 x 0.40	mm
Weight	5.7	g
IC Controller/Driver	STV8102	

2.2 MECHANICAL DRAWING



Notes:

1. Driver IC: STV8102
2. Die Size: 8730um x 1600um
3. COF Number: 8102UA
4. Interface:
   8-bit 68XX/80XX Parallel, 4-wire SPI, I2C
5. General Tolerance: ±0.30
6. The total thickness (2.20 Max) is without polarizer protective film, remove tape & double side tape.
   The actual assembled total thickness with above materials should be 2.70 Max.

3 ELECTRICAL SPECIFICATION

3.1 ABSOLUTE MAXIMUM RATINGS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Min	Max	Unit	Note
Power Supply Voltage	V_{DD_D}	-0.3	4.6	V	1, 2
OLED Power Supply	V_{PP}	-0.3	22	V	1, 2
Operating Temperature	T_{OP}	-20	70	°C	
Storage Temperature	T_{STG}	-30	80	°C	
Static Electricity	Be sure that you are grounded when handling displays.				

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3.2. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3.2 ELECTRICAL CHARACTERISTICS

VSS = 0 V, Ta = 25 °C

Item	Symbol	Condition	Min	Typ	Max	Unit
Power Supply for Logic	V_{DD_D}	Ta = 25 °C	1.8	3.3	3.6	V
Input Voltage	V_{IL}	Ta = 25 °C	GND	-	$0.3\times V_{DD\_D}$	V
	V_{IH}	Ta = 25 °C	$0.7\times V_{DD\_D}$	-	V_{DD_D}	V
OLED Module Driving Voltage	V_{PP}	Ta = 25 °C	11	12	13	V
V_{DD} Current	I_{DD}	50% Display Area ON (1)		TBD	TBD	µA
		100% Display Area ON (1)		TBD	TBD	µA
V_{PP} Current	I_{PP}	50% Display Area ON (1)		TBD	TBD	mA
		100% Display Area ON (1)		TBD	TBD	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	TBD	-	µA
Sleep Mode Current for V_{PP}	$I_{PP, SLEEP}$		-	TBD	-	µA

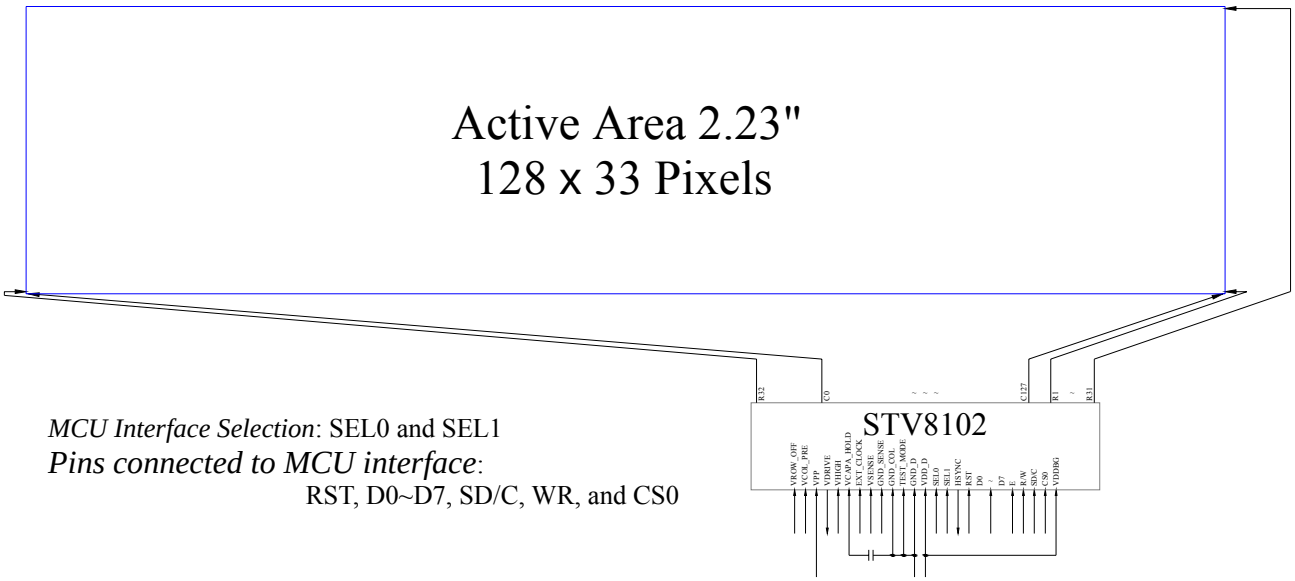
Note 1: V_{DD_D} = 3.3V, V_{PP} = 12V, Frame Rate = 66Hz, Bright Setting = 7Fh

3.3 INTERFACE PIN ASSIGNMENT

<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td>1</td><td>VROW_OFF</td><td>I</td><td>Reference Voltage for Row Electrode Off-Mode. It can be supplied externally or be left open while the reference voltage is internally-generated. A tank capacitor should be connected to the VROW_OFF pin for external setting. When display is not active, the row output pins are pulled-up to the off-state voltage.</td></tr>
<tr><td>2</td><td>VCOL_PRE</td><td>I</td><td>Reference Voltage for Column Electrode Pre-Charge Sequence. It can be supplied externally or be left open while the pre-charge voltage is internally generated. A tank capacitor should be connected to the VCOL_PRE pin for external setting</td></tr>
<tr><td>3</td><td>VPP</td><td>I</td><td>Power Supply for OLED Panel. It can be supplied externally or generated internally by using internal DC/DC voltage converter.</td></tr>
<tr><td>4</td><td>VDRIVE</td><td>O</td><td>Control Signal for Output Voltage Generator
This output pin drives the gate of external power NMOS.</td></tr>
<tr><td>5</td><td>VHIGH</td><td>I</td><td>High Voltage Step-up Circuit. This pin is the feedback signal for voltage regulation loop. It is used to adjust the booster output voltage level (VPP). An internal NMOS transistor connected between pins VHIGH and VDRIVE allows VPP to rise until the voltage on pin VDRIVE (stemming from VPP) is high enough to switch the external NMOS transistor.</td></tr>
<tr><td>6</td><td>VCAPA_HOLD</td><td>I</td><td>Pre-Charge Supply Filtering. This is the voltage supply pin. A capacitor should be connected between this pin and ground.</td></tr>
<tr><td>7</td><td>EXT_CLOCK</td><td>I</td><td>External System Clock Source. When internal clock is enabled, this pin should be left floating. When internal clock is disabled, this pin receives display clock signal from external clock source.</td></tr>
<tr><td>8</td><td>VSENSE</td><td>I</td><td>Feedback Signal. This pin is the feedback signal for voltage regulation loop. It is used to adjust the booster output voltage level (VPP). In case of VSENSE feedback disconnection the Driver is switched off.</td></tr>
<tr><td>9</td><td>GND_SENSE</td><td>I</td><td>Ground of Current Detection. This pin is the feedback signal for current sense. It is used for current detection for step-up circuitry.</td></tr>
<tr><td>10</td><td>GND_COL</td><td>I</td><td>Ground of Column Driver. This is the low level reference voltage for column electrode. It must be connected to external source on ground level or closed to ground.</td></tr>
<tr><td>11</td><td>TEST_MODE</td><td>I</td><td>Test Mode Select. This is a reserved pin for IC testing. It must be connected to ground for normal status.</td></tr>
<tr><td>12</td><td>GND_D</td><td>I</td><td>Ground of Logic Circuit. This is the ground pin. It also acts as the reference for the logic pins. It must be connected to external ground.</td></tr>
<tr><td>13</td><td>VDD_D</td><td>I</td><td>Power Supply for Logic Circuit. This is the voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>14</td><td>SEL0</td><td>I</td><td rowspan="2">Communicating Protocol Select
<table>
<tr><th></th><th>68XX-parallel</th><th>80XX-parallel</th><th>Serial</th><th>I2C</th></tr>
<tr><td>SEL0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>SEL1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td></tr>
<tr><td>15</td><td>SEL1</td><td>I</td></tr>
<tr><td>16</td><td>HSYNC</td><td>O</td><td>Horizontal Synchronization Triggering Signal. This pin will send out a signal that could be used to identify the driver status. It should be left open individually.</td></tr>
<tr><td>17</td><td>RST</td><td>I</td><td>Power Reset for Controller and Driver. This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
</table>

No.	Symbol	I/O	Function
18~25	D0~D7	I/O	*Host Data Input/Output Bus.* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D3/D2 will be the serial data input/output (SDIN/SDOUT) and D4 will be the serial clock input (SCLK). When I2C mode is selected, D5 will be the clock signal (SCL) and D6 will be the I2C data input (SDA). Refer to the configuration of I2C interface.
26	E	I	*Read/Write Enable or Read.* When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS0 is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS0 is pulled low.
27	R/W	I	*Read/Write Select or Write.*. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W) selection input. Read mode will be carried out when this pin is pulled high and write mode when low. When 80XX interface mode is selected, this pin will be the Write (WR) input. Data write operation is initiated when this pin is pulled low and the chip is selected.
28	SD/C	I	*Data/Command Control.*. When the pin is pulled high, the data at D7~D0 is treated as display data. When the pin is pulled low, the data at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
29	CS0	I	*Chip Select.* The chip is enabled for MCU communication only when CS0 is pulled low.
30	VDDBG	I	*Power Supply for Low Voltage Reference.* This is the voltage supply pin. It must be connected to external source.

3.4 BLOCK DIAGRAM



MCU Interface Selection: SEL0 and SEL1

Pins connected to MCU interface:

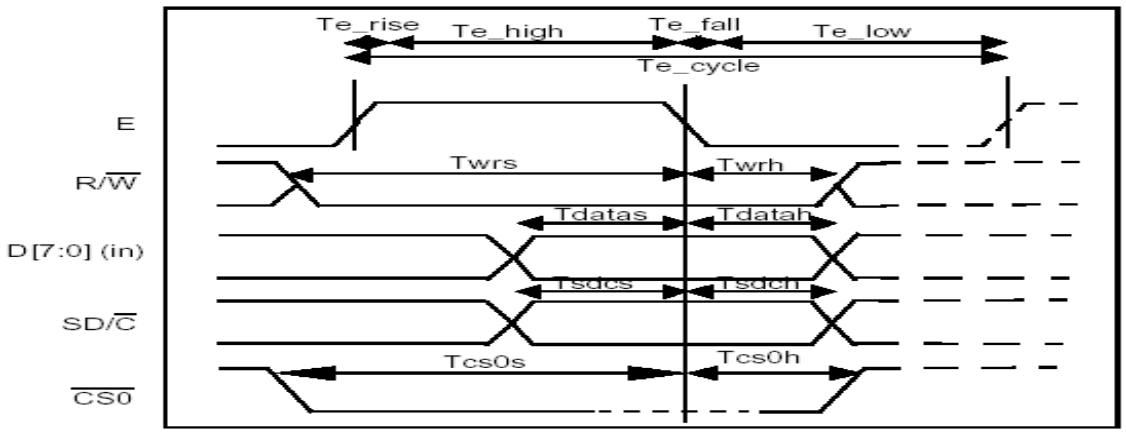
RST, D0~D7, SD/C, WR, and CS0

3.5 TIMING CHARACTERISTICS

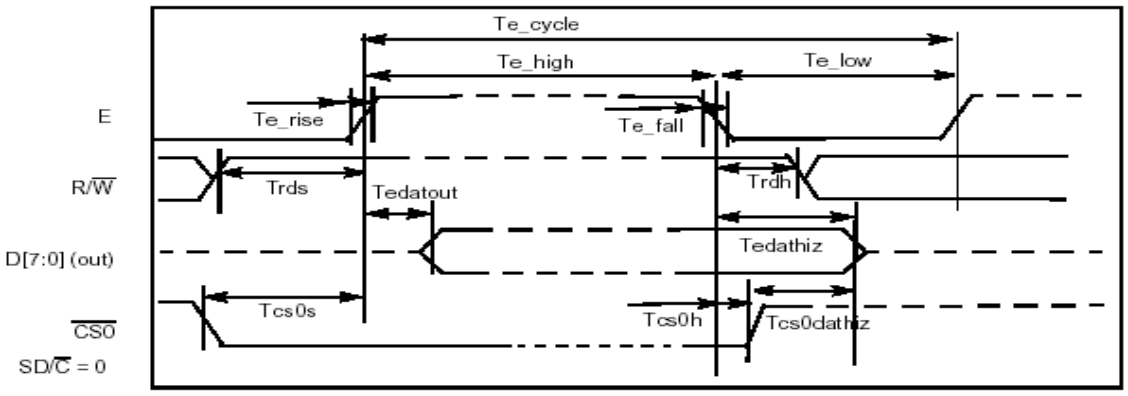
3.5.1 68XX-Series MPU Parallel Interface Timing Characteristics

Characteristics		Symbol	Min	Typ	Max	Unit
System Cycle Time		Te_cycle	300	-	-	ns
Write Low Pulse Width Read Low Pulse Width		Te_low	60 120	-	-	ns
Select High Pulse Width		Te_high	60	-	-	ns
Rise Time Fall Time		Te_rise Te_fall	-	-	15 15	ns
Write Data Setup Time Write Data Hold Time		Twrs Twrh	TBD	50 50	-	ns
Read Setup to E Rising Edge Read Hold fm E Falling Edge	CL=100pF	Trds Trdh	TBD	50 50	-	ns
Data Address Setup Time Data Address Hold Time		Tdatas Tdatah	25 25	-	-	ns
Data Output from E Rising Edge		Tedatout	-	20	TBD	ns
Data Hiz from E Falling Edge		Tedathiz	-	-	TBD	ns
Data Hiz from CS0 Rising Edge		Tcs0dathiz	-	-	TBD	ns
SD/C Setup Time SD/C Hold Time		Tsdcs Tsdch	TBD	60 60	-	ns
Chip Select Setup Time Chip Select Hold Time	Write	Tcs0s Tcs0h	TBD	120 60	-	ns
Chip Select Setup Time Chip Select Hold Time	Read	Tcs0s Tcs0h	120 60	-	-	ns

* All the timing should be based on 30% and 70% of V_{DD}-GND.



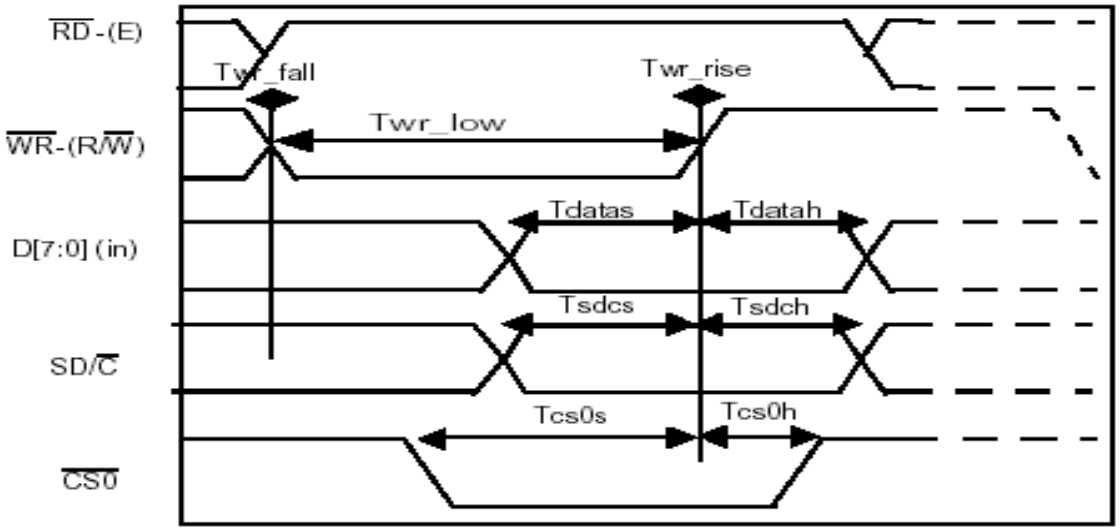
Timing diagram for Write mode



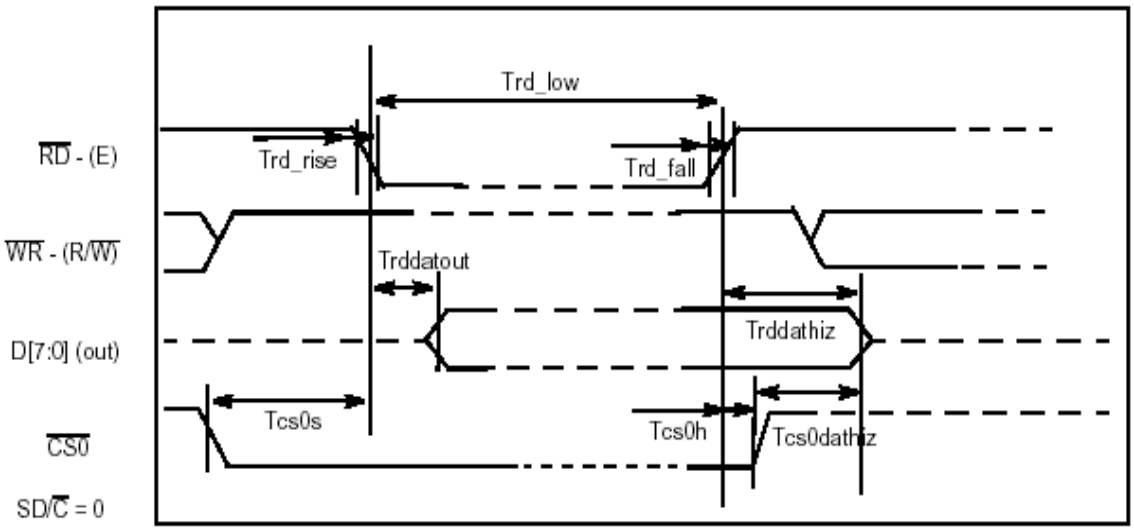
Timing diagram for Read mode (register only)

3.5.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Characteristics		Symbol	Min	Typ	Max	Unit
Write Low Pulse Width Read Low Pulse Width		Twr_low Trd_low	60 120	-	-	ns
Rise Time		Twr_rise Trd_rise	-	-	15 15	ns
Fall Time		Twr_fall Trd_fall	-	-	15 15	ns
Data Address Setup Time Data Address Hold Time		Tdatas Tdatah	25 25	-	-	ns
Data Output from RD Rising Edge	CL=100pF	Trddatout	-	20	TBD	ns
Data Hiz from RD Falling Edge	CL=100pF	Trddathiz	-	-	TBD	ns
Data Hiz from CS0 Rising Edge		Tcs0dathiz	-	-	TBD	ns
SD/C Setup Time SD/C Hold Time		Tsdcs Tsdch	TBD	60 60	-	ns
Chip Select Setup Time Chip Select Hold Time	(Read)	Tcs0s Tcs0h	TBD	120 60	-	ns
Chip Select Setup Time Chip Select Setup Time	(Write)	Tcs0s Tcs0h	120 60	-	-	ns



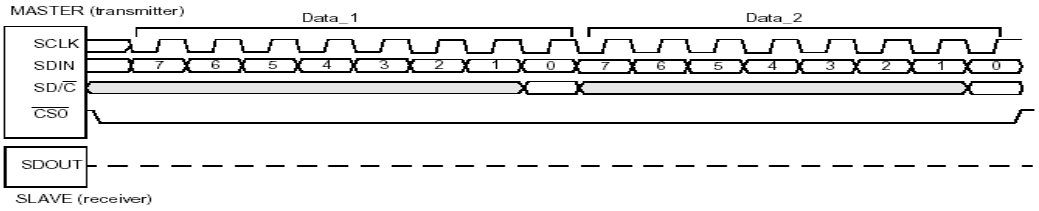
Timing Diagram for Write Mode

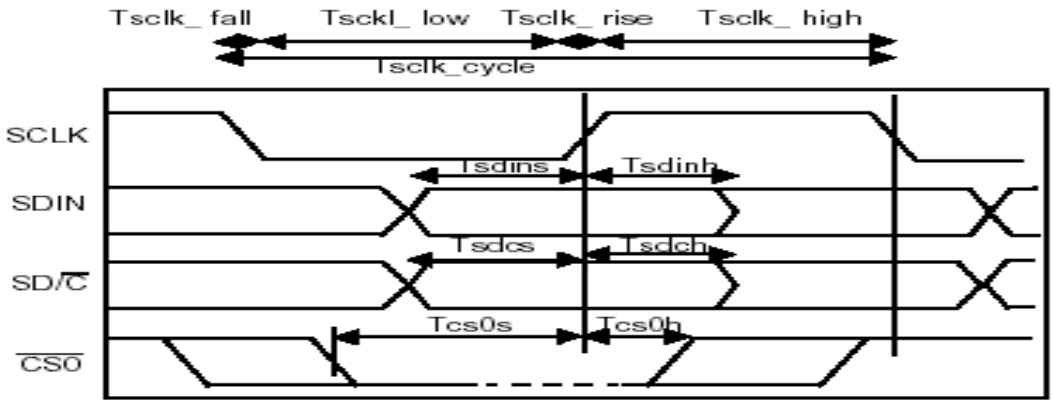


Timing Diagram for Read Mode

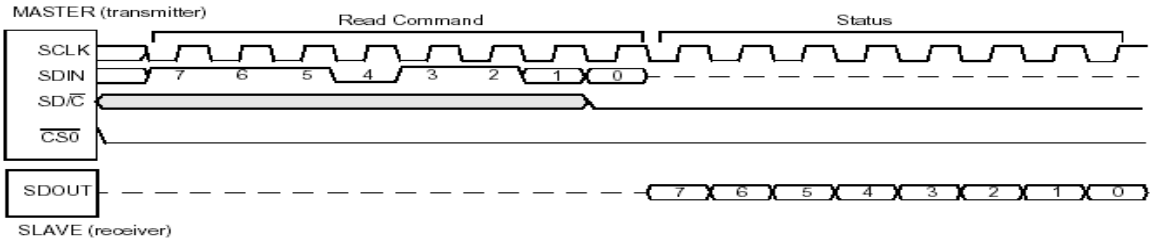
3.5.3 Serial Interface Timing Characteristics

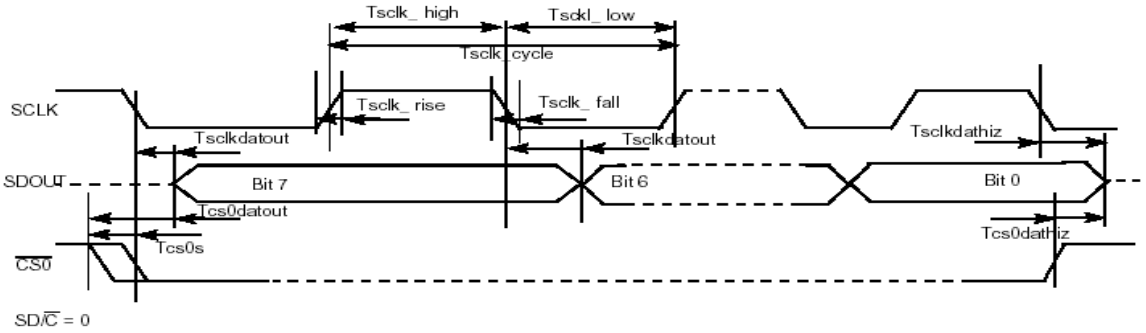
Description		Symbol	Min	Typ	Max	Unit
Serial Clock Cycle Time		T_{sclk_cycle}	250	-	-	ns
Write/Read Low Pulse Width		T_{sclk_low}	100	-	-	ns
Select High Pulse Width		T_{sclk_high}	100	-	-	ns
Rise Time Fall Time		T_{sclk_rise} T_{sclk_fall}	-	-	15 15	ns
Data Output Time after SCLK Falling Edge		$T_{sclkdatout}$	TBD	50	-	ns
Data Output Hiz State Time after SCLK Falling Edge		$T_{sclkdathiz}$	TBD	50	-	ns
Data Output Time after CS0 Falling Edge		$T_{cs0datout}$	TBD	50	-	ns
Data Output Hiz State Time after CS0 Rising Edge		$T_{cs0dathiz}$	TBD	50	-	ns
SDIN Setup Time SDIN Hold Time		T_{sdins} T_{sdinh}	100 100	-	-	ns
SD/C Setup Time SD/C Hold Time		T_{sdcs} T_{sdch}	150 150	-	-	ns
Chip Select Setup Time Chip Select Hold Time	(Write)	T_{cs0s} T_{cs0h}	150 150	-	-	ns
Chip Select Setup before SCLK Rising Edge	(Read)	T_{cs0s}	0	-	-	ns





Timing Diagram for Write Mode

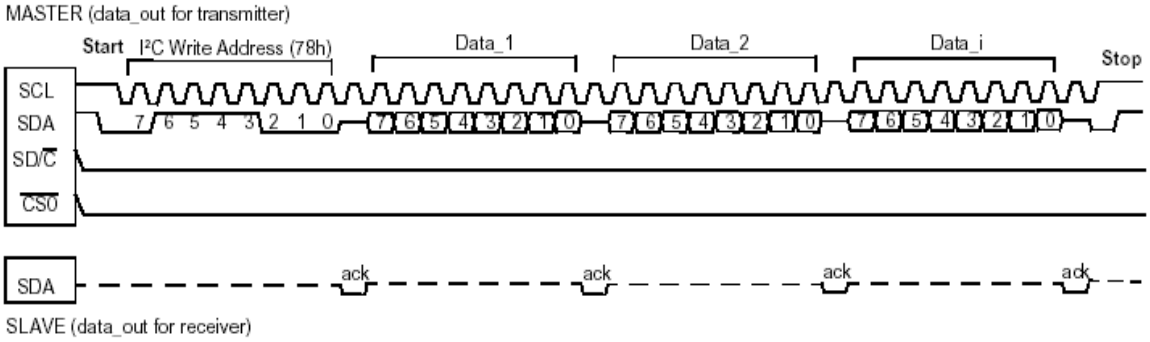




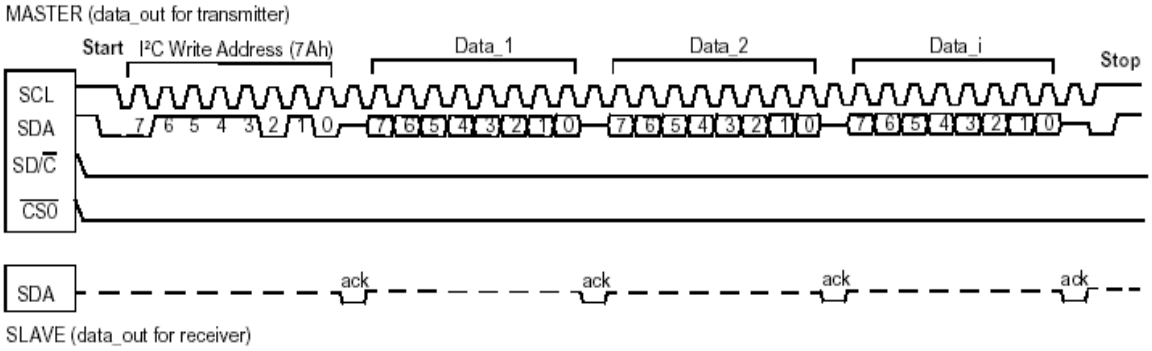
Timing diagram for Read mode (register only)

3.5.4 I²C Interface Timing Characteristics

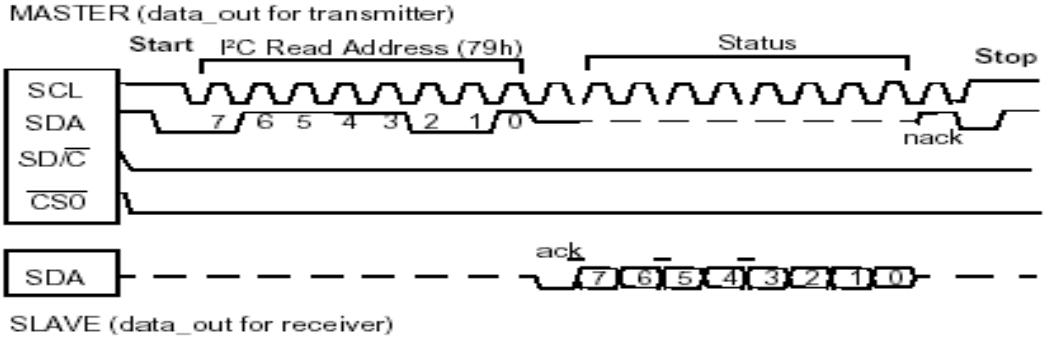
Description	Symbol	Min	Typ	Max	Unit
Serial Clock Cycle Time	T_{scl_cycle}	2.5	-	-	μs
Write/Read Low Pulse Width	T_{scl_low}	100	-	-	ns
Select High Pulse Width	T_{scl_high}	100	-	-	ns
Rise Time Fall Time	T_{scl_rise} T_{scl_fall}	-	-	15 15	ns
Data Setup Time Data Hold Time	T_{datas} T_{datah}	100 100	-	-	ns
Chip Select Setup Time Chip Select Hold Time	T_{cs0s} T_{cs0h}	120 120	-	-	ns



Timing Diagram for Write Mode (Register)



Timing Diagram for Write Mode (RAM)



Timing Diagram for Read Mode (Register Only)

4 OPTICAL SPECIFICATION

4.1 OPTICAL CHARACTERISTICS

Ta = 25 °C

Item	Symbol	Condition	Min	Typ	Max	Unit	Note
Brightness	L_{BR}	With Polarizer	60	80	-	cd/m²	Note1
C.I.E. (Blue)	(x) (y)	Without Polarizer	0.12 0.22	0.16 0.26	0.20 0.30		Note1
			0.12 0.22	0.16 0.26	0.20 0.30		Note1
Contrast Ratio	CR	Ta = 25 °C, dark room	-	>1:100	-	-	Note1
Viewing Angle			>160	-	-	degree	Note1

Note1: Optical measurement taken at 1/33 duty, 66Hz Frame Rate, 7Fh Bright Setting.

5 FUNCTIONAL SPECIFICATION

5.1 COMMANDS

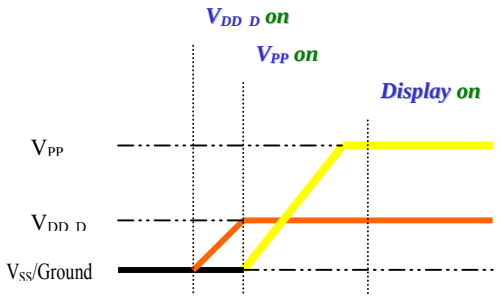
Refer to the Technical Manual for the STV8102

5.2 POWERING SEQUENCES

To protect the OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

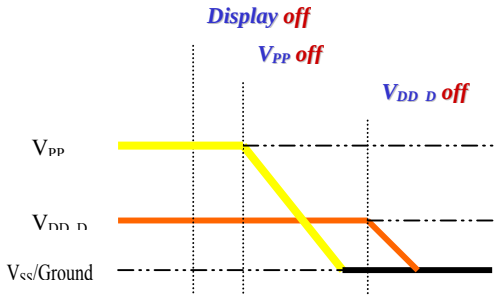
Power up Sequence:

1. Power up V_{DD_D}
2. Send Display off command
3. Clear Screen
4. Power up V_{PP}
5. Delay 100ms (when V_{DD_D} is stable)
6. Send Display on command



Power down Sequence:

1. Send Display off command
2. Power down V_{PP}
3. Delay 100ms (when V_{PP} reaches 0 and panel is completely discharges)
4. Power down V_{DD_D}



5.3 INITIALIZATION

5.3.1 Hardware Reset

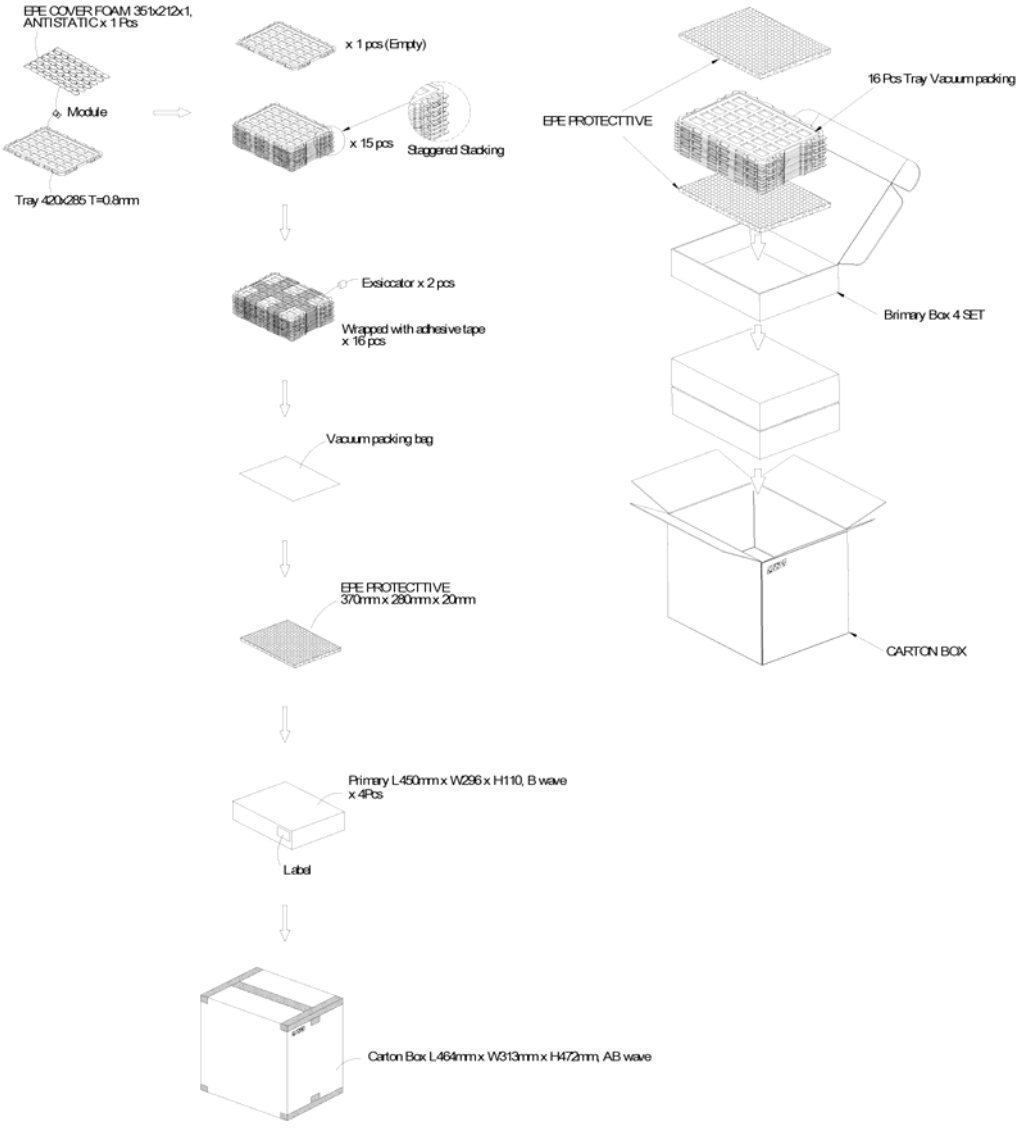
The default configuration after a hardware reset is the following:

- All the control registers are cleared: Display Off, DC/DC Step-up Off, Internal Oscillator Off, Scanning Off.
- The RAM contents are unchanged: after on Power On RAM contents are defined.

The hardware reset must be applied during the whole power-up sequence long, until the supplies reach the minimum value.

6 PACKAGING AND LABELLING SPECIFICATION

6.1 PACKAGING



6.2 LABELLING & MARKING

DENSITRON DD-12833BE-1A TW YYMM

7 QUALITY ASSURANCE SPECIFICATION

7.1 CONFORMITY

The performance, function and reliability of the shipped products conform to the Product Specification.

7.2 DELIVERY ASSURANCE

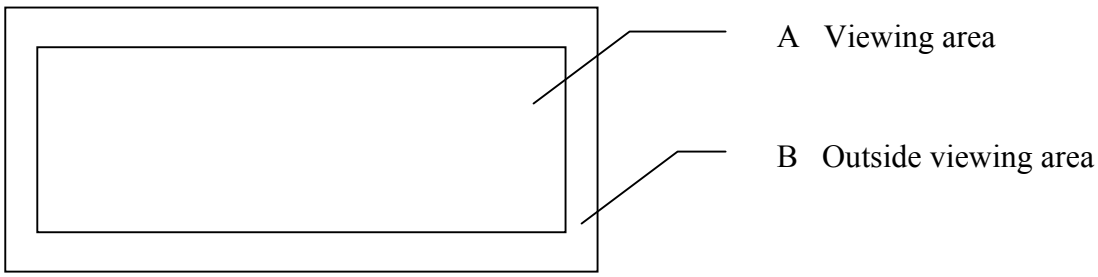
7.2.1 Delivery inspection standards

- MIL-STD-105E, general inspection level II, single sampling level;
- IPC-AA610 rev. C, class 2 electronic assemblies standard

The quality assurance levels are shown below:

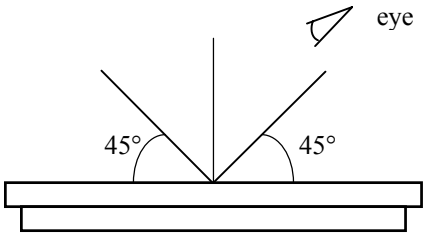
Class	AQL (%)
Critical defect	0.5%
Major defect	1.0%
Minor defect	1.5%
TOTAL	2.0%

7.2.2 Zone definition



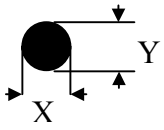
7.2.3 Visual inspection

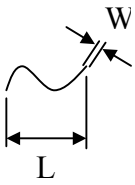
- Inspect under 30W fluorescent lamp leaving 50 cm between the module and the lamp and 30 cm between the module and the eye (measuring position).
- Appearance is inspected at the best contrast voltage (best contrast is adjusted considering clearness and crosstalk on screen).
- Inspect the module at 45° right and left, top and bottom.
- Use the optimum viewing angle during the contrast inspection.

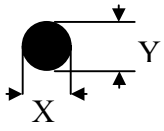


7.2.3.1 Standard of appearance inspection

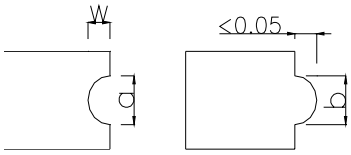
Units: mm

<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td rowspan="2">Packing & Label</td><td>Outside & inside package | Presence of product no., lot no., quantity</td></tr>
<tr><td>Critical</td><td>Product must not be mixed with others and quantity must not be different from that indicated on the label</td></tr>
<tr><td>Major</td><td>Dimension</td><td>Product dimensions must be according to specification and drawing</td></tr>
<tr><td>Major</td><td>Electrical</td><td>Product electrical characteristics must be according to specification</td></tr>
<tr><td>Critical</td><td>LCD Display</td><td>Missing lines or wrong patterns on LCD display are not allowed</td></tr>
<tr><td>Minor</td><td>Black spot, white spot, dust</td><td>Round type: as per following drawing
∅ = (X+Y)/2
 

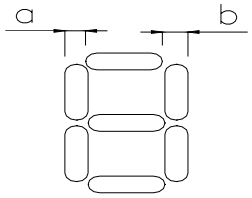
<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>0.1<∅<0.2</td><td>3</td></tr><tr><td>0.2<∅<0.25</td><td>1</td></tr><tr><td>0.25<∅</td><td>0</td></tr></table>
Line type: as per following drawing
 

<table><tr><th colspan="4">Acceptable quantity</th></tr><tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr><tr><td>- -</td><td>W≤0.05</td><td>Any number</td><td rowspan="3">Any number</td></tr><tr><td>L≤2.0</td><td>W≤0.1</td><td>3</td></tr><tr><td>L>2.0</td><td></td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
<tr><td>Minor</td><td>Polariser scratch</td><td>Scratch on protective film is permitted
Scratch on polariser: same as No. 1</td></tr>
<tr><td>Minor</td><td>Polariser bubble</td><td>∅ = (X+Y)/2
 

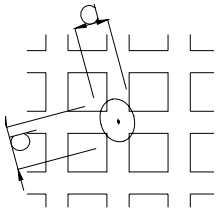
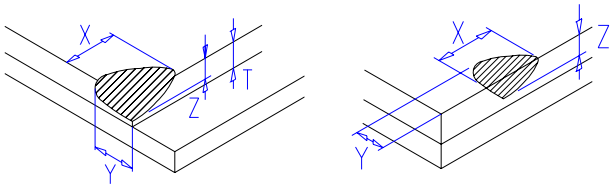
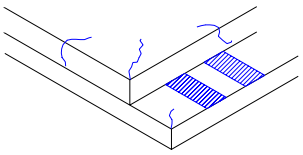
<table><tr><th colspan="3">Acceptable quantity</th></tr><tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr><tr><td>∅<0.5</td><td>Any number</td><td rowspan="2">Any number</td></tr><tr><td>∅>0.5</td><td>0</td></tr></table>
Total acceptable quantity: 3</td></tr>
</table>

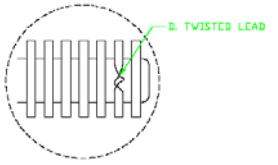
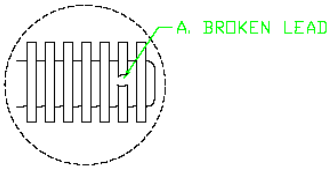
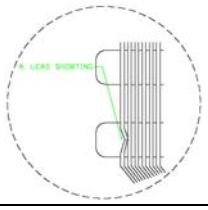
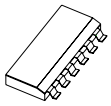
<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Segment deformation</td><td>1b. Pin hole on dot matrix display
 

<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>a,b<0.1</td><td>Any number</td></tr>
<tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr>
<tr><td>0.5<∅<1.0</td><td>3</td></tr>
</table>
Total acceptable quantity: 7

2. Segments / dots with different width
 

<table>
<tr><td colspan="2">Acceptable</td></tr>
<tr><td>a≥b</td><td>a/b≤4/3</td></tr>
<tr><td>a<b</td><td>a/b>4/3</td></tr>
</table>

3. Alignment layer defect
∅ = (a+b)/2
 
<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>∅≤0.4</td><td>Any number</td></tr>
<tr><td>0.4<∅≤1.0</td><td>5</td></tr>
<tr><td>1.0<∅≤1.5</td><td>3</td></tr>
<tr><td>1.5<∅≤2.0</td><td>2</td></tr>
</table>
Total acceptable quantity: 7</td></tr>
<tr><td>Minor</td><td>Panel Chipping</td><td>X ≤ 1/6 Panel length
Y ≤ 1
Z ≤ T
 
</td></tr>
<tr><td>Minor</td><td>Panel Cracking</td><td>Cracks not allowed
  </td></tr>
<tr><td>Minor</td><td>Cupper exposed (pin or film)</td><td>Not allowed if visible by eye inspection</td></tr>
<tr><td>Minor</td><td>Film or Trace Damage</td><td>Not allowed if affects electrical function</td></tr>
</table>

<table>
<tr><th>Class</th><th>Item</th><th>Criteria</th></tr>
<tr><td>Minor</td><td>Contact
Lead Twist</td><td>Not allowed  </td></tr>
<tr><td>Minor</td><td>Contact
Lead
Broken</td><td>Not allowed  </td></tr>
<tr><td rowspan="2">Minor</td><td rowspan="2">Contact
Lead Bent</td><td>Not allowed if
bent lead causes
short circuit  </td></tr>
<tr><td>Not allowed if bent lead
extends horizontally
more than 50%
of its width  </td></tr>
<tr><td>Minor</td><td>Colour
uniformity</td><td>Level of sample for approval set as limit sample</td></tr>
<tr><td>Major</td><td rowspan="4">PCB  </td><td>No unmelted solder paste should be present on PCB</td></tr>
<tr><td>Critical</td><td>Cold solder joints, missing solder connections, or oxidation are not allowed</td></tr>
<tr><td>Minor</td><td>No residue or solder balls on PCB are allowed</td></tr>
<tr><td>Critical</td><td>Short circuits on components are not allowed</td></tr>
<tr><td>Minor</td><td>Tray
particles</td><td>
<table>
<tr><th></th><th>Size</th><th>Quantity</th></tr>
<tr><td rowspan="2">On tray</td><td>∅<0.2</td><td>Any number</td></tr>
<tr><td>∅>0.25</td><td>4</td></tr>
<tr><td rowspan="2">On display</td><td>∅≥0.25</td><td>2</td></tr>
<tr><td>L = 3</td><td>1</td></tr>
</table>
</td></tr>
</table>

7.3 DEALING WITH CUSTOMER COMPLAINTS

7.3.1 Non-conforming analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.
After accepting it, Densitron should complete the analysis in two weeks from receiving the sample.
If the analysis cannot be completed on time, Densitron must inform the purchaser.

7.3.2 Handling of non-conforming displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.
Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.
Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

8 RELIABILITY SPECIFICATION

8.1 RELIABILITY TESTS

Test Item	Test Condition	Evaluation and assessment
High Temperature Operation	85°C, 500 hrs	No abnormalities in function* and appearance Brightness > ½ initial value
Low Temperature Operation	-30°C, 500 hrs	
High Temperature Storage	90°C, 500 hrs	
Low Temperature Storage	-40°C, 500 hrs	
High Temperature & High Humidity Storage	60°C, 90% RH, 500 hrs	
Thermal Shock Storage	-40°C ⇔ 85°C, 100 cycles 30 mins dwell	

- The brightness should be greater than 50% of the initial brightness.
- The samples used for above tests do not include polarizer.
- No moisture condensation is observed during tests.

8.1.1 FAILURE CHECK STANDARD

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5 °C; 55±15% RH

8.2 LIFE TIME

Item	Description
1	Function, performance, appearance, etc. shall be free from remarkable deterioration within 15,000 hours under ordinary operating and storage conditions of room temperature (25±10 °C), normal humidity (45±20% RH), and in area not exposed to direct sunlight.
2	End of lifetime is specified as 50% of initial brightness.

9 HANDLING PRECAUTIONS

Safety
If the panel breaks, be careful not to get the organic substance in your mouth or in your eyes.
If the organic substance touches your skin or clothes, wash it off immediately using soap and plenty of water.

Mounting and Design
Place a transparent plate (e.g. acrylic, polycarbonate or glass) on the display surface to protect the display from external pressure. Leave a small gap between the transparent plate and the display surface.
Design the system so that no input signal is given unless the power supply voltage is applied.

Caution during OLED cleaning
Lightly wipe the display surface with a soft cloth soaked with Isopropyl alcohol, Ethyl alcohol or Trichlorotriflorothane.
Do not wipe the display surface with dry or hard materials that will damage the polariser surface.
Do not use aromatic solvents (toluene and xylene), or ketonic solvents (ketone and acetone).

Caution against static charge
As the display uses C-MOS LSI drivers, connect any unused input terminal to V_{DD} or V_{SS}. Do not input any signals before power is turned on.
Also, ground your body, work/assembly table and assembly equipment to protect against static electricity.

Packaging
Displays use OLED elements, and must be treated as such. Avoid strong shock and drop from a height.
To prevent displays from degradation, do not operate or store them exposed directly to sunshine or high temperature/humidity.

Caution during operation
It is indispensable to drive the display within the specified voltage limit since excessive voltage shortens its life.

Other Precautions
When a display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored.
Also, there will be no problem in the reliability of the module.

Storage
Store the display in a dark place where the temperature is 25°C ± 10°C and the humidity below 50%RH.
Store the display in a clean environment, free from dust, organic solvents and corrosive gases.
Do not crash, shake or jolt the display (including accessories).