PRELIMINARY

CY9C62256

32K x 8 Magnetic Nonvolatile CMOS RAM

Features

- **100% form, fit, function-compatible with 32K × 8 micropower SRAM (CY62256)**
  - **— Fast Read and Write access: 70 ns**
  - **— Voltage range: 4.5V–5.5V operation**
  - **— Low power: 330 mW Active; 495 μW standby**
  - **— Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
  - **— TTL-compatible inputs and outputs**
  - **— Automatic power-down when deselected**
- **Replaces 32K × 8 Battery Backed (BB)SRAM, SRAM, EEPROM, FeRAM or Flash memory**
- **Data is automatically Write protected during power loss**
- **Write Cycles Endurance: > 10^{15} cycles**
- **Data Retention: > 10 Years**
- **Shielded from external magnetic fields**
- **Extra 64 Bytes for device identification and tracking**
- **Temperature ranges**
  - **— Commercial: 0°C to 70°C**
  - **— Industrial: – 40°C to 85°C**
- **JEDEC STD 28-pin DIP (600-mil), 28-pin (300-mil) SOIC, and 28-pin TSOP-1 packages. Also available in 450-mil wide (300-mil body width) 28-pin narrow SOIC.**

Functional Description

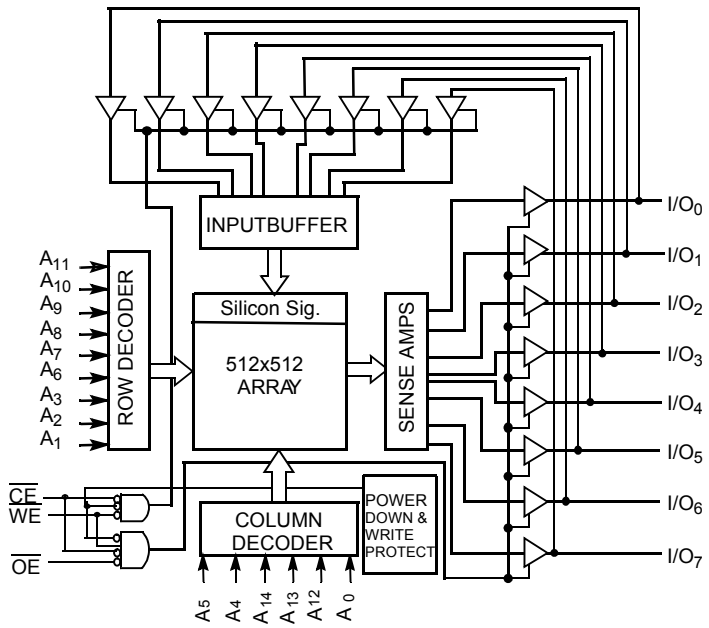
The CY9C62256 is a high-performance CMOS nonvolatile RAM employing an advanced magnetic RAM (MRAM) process. An MRAM is nonvolatile memory that operates as a fast read and write RAM. It provides data retention for more than ten years while eliminating the reliability concerns, functional disadvantages and system design complexities of battery-backed SRAM, EEPROM, Flash and FeRAM. Its fast writes and high write cycle endurance makes it superior to other types of nonvolatile memory.

The CY9C62256 operates very similarly to SRAM devices. Memory read and write cycles require equal times. The MRAM memory is nonvolatile due to its unique magnetic process. Unlike BBSRAM, the CY9C62256 is truly a monolithic nonvolatile memory. It provides the same functional benefits of a fast write without the serious disadvantages associated with modules and batteries or hybrid memory solutions.

These capabilities make the CY9C62256 ideal for nonvolatile memory applications requiring frequent or rapid writes in a bytewide environment.

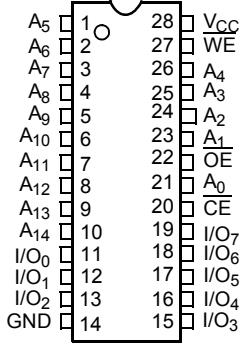
The CY9C62256 is offered in both commercial and industrial temperature ranges.

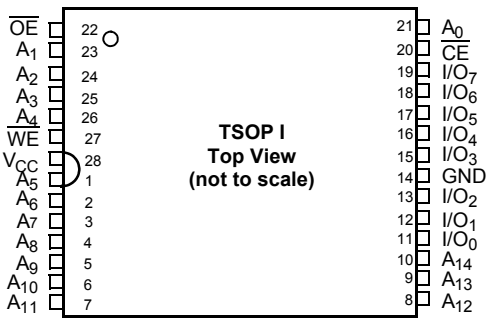
Logic Block Diagram



Pin Configurations

SOIC/DIP
Top View





TSOP I
Top View
(not to scale)

Overview

The CY9C62256 is a byte wide MRAM memory. The memory array is logically organized as 32,768 x 8 and is accessed using an industry standard parallel asynchronous SRAM-like interface. The CY9C62256 is inherently nonvolatile and offers write protect during sudden power loss. Functional operation of the MRAM is similar to SRAM-type devices, otherwise.

Memory Architecture

Users access 32,768 memory locations each with eight data bits through a parallel interface. Internally, the memory array is organized into eight blocks of 512 rows x 64 columns each.

The access and cycle time are the same for read and write memory operations. Unlike an EEPROM or Flash, it is not necessary to poll the device for a ready condition since writes occur at bus speed.

Memory Operation

The CY9C62256 is designed to operate in a manner similar to other bytewide memory products. For users familiar with BBSRAM, the MRAM performance is superior. For users familiar with EEPROM, Flash and FeRAM, the obvious differences result from higher write performance of MRAM technology and much higher write endurance.

All memory array bits are set to logic “1” at the time of shipment.

Read Operation

A read cycle begins whenever $\overline{WE}$ (Write Enable bar) is inactive (HIGH) and $\overline{CE}$ (Chip Enable bar) and $\overline{OE}$ (Output Enable bar) are active LOW. The unique address specified by the 15 address inputs (A0–A14) defines which of the 32,768 bytes of data is to be accessed. Valid data will be available at the eight output pins within t_{AA} (access time) after the last address input is stable, providing that $\overline{CE}$ and $\overline{OE}$ access times are also satisfied. If $\overline{CE}$ and $\overline{OE}$ access times are not satisfied then the data access must be measured from the later-occurring signal ($\overline{CE}$ or $\overline{OE}$) and the limiting parameter is either t_{ACE} for $\overline{CE}$ or t_{DOE} for the $\overline{OE}$ rather than address access.

Write Cycle

The CY9C62256 initiates a write cycle whenever the $\overline{WE}$ and $\overline{CE}$ signals are active (LOW) after address inputs are stable. The later occurring falling edge of $\overline{CE}$ or $\overline{WE}$ will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of $\overline{CE}$ or $\overline{WE}$. All address inputs must be kept valid throughout the write cycle. The $\overline{OE}$ control signal should be kept inactive (HIGH) during write cycles to avoid bus contention. However, if the output drivers are enabled ($\overline{CE}$ and $\overline{OE}$ active) $\overline{WE}$ will disable the outputs in t_{HZWE} from the $\overline{WE}$ falling edge.

Unlike other nonvolatile memory technologies, there is no write delay with MRAM. The entire memory operation occurs in a single bus cycle. Therefore, any operation including read or write can occur immediately following a write. Data Polling, a technique used with EEPROMs to determine if the write is complete is unnecessary. Page write, a technique used to enhance EEPROM write performance is also unnecessary because of inherently fast write cycle time for MRAM.

The total Write time for the entire 256K array is 2.3 ms.

Write Inhibit and Data Retention Mode

This feature protects against the inadvertent write. The CY9C62256 provides full functional capability for V_{CC} greater than 4.5V and write protects the device below 4.0V. Data is maintained in the absence of V_{CC}. During the power-up, normal operation can resume 20 µs after V_{PFD} is reached. Refer to page 8 for details.

Sudden Power Loss—“Brown Out”

The nonvolatile RAM constantly monitors V_{CC}. Should the supply voltage decay below the operating range, the CY9C62256 automatically write-protects itself, all inputs become don’t care, and all outputs become high-impedance. Refer to page 8 for details.

Silicon Signature/Device ID

An extra 64 bytes of MRAM are available to the user for Device ID. By raising A9 to V_{CC} + 2.0V and by using address locations 00(Hex) to 3F(Hex) on address pins A7, A6, A14, A13, A12 and A0 (MSB to LSB) respectively, the additional Bytes may be accessed in the same manner as the regular memory array, with 140 ns access time. Dropping A9 from input high (V_{CC} + 2.0V) to $\leq V_{CC}$ returns the device to normal operation after 140-ns delay.

Address (MSB to LSB) A7 A6 A14 A13 A12 A0	Description	ID
00h	Manufacturer ID	34h
01h	Device ID	40h
02h – 3Fh	User Space	62 Bytes

All User Space bits above are set to logic “1” at the time of shipment.

Magnetic Shielding

CY9C62256 is protected from external magnetic fields through the application of a “magnetic shield” that covers the entire memory array.

Applications

Battery-Backed SRAM (BB SRAM) Replacement

CY9C62256 is designed to replace (plug and play) existing BBSRAM while eliminating the need for battery and V_{CC} monitor IC, reducing cost and board space and improving system reliability.

The cost associated with multiple components and assemblies and manufacturing overhead associated with battery-backed SRAM is eliminated by using monolithic MRAM. CY9C62256 eliminates multiple assemblies, connectors, modules, field maintenance and environmental issues common with BB SRAM. MRAM is a true nonvolatile RAM with high performance, high endurance, and data retention.

Battery-backed SRAMs are forced to monitor V_{CC} in order to switch to the backup battery. Users that are modifying existing designs to use MRAM in place of BB SRAM, can eliminate the V_{CC} controller IC along with the battery. MRAM performs this function on chip.

Cost: The cost of both the component and manufacturing overhead of battery-backed SRAM is high. In addition, there is a built in rework step required for battery attachment in case

of surface mount assembly. This can be eliminated with MRAM. In case of DIP battery backed modules, the assembly techniques are constrained to through-hole assembly and board wash using no water.

System Reliability: Battery-backed SRAM is inherently vulnerable to shock and vibration. In addition, a negative voltage, even a momentary undershoot, on any pin of a battery-backed SRAM can cause data loss. The negative voltage causes current to be drawn directly from the battery, weakens the battery, and reduces its capacity over time. In general, there is no way to monitor the lost battery capacity. MRAM guarantees reliable operation across the voltage range with inherent nonvolatility.

Space: Battery-backed SRAM in DIP modules takes up board space height and dictates through-hole assembly. MRAM is offered in surface mount as well as DIP packages.

Field Maintenance: Batteries must eventually be replaced and this creates an inherent maintenance problem. Despite projections of long life, it is difficult to know how long a battery will last, considering all the factors that degrade them.

Environmental: Lithium batteries are a potential disposal burden and considered a fire hazard. MRAM eliminates all such issues through a truly monolithic nonvolatile solution.

Users replacing battery-backed SRAMs with integrated Real Time Clock (RTC) in the same package may need to move RTC function to a different location within the system.

EEPROM Replacement

CY9C62256 can also replace EEPROM in current applications. CY9C62256 is pinout and functionally compatible to bytewide EEPROM, however it does not need data-bar polling, page write and hardware write protect due to its fast write and inadvertent write protect features.

Users replacing EEPROMs with MRAM can eliminate the page mode operation and simplify to standard asynchronous write. Additionally, data-bar polling can be eliminated, since every byte write is completed within same cycle. All writes are completed within 70 ns.

FeRAM Replacement

FeRAM requires addresses to be latched on falling edge of $\overline{CE}$, which adds to system overhead in managing the $\overline{CE}$ and latching function. MRAM eliminates this overhead by offering a simple asynchronous SRAM interface.

Users replacing FeRAM can simplify their address decoding since $\overline{CE}$ does not need to be driven active and then inactive for each address. This overhead is eliminated when using MRAM.

Secondly, MRAM read is nondestructive and no precharge cycle is required like the one used with FeRAM.This has no apparent impact to the design, however the read cycle time can now see immediate improvement equal to the precharge time.

Boot-up PROM (EPROM, PROM) Function Replacement

The CY9C62256 can be accessed like an EPROM or PROM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. MRAM may be used to accomplish system boot up function using this condition.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–40°C to +85°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... –0.5V to +7.0V

DC Voltage Applied to Outputs in High-Z State[1] .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[1].....–0.5V to V_{CC} + 0.5V

except in case of Super Voltage pin (A9) while accessing 64 device ID and Silicon signature Bytes.....–0.5V to V_{CC} + 2.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage .....> 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Maximum Exposure to Magnetic Field @ Device Package[2,3] ..... ≤ 20 Oe

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

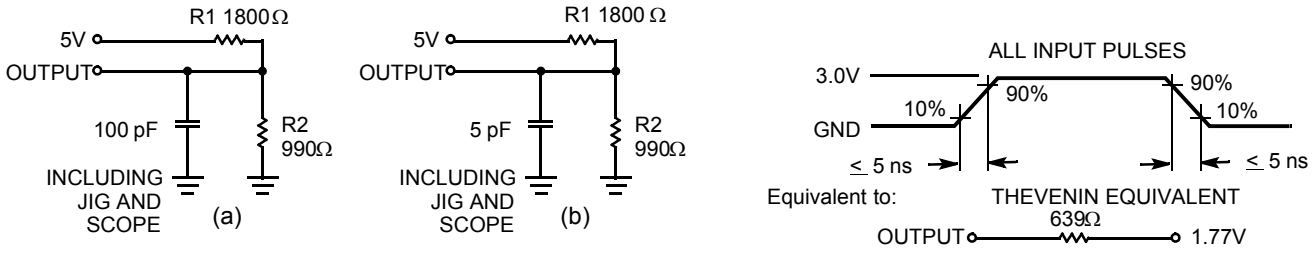
Parameter	Description	Test Conditions	CY9C62256-70			Unit
			Min.	Typ.[5]	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA	2.4			V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 2.1 mA			0.4	V
V_{IH}	Input HIGH Voltage		2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage		–0.5[1]		0.8	V
I_{IX}[4]	Input Leakage Current	GND ≤ V_I ≤ V_{CC}	–0.5		+0.5	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled	–0.5		+0.5	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$			60	mA
I_{SB1}	Automatic $\overline{CE}$ Power-down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			500	µA
I_{SB2}	Automatic $\overline{CE}$ Power-down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = 0			90	µA

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	6	pF
C_{OUT}	Output Capacitance		8	pF

Notes:
1. V_{IL} (min.) = –2.0V for pulse duration of 20 ns.
2. Magnetic field exposure is highly dependent on the distance from the magnetic field source. The magnetic field falls off as 1/R squared, where R is the distance from the magnetic source.
3. Exposure beyond this level may cause loss of data.
4. I_{IX} during access to 64 device ID and silicon signature bytes with super voltage pin at V_{CC} + 2.0V will be 100 µA max.
5. Typical specifications are the mean values measured over a large sample size across normal production process variations and are taken at nominal conditions (T_A = 25°C, V_{CC}). Parameters are guaranteed by design and characterization, and not 100% tested.
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



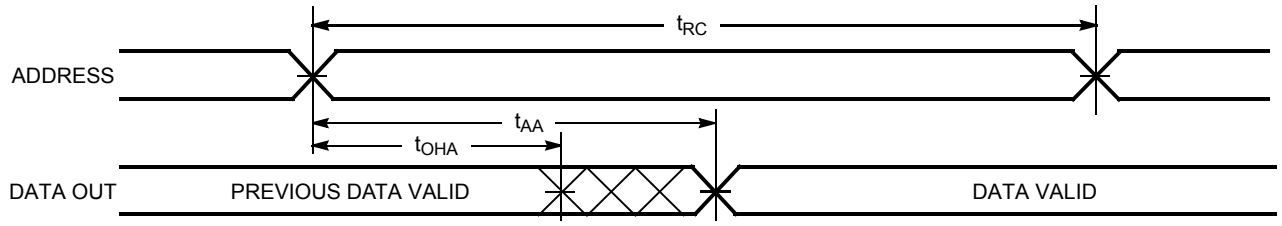
Switching Characteristics Over the Operating Range[7]

Parameter	Description	CY9C62256-70		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	5		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[8]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[8,9]		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[8]	5		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[8,9]		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		70	ns
Write Cycle[10,11]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		ns
t_{AW}	Address Set-up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{SD}	Data Set-up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[8, 9]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[8]	5		ns

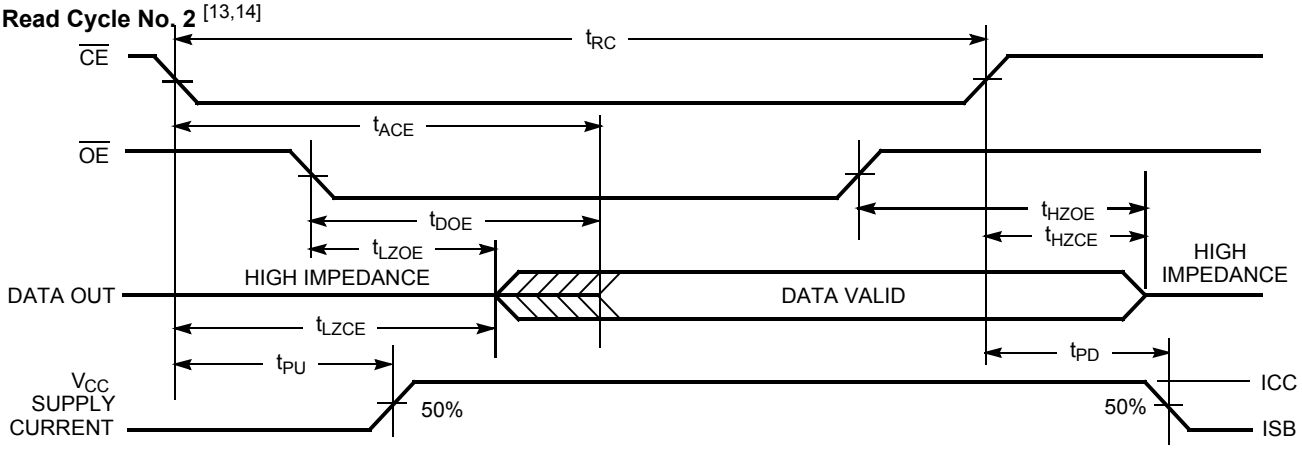
Notes:
7. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
8. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
11. The minimum write pulse width for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

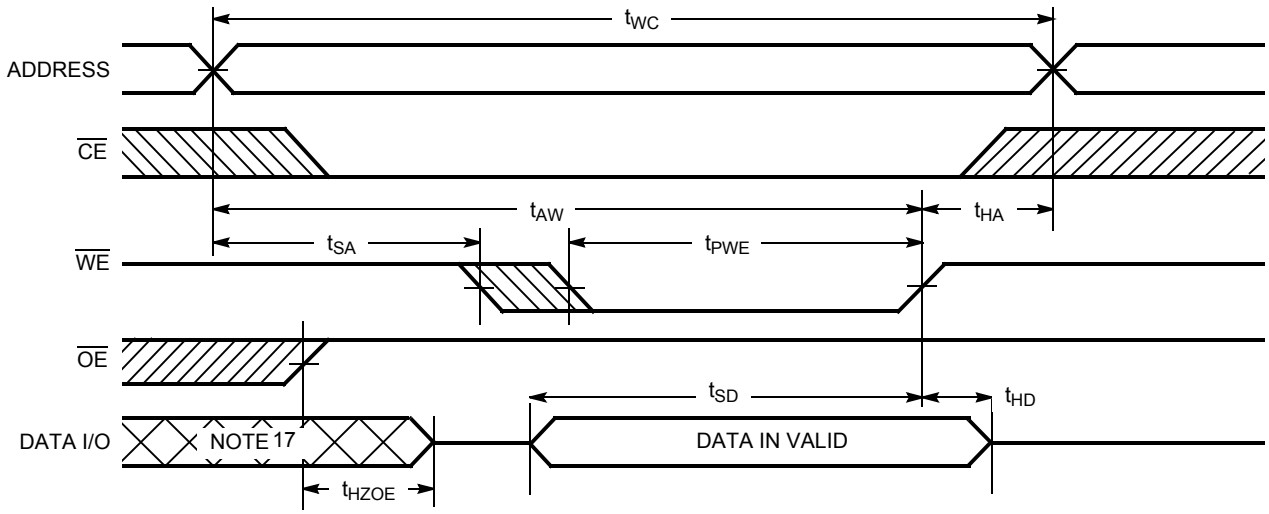
Read Cycle No. 1 [12, 13]



Read Cycle No. 2 [13,14]



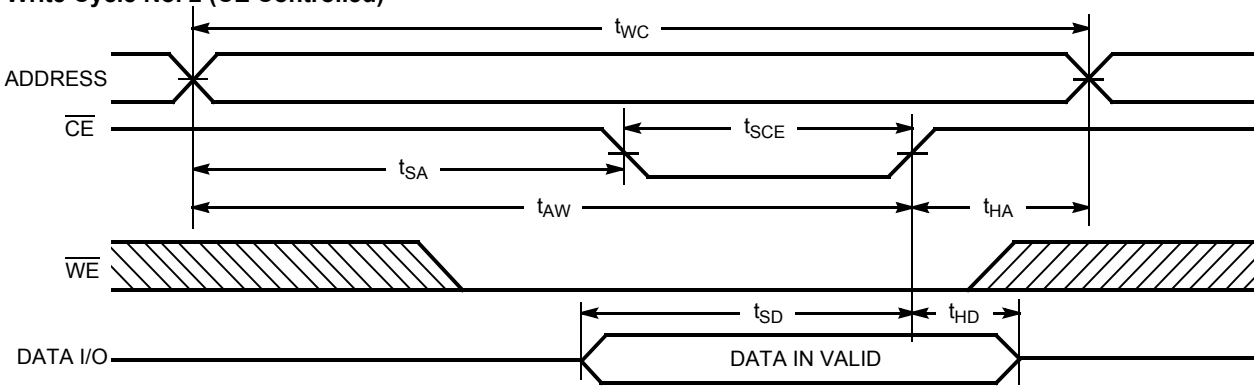
Write Cycle No. 1 ($\overline{WE}$ Controlled) [10,15,16]



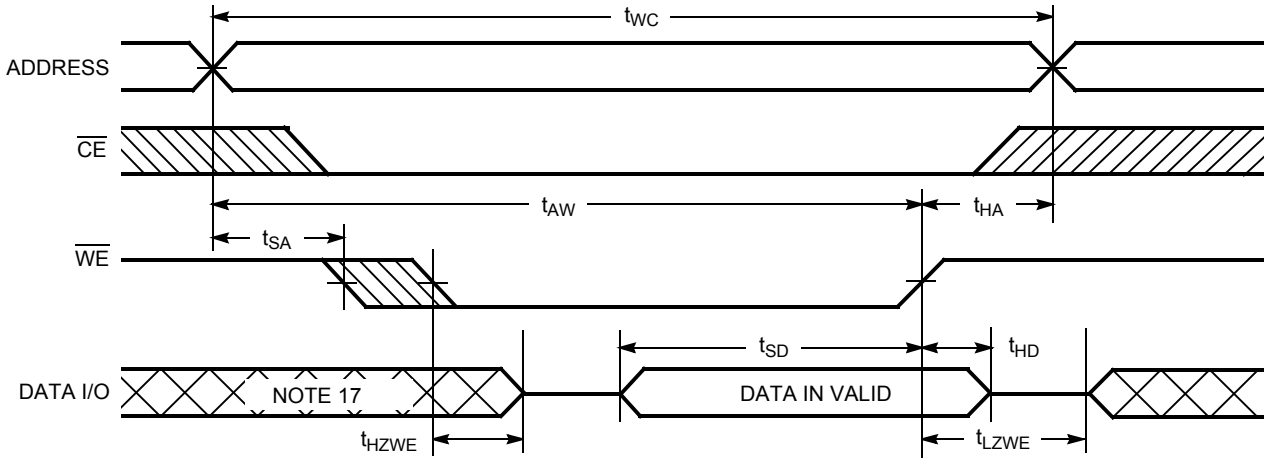
Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
15. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state.
17. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled) [10,15,16]



Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [11,16]

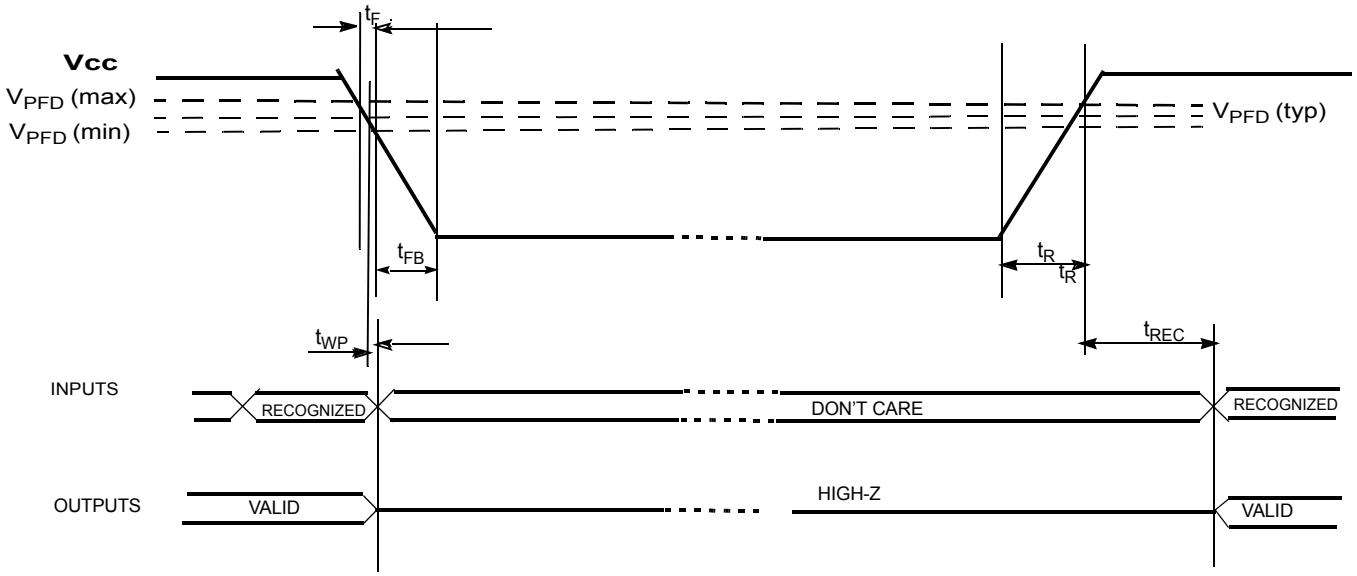


Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	V_{CC}	Inputs/Outputs	Mode	Power
H	X	X	4.5V–5.5V	High Z	Deselect/Power-down	Standby (I_{SB})
L	H	L	4.5V–5.5V	Data Out	Read	Active (I_{CC})
L	L	X	4.5V–5.5V	Data In	Write	Active (I_{CC})
L	H	H	4.5V–5.5V	High Z	Deselect, Output Disabled	Active (I_{CC})
X	X	X	<4.0V	Inputs = X, Outputs = Hi-Z	Write Inhibit	Active (I_{CC})

Power-down/-up Mode AC Waveforms

Parameter	Description	Min.	Typ.	Max.	Unit
V_{PFD}	Power-fail Deselect Voltage	4.2	4.35	4.5	V
t_F[18]	V_{PFD} (max.) to V_{PFD} (min.) V_{CC} Fall Time	100			µs
t_{FB}	V_{PFD} (min.) to V_{SS} V_{CC} Fall Time	50			µs
t_R	V_{SS} to V_{PFD} (max.) Rise Time	20			µs
t_{WP}	Write Protect Time On V_{CC} = V_{PFD} (typ)			20	µs
t_{REC}	V_{PFD} (max.) to Inputs Recognized			500	µs



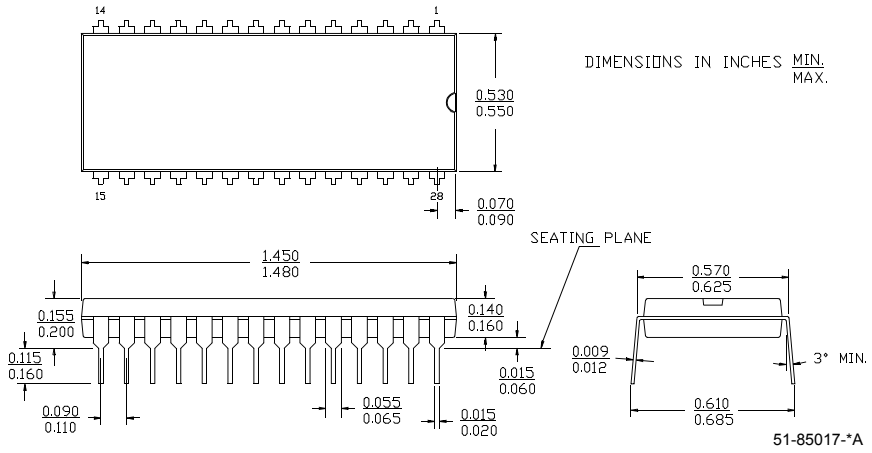
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY9C62256–70SC	S21	28-lead (300-mil) Molded SOIC	Commercial
	CY9C62256-70SI	S21	28-lead (300-mil) Molded SOIC	Industrial
	CY9C62256-70SNC	SN28	28-lead (300-mil) Narrow Body SOIC	Commercial
	CY9C62256-70SNI	SN28	28-lead (300-mil) Narrow Body SOIC	Industrial
	CY9C62256–70ZC	Z28	28-lead Thin Small Outline Package	Commercial
	CY9C62256–70ZI	Z28	28-lead Thin Small Outline Package	Industrial
	CY9C62256–70PC	P15	28-lead (600-mil) Molded DIP	Commercial
	CY9C62256-70PI	P15	28-lead (600-mil) Molded DIP	Industrial

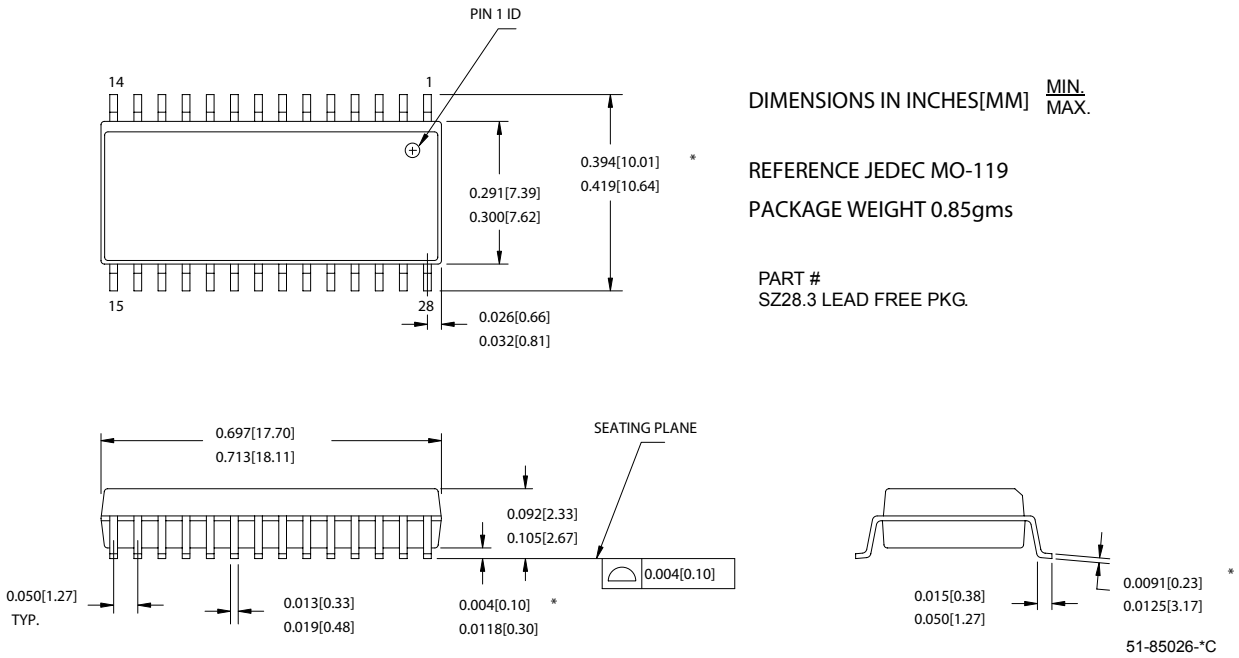
Note:
18. V_{PFD} (max.) to V_{PFD} (min.) fall time of less than t_F may result in deselection/ write protection not occurring until 20 µs after V_{CC} passes V_{PFD} (min.).

Package Diagrams

28-lead (600-mil) Molded DIP P15

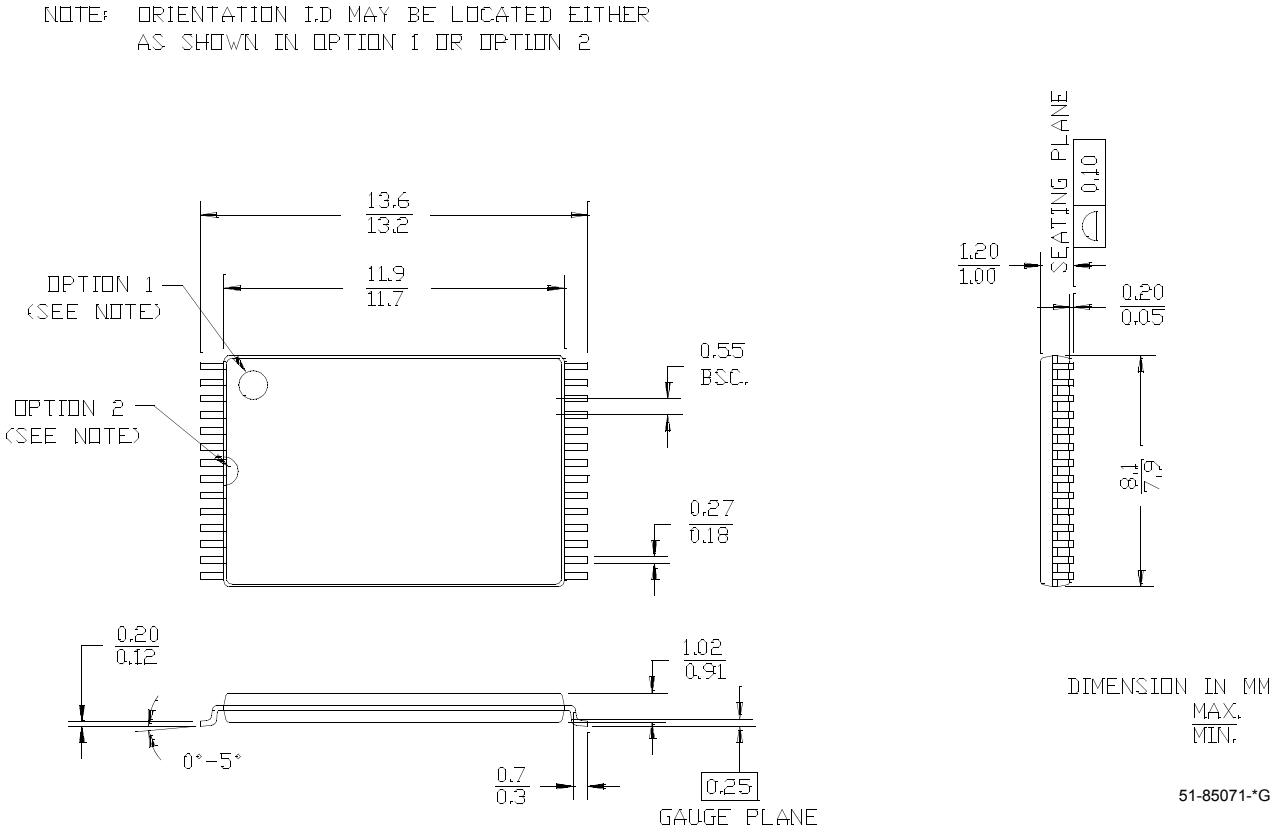


28-Lead (300-Mil) Molded SOIC S21

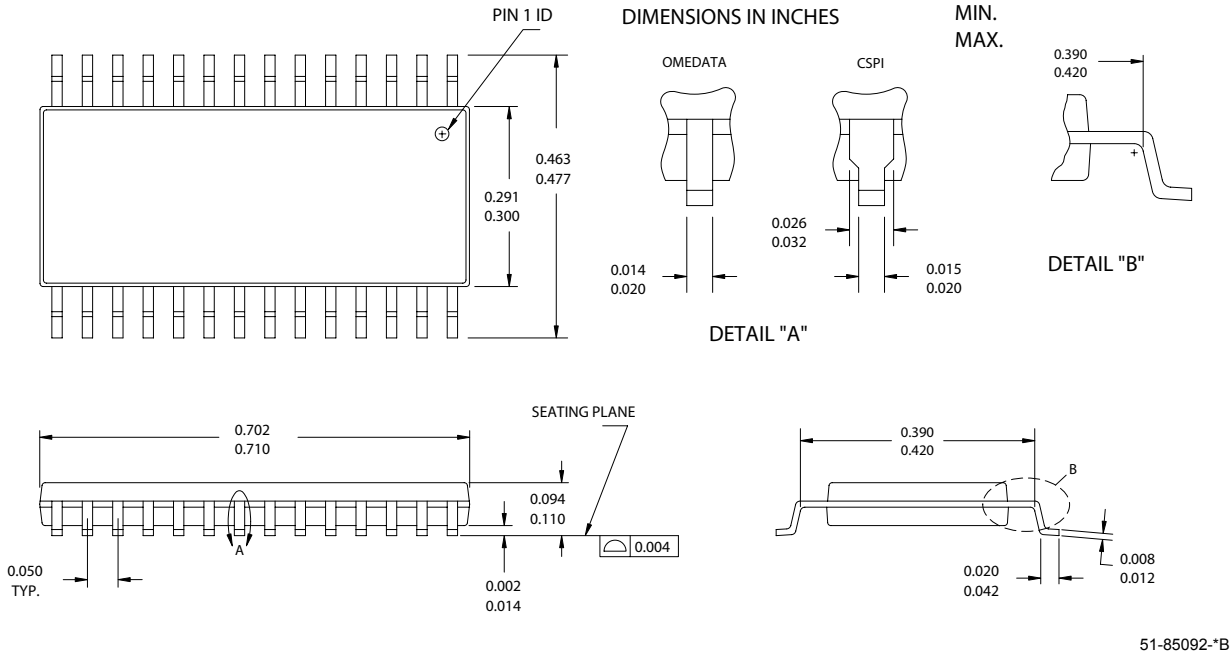


Package Diagrams (continued)

28-lead Thin Small Outline Package Type 1 (8 × 13.4 mm) Z28



450-mil Wide (300-mil Body Width) 28-pin Narrow SOIC (SN28)



Document History Page

Document Title: CY9C62256 32K x 8 Magnetic Nonvolatile CMOS RAM Document Number: 38-15001				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	115831	05/29/02	NBP	New data sheet
*A	116770	07/25/02	NBP	Add state of memory bits at the time of shipment
*B	117612	07/26/02	LJN	Minor Change needed to change footer from 38-15003 to 38-15001
*C	208424	SEE ECN	NBP	Icc, Isb1, Isb2, Non-Operating Shielding Specification, Condition to emulate Boot PROM functionality
*D	227582	SEE ECN	NBP	Changed Magnetic Shielding Specification
*E	285756	SEE ECN	NBP	Added SNC 28-pin SOIC package and Changed V_{PFD} and t_{WP} specification