CY7C4261V/CY7C4271V
CY7C4281V/CY7C4291V

16K/32K/64K/128Kx9 Low Voltage Deep Sync™ FIFOs

Features

- **3.3V operation for low power consumption and easy integration into low voltage systems**
- **High-speed, low-power, first-in first-out (FIFO) memories**
- **16K x 9 (CY7C4261V)**
- **32K x 9 (CY7C4271V)**
- **64K x 9 (CY7C4281V)**
- **128K x 9 (CY7C4291V)**
- **0.35-micron CMOS for optimum speed/power**
- **High-speed 100-MHz operation (10 ns read/write cycle times)**
- **Low power**
  - **— I_{CC} = 25 mA**
  - **— I_{SB} = 4 mA**
- **Fully asynchronous and simultaneous read and write operation**
- **Empty, Full, and programmable Almost Empty and Almost Full status flags**
- **Output Enable ($\overline{OE}$) pin**
- **Independent read and write enable pins**
- **Supports free-running 50% duty cycle clock inputs**
- **Width Expansion capability**
- **32-pin PLCC**
- **Pin-compatible density upgrade to CY7C42X1V family**
- **Pin-compatible 3.3V solutions for CY7C4261/71/81/91**

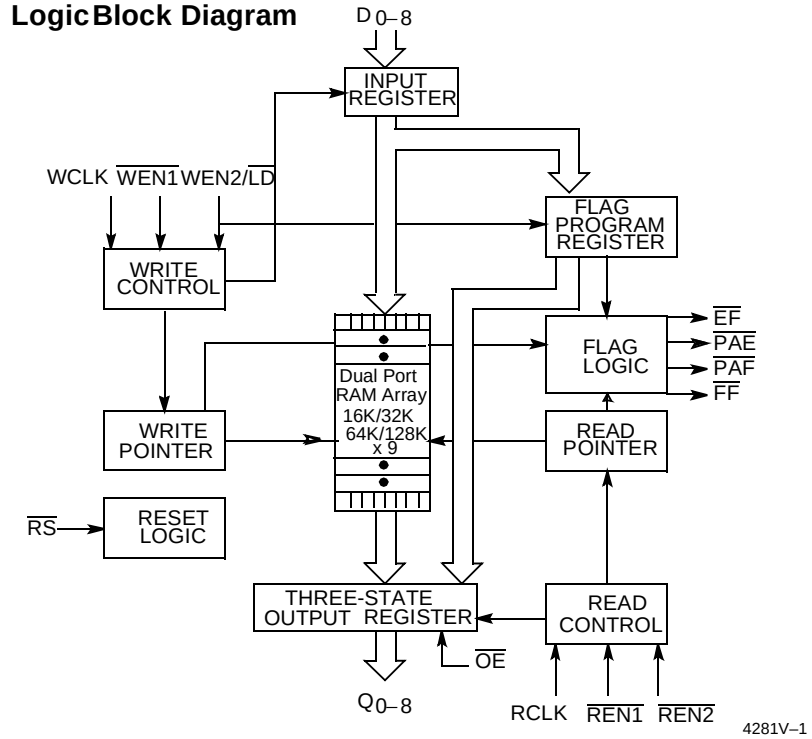
Functional Description

The CY7C4261/71/81/91V are high-speed, low-power, first-in first-out (FIFO) memories with clocked read and write interfaces. All are 9 bits wide. The CY7C4261/71/81/91V are pin-compatible to the CY7C42x1V Synchronous FIFO family. Programmable features include Almost Full/Almost Empty flags. These FIFOs provide solutions for a wide variety of data buffering needs, including high-speed data acquisition, multiprocessor interfaces, and communications buffering.

These FIFOs have 9-bit input and output ports that are controlled by separate clock and enable signals. The input port is controlled by a free-running clock (WCLK) and two write-enable pins ($\overline{WEN1}$, WEN2/$\overline{LD}$).

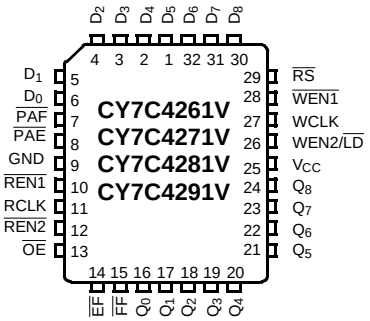
When $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH, data is written into the FIFO on the rising edge of the WCLK signal. While $\overline{WEN1}$ and WEN2/$\overline{LD}$ are held active, data is continually written into the FIFO on each WCLK cycle. The output port is controlled in a similar manner by a free-running read clock (RCLK) and two read enable pins ($\overline{REN1}$, $\overline{REN2}$). In addition, the CY7C4261/71/81/91V has an output enable pin ($\overline{OE}$). The read (RCLK) and write (WCLK) clocks may be tied together for single-clock operation or the two clocks may be run independently for asynchronous read/write applications. Clock frequencies up to 100 MHz are achievable. Depth expansion is possible using one enable input for system control, while the other enable is controlled by expansion logic to direct the flow of data.

Logic Block Diagram



Pin Configuration

PLCC
Top View



Deep Sync is a trademark of Cypress Semiconductor.

Functional Description (continued)

The CY7C4261/71/81/91V provides four status pins: Empty, Full, Programmable Almost Empty, and Programmable Almost Full. The Almost Empty/Almost Full flags are programmable to single word granularity. The programmable flags default to Empty +7 and Full –7.

The flags are synchronous, i.e., they change state relative to either the read clock (RCLK) or the write clock (WCLK). When entering or exiting the Empty and Almost Empty states, the flags are updated exclusively by the RCLK. The flags denoting Almost Full, and Full states are updated exclusively by WCLK. The synchronous flag architecture guarantees that the flags maintain their status for at least one cycle

All configurations are fabricated using an advanced 0.35µ CMOS technology. Input ESD protection is greater than 2001V, and latch-up is prevented by the use of guard rings.

Selection Guide

		7C4261/71/81/91V-10	7C4261/71/81/91V-15	7C4261/71/81/91V-25
Maximum Frequency (MHz)		100	66.7	40
Maximum Access Time (ns)		8	10	15
Minimum Cycle Time (ns)		10	15	25
Minimum Data or Enable Set-Up (ns)		3.5	4	6
Minimum Data or Enable Hold (ns)		0	0	1
Maximum Flag Delay (ns)		8	10	15
Active Power Supply Current (I_{CC1}) (mA)	Commercial	25	25	25
	Industrial		30	

	CY7C4261V	CY7C4271V	CY7C4281V	CY7C4291V
Density	16k x 9	32k x 9	64k x 9	128k x 9
Package	32-pin PLCC	32-pin PLCC	32-pin PLCC	32-pin PLCC

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential..... –0.5V to +3.6V

DC Voltage Applied to Outputs in High Z State ..... –0.5V to V_{CC}+0.5V

DC Input Voltage ..... –0.5V to V_{CC}+0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}[1]
Commercial	0°C to +70°C	3.3V ±300 mV
Industrial	–40°C to +85°C	3.3V ±300 mV

Pin Definitions

Signal Name	Description	I/O	Description
D_{0-8}	Data Inputs	I	Data Inputs for 9-bit bus
Q_{0-8}	Data Outputs	O	Data Outputs for 9-bit bus
$\overline{WEN1}$	Write Enable 1	I	The only write enable when device is configured to have programmable flags. Data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is asserted and $\overline{FF}$ is HIGH. If the FIFO is configured to have two write enables, data is written on a LOW-to-HIGH transition of WCLK when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ and $\overline{FF}$ are HIGH.
WEN2/$\overline{LD}$ Dual Mode Pin	Write Enable 2 Load	I	If HIGH at reset, this pin operates as a second write enable. If LOW at reset, this pin operates as a control to write or read the programmable flag offsets. $\overline{WEN1}$ must be LOW and WEN2 must be HIGH to write data into the FIFO. Data will not be written into the FIFO if the $\overline{FF}$ is LOW. If the FIFO is configured to have programmable flags, WEN2/$\overline{LD}$ is held LOW to write or read the programmable flag offsets.
$\overline{REN1}$, $\overline{REN2}$	Read Enable Inputs	I	Enables the device for Read operation. Both $\overline{REN1}$ and $\overline{REN2}$ must be asserted to allow a read operation.
WCLK	Write Clock	I	The rising edge clocks data into the FIFO when $\overline{WEN1}$ is LOW and WEN2/$\overline{LD}$ is HIGH and the FIFO is not Full. When $\overline{LD}$ is asserted, WCLK writes data into the programmable flag-offset register.
RCLK	Read Clock	I	The rising edge clocks data out of the FIFO when $\overline{REN1}$ and $\overline{REN2}$ are LOW and the FIFO is not Empty. When WEN2/$\overline{LD}$ is LOW, RCLK reads data out of the programmable flag-offset register.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ is LOW, the FIFO is empty. $\overline{EF}$ is synchronized to RCLK.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full. $\overline{FF}$ is synchronized to WCLK.
$\overline{PAE}$	Programmable Almost Empty	O	When $\overline{PAE}$ is LOW, the FIFO is almost empty based on the almost empty offset value programmed into the FIFO. $\overline{PAE}$ is synchronized to RCLK.
$\overline{PAF}$	Programmable Almost Full	O	When $\overline{PAF}$ is LOW, the FIFO is almost full based on the almost full offset value programmed into the FIFO. $\overline{PAF}$ is synchronized to WCLK.
$\overline{RS}$	Reset	I	Resets device to empty condition. A reset is required before an initial read or write operation after power-up.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in High Z (high-impedance) state.

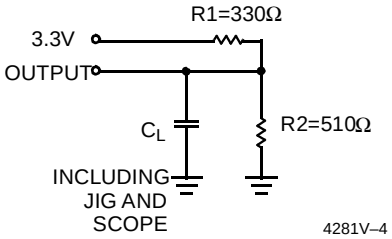
Electrical Characteristics Over the Operating Range

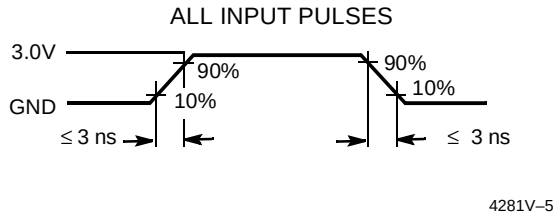
Parameter	Description	Test Conditions		7C4261/71/81/91V -10		7C4261/71/81/91V -15		7C4261/71/81/91V -25		Unit
				Min.	Max.	Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –1.0 mA V_{CC} = 3.0V, I_{OH} = –2.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 4.0 mA V_{CC} = 3.0V, I_{OL} = 8.0 mA			.04		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V
V_{IL}	Input LOW Voltage			–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	V_{CC} = Max.		–10	+10	–10	+10	–10	+10	µA
I_{OZL} I_{OZH}	Output OFF, High Z Current	$\overline{OE} \geq V_{IH}$, $V_{SS} < V_O < V_{CC}$		–10	+10	–10	+10	–10	+10	µA
I_{CC1}[2]	Active Power Supply Current		Com'l		25		25		25	mA
			Ind				30			mA
I_{SB}[3]	Average Stand-by Current		Com'l		4		4		4	mA
			Ind				4			mA

Capacitance[4]

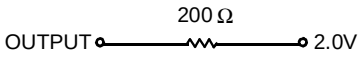
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	5	pF
C_{OUT}	Output Capacitance		7	pF

AC Test Loads and Waveforms (-15 & -25)[5, 6]

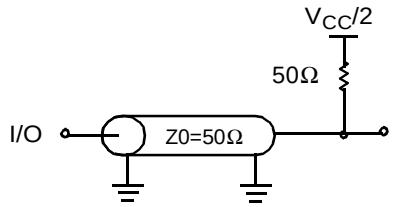


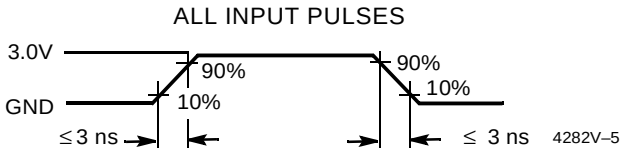


Equivalent to: THÉVENIN EQUIVALENT



AC Test Loads and Waveforms (-10)





Notes:

1. V_{CC} Range for commercial -10 ns is 3.3V ±150mV.
2. Input signals switch from 0V to 3V with a rise/fall time of less than 3 ns, clocks and clock enables switch at maximum frequency of 20 MHz, while data inputs switch at 10 MHz. Outputs are unloaded.)
3. All inputs = V_{CC} – 0.2V, except WCLK and RCLK (which are at frequency = 0 MHz). All outputs are unloaded.
4. Tested initially and after any design or process changes that may affect these parameters.
5. C_L = 30 pF for all AC parameters except for t_{OHZ}.
6. C_L = 5 pF for t_{OHZ}.

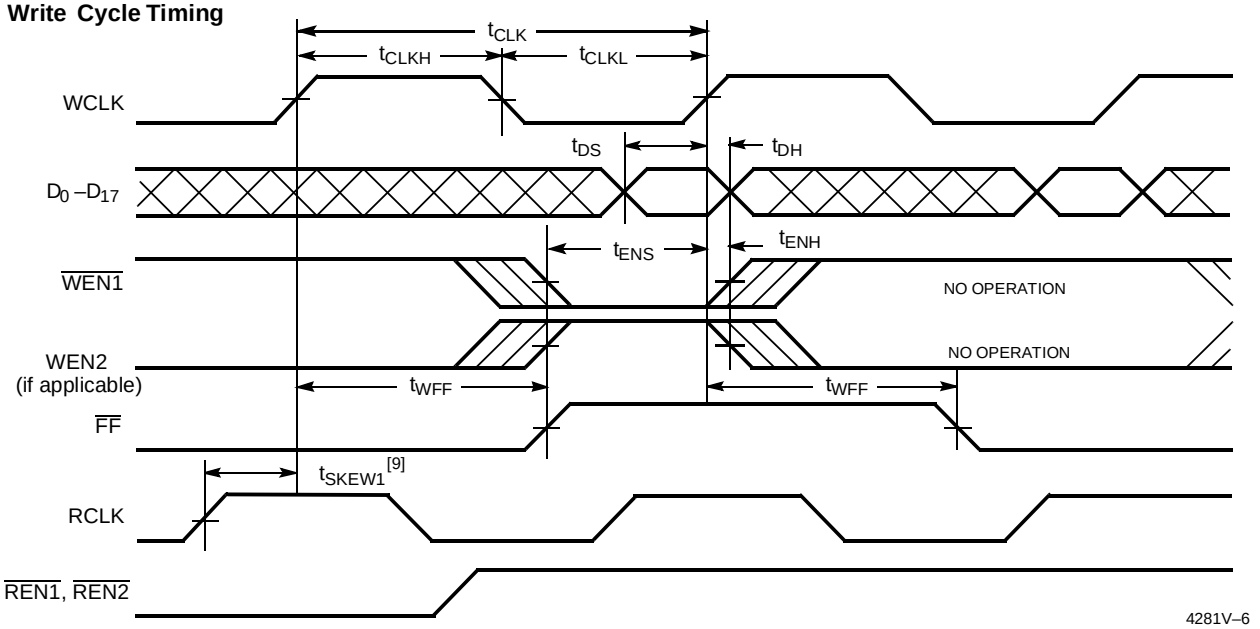
Switching Characteristics Over the Operating Range

Parameter	Description	7C4261/71/81/91V -10		7C4261/71/81/91V -15		7C4261/71/81/91V -25		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_S	Clock Cycle Frequency		100		66.7		40	MHz
t_A	Data Access Time	2	8	2	10	2	15	ns
t_{CLK}	Clock Cycle Time	10		15		25		ns
t_{CLKH}	Clock HIGH Time	4.5		6		10		ns
t_{CLKL}	Clock LOW Time	4.5		6		10		ns
t_{DS}	Data Set-Up Time	3.5		4		6		ns
t_{DH}	Data Hold Time	0		0		1		ns
t_{ENS}	Enable Set-Up Time	3.5		4		6		ns
t_{ENH}	Enable Hold Time	0		0		1		ns
t_{RS}	Reset Pulse Width[7]	10		15		25		ns
t_{RSS}	Reset Set-Up Time	8		10		15		ns
t_{RSR}	Reset Recovery Time	8		10		15		ns
t_{RSF}	Reset to Flag and Output Time		10		15		25	ns
t_{OLZ}	Output Enable to Output in Low Z[8]	0		0		0		ns
t_{OE}	Output Enable to Output Valid	3	7	3	10	3	12	ns
t_{OHZ}	Output Enable to Output in High Z[8]	3	7	3	8	3	12	ns
t_{WFF}	Write Clock to Full Flag		8		10		15	ns
t_{REF}	Read Clock to Empty Flag		8		10		15	ns
t_{PAF}	Clock to Programmable Almost-Full Flag		8		10		15	ns
t_{PAE}	Clock to Programmable Almost-Full Flag		8		10		15	ns
t_{SKEW1}	Skew Time between Read Clock and Write Clock for Empty Flag and Full Flag	5		6		10		ns
t_{SKEW2}	Skew Time between Read Clock and Write Clock for Almost-Empty Flag and Almost-Full Flag	10		15		18		ns

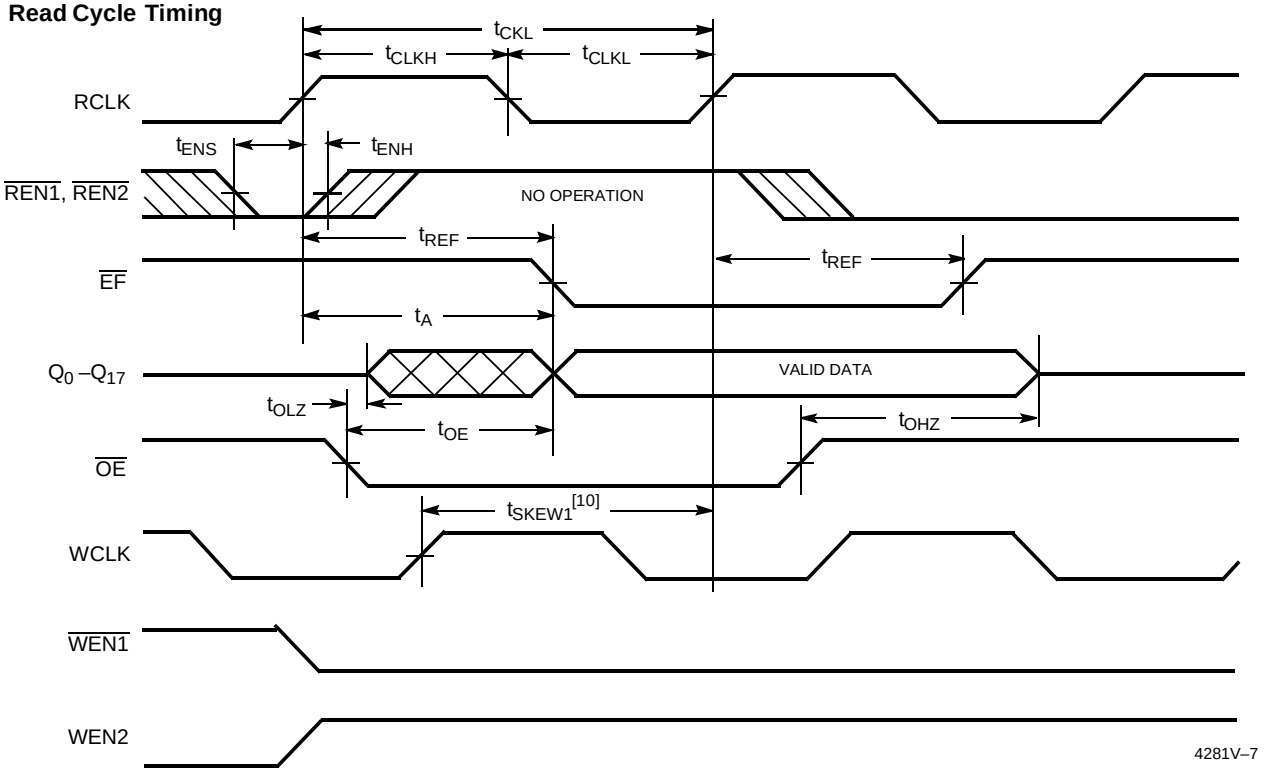
Notes:
7. Pulse widths less than minimum values are not allowed.
8. Values guaranteed by design, not currently tested.

Switching Waveforms

Write Cycle Timing



Read Cycle Timing

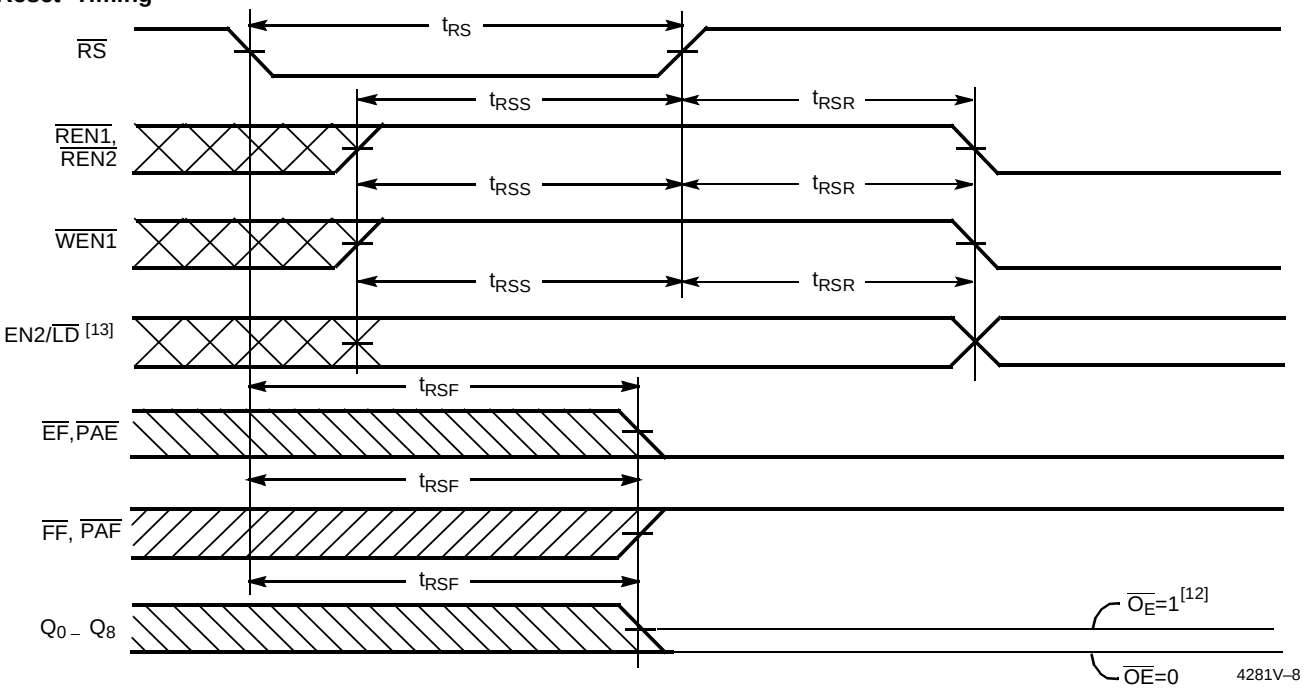


Notes:

9. t_{SKEW1} is the minimum time between a rising RCLK edge and a rising WCLK edge to guarantee that $\overline{FF}$ will go HIGH during the current clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW1}, then $\overline{FF}$ may not change state until the next WCLK rising edge.
10. t_{SKEW1} is the minimum time between a rising WCLK edge and a rising RCLK edge to guarantee that $\overline{EF}$ will go HIGH during the current clock cycle. It the time between the rising edge of WCLK and the rising edge of RCLK is less than t_{SKEW2}, then $\overline{EF}$ may not change state until the next RCLK rising edge.

Switching Waveforms (continued)

Reset Timing[11]

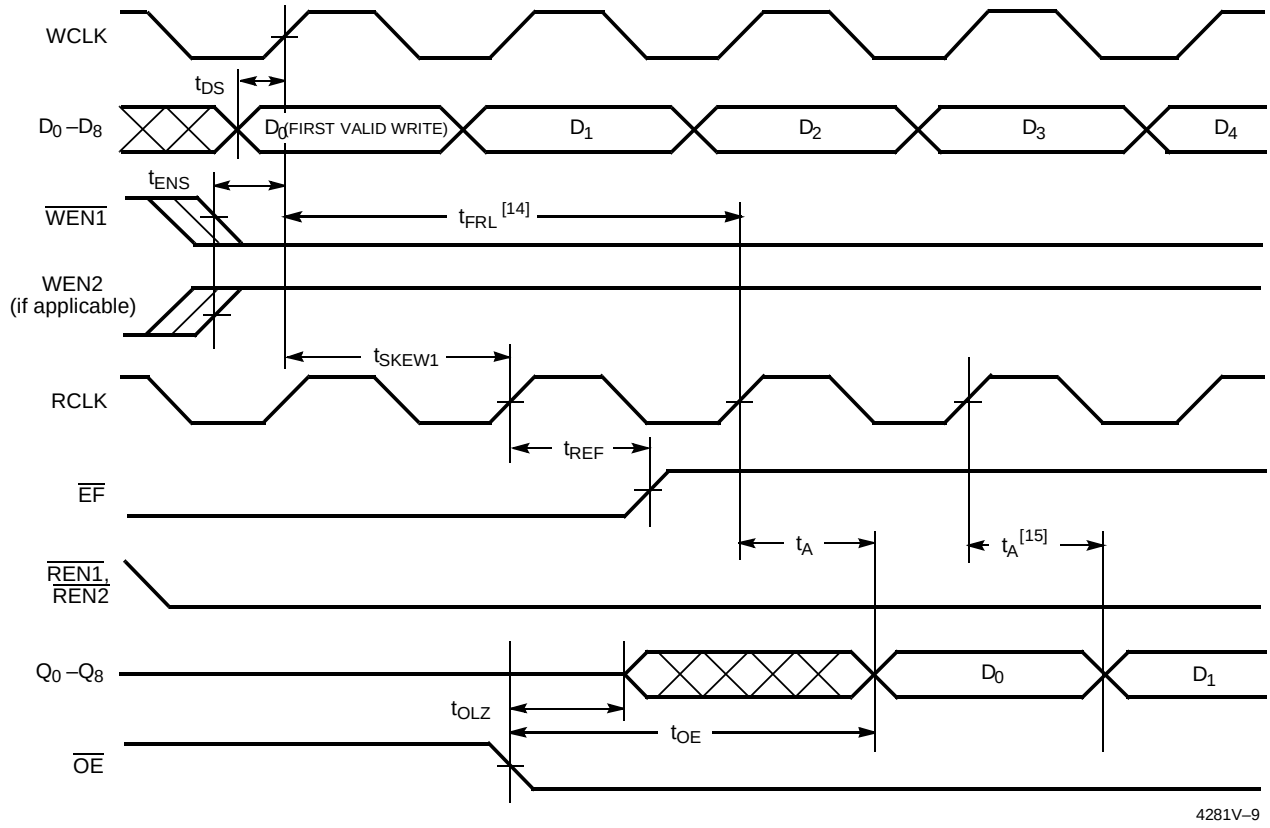


Notes:

11. The clocks (RCLK, WCLK) can be free-running during reset.
12. After reset, the outputs will be LOW if $\overline{OE}$ = 0 and three-state if $\overline{OE}$=1.
13. Holding WEN2/$\overline{LD}$ HIGH during reset will make the pin act as a second enable pin. Holding WEN2/$\overline{LD}$ LOW during reset will make the pin act as a load enable for the programmable flag offset registers.

Switching Waveforms (continued)

First Data Word Latency after Reset with Read and Write

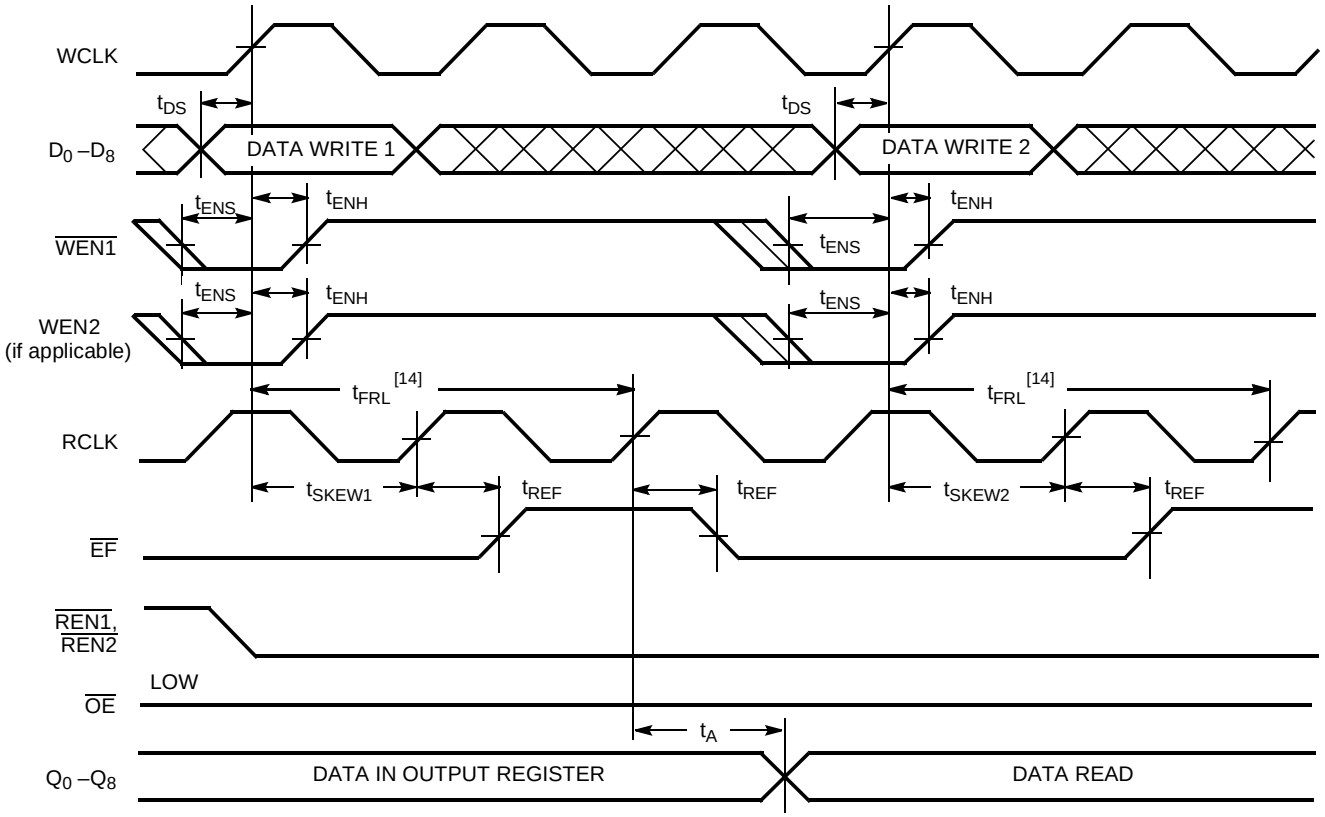


Notes:

14. When $t_{SKEW1} \geq$ minimum specification, t_{FRL} (maximum) = $t_{CLK} + t_{SKEW2}$. When $t_{SKEW1} <$ minimum specification, t_{FRL} (maximum) = either $2*t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$. The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).
15. The first word is available the cycle after $\overline{EF}$ goes HIGH, always.

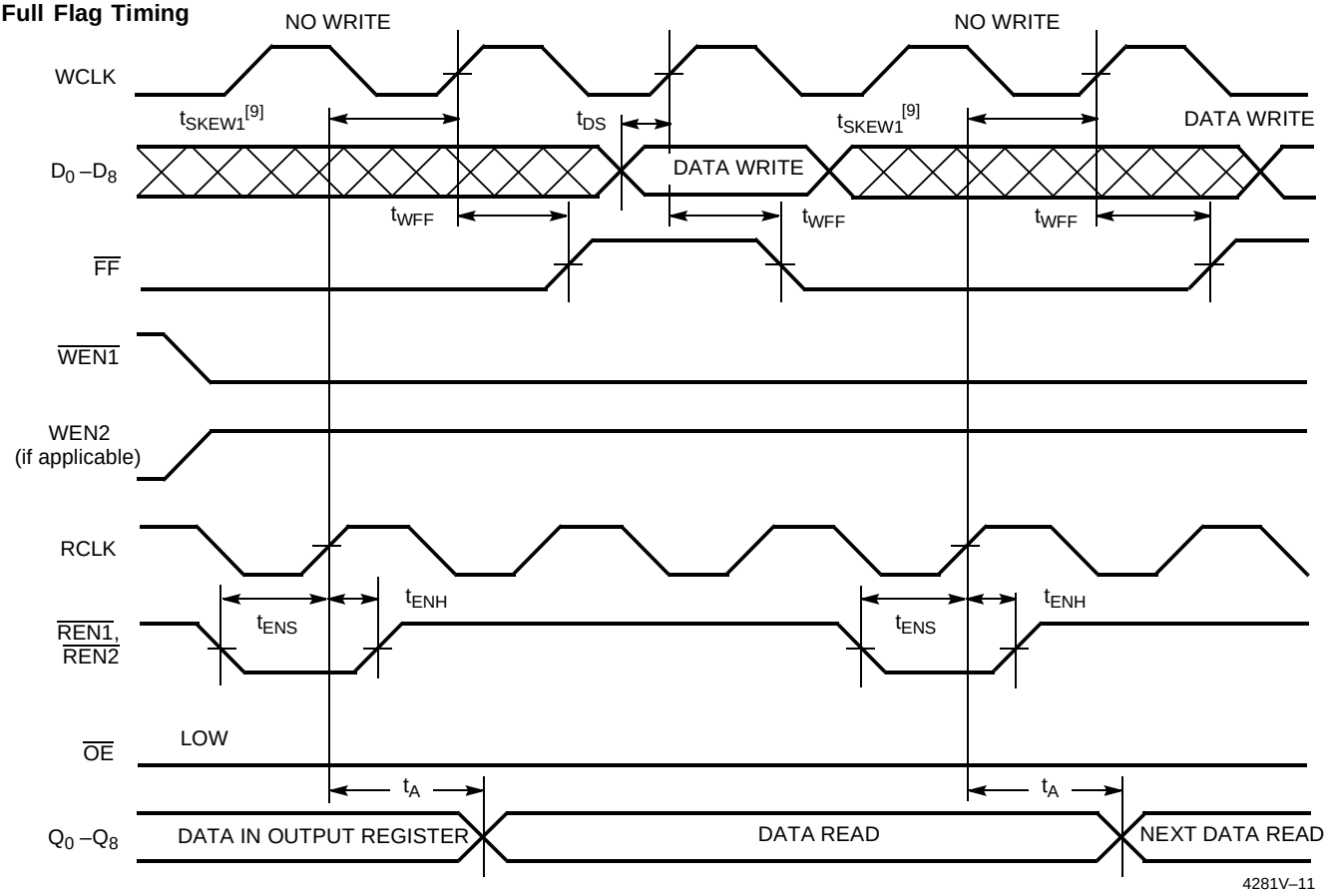
Switching Waveforms (continued)

Empty Flag Timing



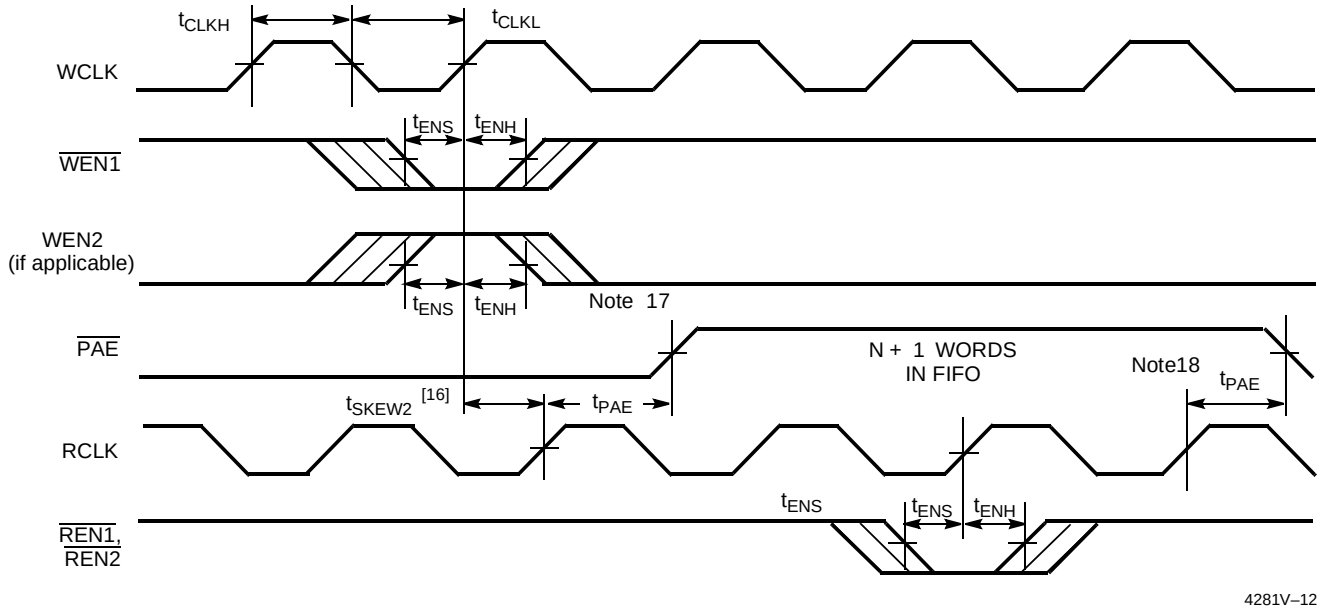
Switching Waveforms (continued)

Full Flag Timing

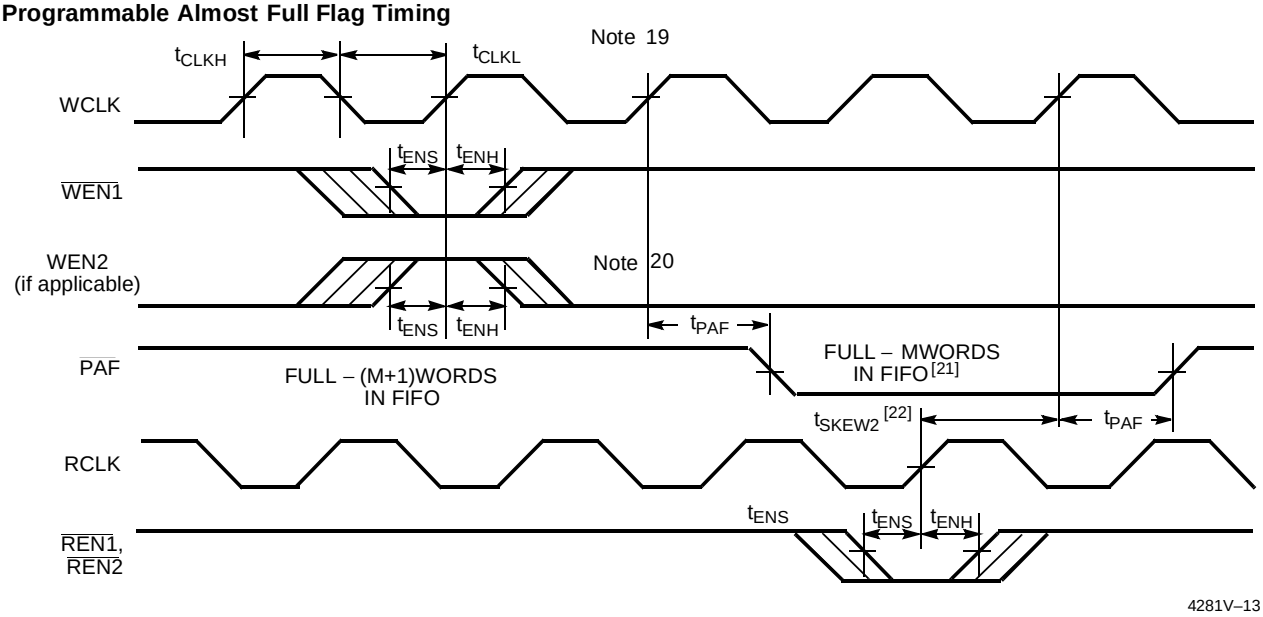


Switching Waveforms (continued)

Programmable Almost Empty Flag Timing



Programmable Almost Full Flag Timing

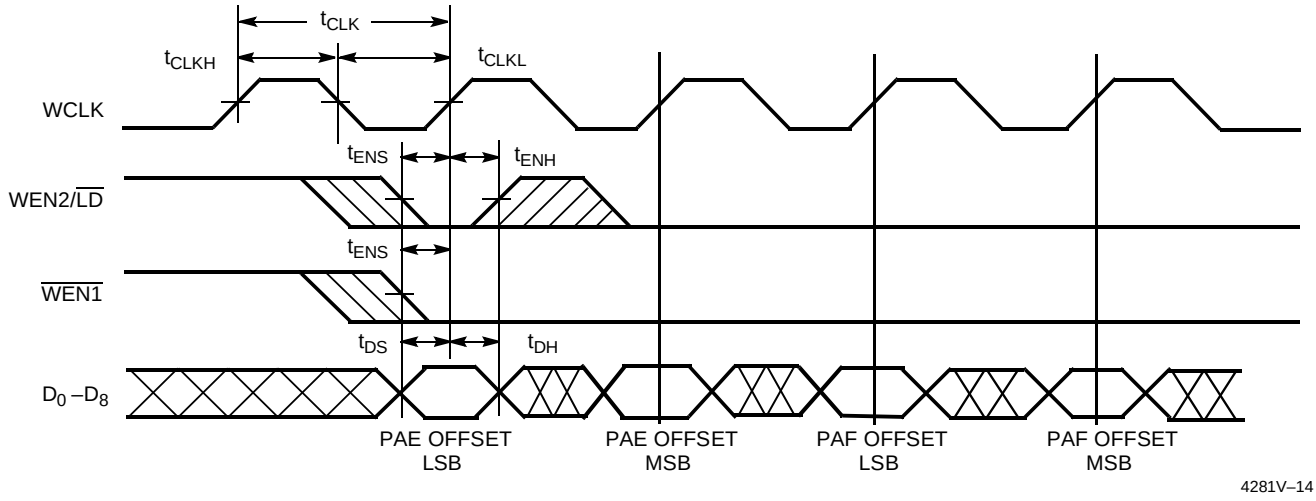


Notes:

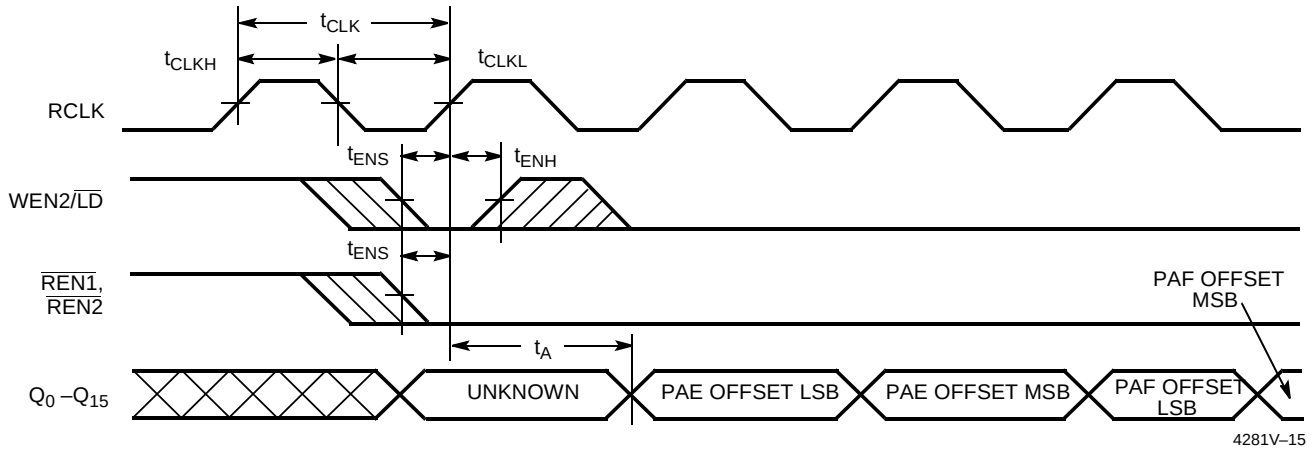
16. t_{SKEW2} is the minimum time between a rising WCLK and a rising RCLK edge for $\overline{PAE}$ to change state during that clock cycle. If the time between the edge of WCLK and the rising RCLK is less than t_{SKEW2}, then $\overline{PAE}$ may not change state until the next RCLK.
17. PAE offset= n.
18. If a read is performed on this rising edge of the read clock, there will be Empty + (n–1) words in the FIFO when $\overline{PAE}$ goes LOW.
19. If a write is performed on this rising edge of the write clock, there will be Full – (m–1) words of the FIFO when $\overline{PAF}$ goes LOW.
20. PAF offset = m.
21. 16K – m words for CY7C4261V, 32K – m words for CY7C4271V, 64K – m words for CY7C4281V, and 128K – m words for CY4291V.
22. t_{SKEW2} is the minimum time between a rising RCLK edge and a rising WCLK edge for $\overline{PAF}$ to change during that clock cycle. If the time between the rising edge of RCLK and the rising edge of WCLK is less than t_{SKEW2}, then $\overline{PAF}$ may not change state until the next WCLK.

Switching Waveforms (continued)

Write Programmable Registers



Read Programmable Registers



Architecture

The CY7C4261/71/81/91V consists of an array of 16k, 32k, 64k, or128k words of 9 bits each (implemented by a dual-port array of SRAM cells), a read pointer, a write pointer, control signals (RCLK, WCLK, $\overline{REN1}$, $\overline{REN2}$, $\overline{WEN1}$, WEN2, $\overline{RS}$), and flags ($\overline{EF}$, $\overline{PAE}$, $\overline{PAF}$, $\overline{FF}$).

Resetting the FIFO

Upon power-up, the FIFO must be reset with a Reset ($\overline{RS}$) cycle. This causes the FIFO to enter the Empty condition signified by $\overline{EF}$ being LOW. All data outputs ($Q_{0–8}$) go LOW t_{RSF} after the rising edge of $\overline{RS}$. In order for the FIFO to reset to its default state, the user must not read or write while $\overline{RS}$ is LOW. All flags are guaranteed to be valid t_{RSF} after $\overline{RS}$ is taken LOW.

FIFO Operation

When the $\overline{WEN1}$ signal is active LOW, WEN2 is active HIGH, and $\overline{FF}$ is active HIGH, data present on the $D_{0–8}$ pins is written into the FIFO on each rising edge of the WCLK signal. Similarly, when the $\overline{REN1}$ and $\overline{REN2}$ signals are active LOW and $\overline{EF}$ is active HIGH, data in the FIFO memory will be presented on the $Q_{0–8}$ outputs. New data will be presented on each rising edge of RCLK while $\overline{REN1}$ and $\overline{REN2}$ are active. $\overline{REN1}$ and $\overline{REN2}$ must set up t_{ENS} before RCLK for it to be a valid read function. $\overline{WEN1}$ and WEN2 must occur t_{ENS} before WCLK for it to be a valid write function.

An output enable ($\overline{OE}$) pin is provided to three-state the $Q_{0–8}$ outputs when $\overline{OE}$ is asserted. When $\overline{OE}$ is enabled (LOW), data in the output register will be available to the $Q_{0–8}$ outputs after t_{OE}. If devices are cascaded, the $\overline{OE}$ function will only output data on the FIFO that is read enabled.

The FIFO contains overflow circuitry to disallow additional writes when the FIFO is full, and underflow circuitry to disallow additional reads when the FIFO is empty. An empty FIFO maintains the data of the last valid read on its $Q_{0–8}$ outputs even after additional reads occur.

Write Enable 1 ($\overline{WEN1}$) - If the FIFO is configured for programmable flags, Write Enable 1 ($\overline{WEN1}$) is the only write enable control pin. In this configuration, when Write Enable 1 ($\overline{WEN1}$) is LOW, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored is the RAM array sequentially and independently of any on-going read operation.

Write Enable 2/Load (WEN2/$\overline{LD}$) - This is a dual-purpose pin. The FIFO is configured at Reset to have programmable flags or to have two write enables, which allows for depth expansion. If Write Enable 2/Load (WEN2/$\overline{LD}$) is set active HIGH at Reset ($\overline{RS}$=LOW), this pin operates as a second write enable pin.

If the FIFO is configured to have two write enables, when Write Enable ($\overline{WEN1}$) is LOW and Write Enable 2/Load (WEN2/$\overline{LD}$) is HIGH, data can be loaded into the input register and RAM array on the LOW-to-HIGH transition of every write clock (WCLK). Data is stored in the RAM array sequentially and independently of any on-going read operation.

Programming

When WEN2/$\overline{LD}$ is held LOW during Reset, this pin is the load ($\overline{LD}$) enable for flag offset programming. In this configuration, WEN2/$\overline{LD}$ can be used to access the four 9-bit offset registers contained in the CY7C4261/71/81/91V for writing or reading data to these registers.

When the device is configured for programmable flags and both WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW, the first LOW-to-HIGH transition of WCLK writes data from the data inputs to the empty offset least significant bit (LSB) register. The second, third, and fourth LOW-to-HIGH transitions of WCLK store data in the empty offset most significant bit (MSB) register, full offset LSB register, and full offset MSB register, respectively, when WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW. The fifth LOW-to-HIGH transition of WCLK while WEN2/$\overline{LD}$ and $\overline{WEN1}$ are LOW writes data to the empty LSB register again. *Figure 1* shows the registers sizes and default values for the various device types.

It is not necessary to write to all the offset registers at one time. A subset of the offset registers can be written; then by bringing the WEN2/$\overline{LD}$ input HIGH, the FIFO is returned to normal read and write operation. The next time WEN2/$\overline{LD}$ is brought LOW, a write operation stores data in the next offset register in sequence.

The contents of the offset registers can be read to the data outputs when WEN2/$\overline{LD}$ is LOW and both $\overline{REN1}$ and $\overline{REN2}$ are LOW. LOW-to-HIGH transitions of RCLK read register contents to the data outputs. Writes and reads should not be performed simultaneously on the offset registers.

Programmable Flag ($\overline{PAE}$, $\overline{PAF}$) Operation

Whether the flag offset registers are programmed as described in *Table 1* or the default values are used, the programmable almost-empty flag ($\overline{PAE}$) and programmable almost-full flag ($\overline{PAF}$) states are determined by their corresponding offset registers and the difference between the read and write pointers.

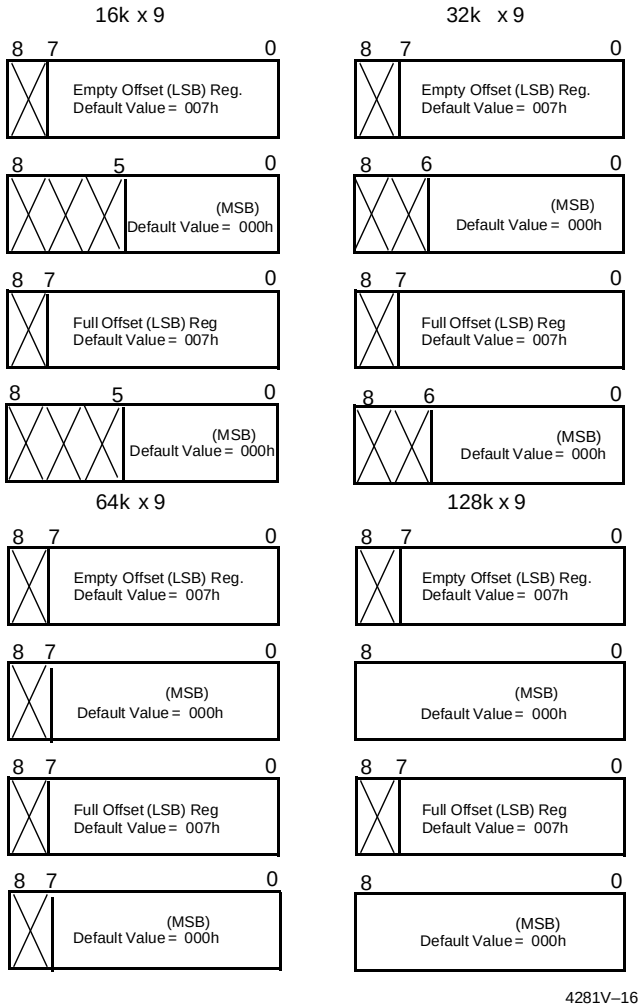


Figure 1. Offset Register Location and Default Values

Table 1. Writing the Offset Registers

$\overline{LD}$	$\overline{WEN}$	WCLK[24]	Selection
0	0		Empty Offset (LSB) Empty Offset (MSB) Full Offset (LSB) Full Offset (MSB)
0	1		No Operation
1	0		Write Into FIFO
1	1		No Operation

The number formed by the empty offset least significant bit register and empty offset most significant bit register is referred to as *n* and determines the operation of $\overline{PAE}$. $\overline{PAF}$ is synchronized to the LOW-to-HIGH transition of RCLK by one flip-flop and is LOW when the FIFO contains n or fewer unread words. $\overline{PAE}$ is set HIGH by the LOW-to-HIGH transition of RCLK when the FIFO contains (n+1) or greater unread words.

The number formed by the full offset least significant bit register and full offset most significant bit register is referred to as *m* and determines the operation of $\overline{PAF}$. $\overline{PAE}$ is synchronized to the LOW-to-HIGH transition of WCLK by one flip-flop and is set LOW when the number of unread words in the FIFO is greater than or equal to CY7C4261V (16k – m), CY7C4271V (32k – m), CY7C4281V (64k – m) and CY7C4291V (128k – m). $\overline{PAF}$ is set HIGH by the LOW-to-HIGH transition of WCLK when the number of available memory locations is greater than m.

Table 2. Status Flags

Number of Words in FIFO				$\overline{FF}$	$\overline{PAF}$	$\overline{PAE}$	$\overline{EF}$
CY7C4261V	CY7C4271V	CY7C4281V	CY7C4291V				
0	0	0	0	H	H	L	L
1 to n[24]	1 to n[24]	1 to n[24]	1 to n[24]	H	H	L	H
(n+1) to (1638 – (m+1))	(n+1) to (32768 – (m+1))	(n+1) to (65536 – (m+1))	(n+1) to (131072– (m+1))	H	H	H	H
(16384 – m)[25] to 16383	(32768 – m)[25] to 32767	(65536 – m)[25] to 65535	(131072 – m)[25] to 131071	H	L	H	H
16384	32768	65536	131072	L	L	H	H

Notes:
23. The same selection sequence applies to reading from the registers. $\overline{REN1}$ and $\overline{REN2}$ are enabled and a read is performed on the LOW-to-HIGH transition of RCLK
24. n = Empty Offset (n=7 default value).
25. m = Full Offset (m=7 default value).

Width Expansion Configuration

Word width may be increased simply by connecting the corresponding input controls signals of multiple devices. A composite flag should be created for each of the end-point status flags ($\overline{EF}$ and $\overline{FF}$). The partial status flags ($\overline{PAE}$ and $\overline{PAF}$) can be detected from any one device. *Figure 2* demonstrates a 18-bit word width by using two CY7C42x1Vs. Any word width can be attained by adding additional CY7C42x1Vs.

When the CY7C42x1V is in a Width Expansion Configuration, the Read Enable ($\overline{REN2}$) control input can be grounded (See *Figure 2*). In this configuration, the Write Enable 2/Load (WEN2/$\overline{LD}$) pin is set to LOW at Reset so that the pin operates as a control to load and read the programmable flag offsets.

Flag Operation

The CY7C4261/71/81/91V devices provide five flag pins to indicate the condition of the FIFO contents. Empty, Full, $\overline{PAE}$, and $\overline{PAF}$ are synchronous.

Full Flag

The Full Flag ($\overline{FF}$) will go LOW when the device is full. Write operations are inhibited whenever $\overline{FF}$ is LOW regardless of the state of $\overline{WEN1}$ and WEN2/$\overline{LD}$. $\overline{FF}$ is synchronized to WCLK, i.e., it is exclusively updated by each rising edge of WCLK.

Empty Flag

The Empty Flag ($\overline{EF}$) will go LOW when the device is empty. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the state of $\overline{REN1}$ and $\overline{REN2}$. $\overline{EF}$ is synchronized to RCLK, i.e., it is exclusively updated by each rising edge of RCLK.

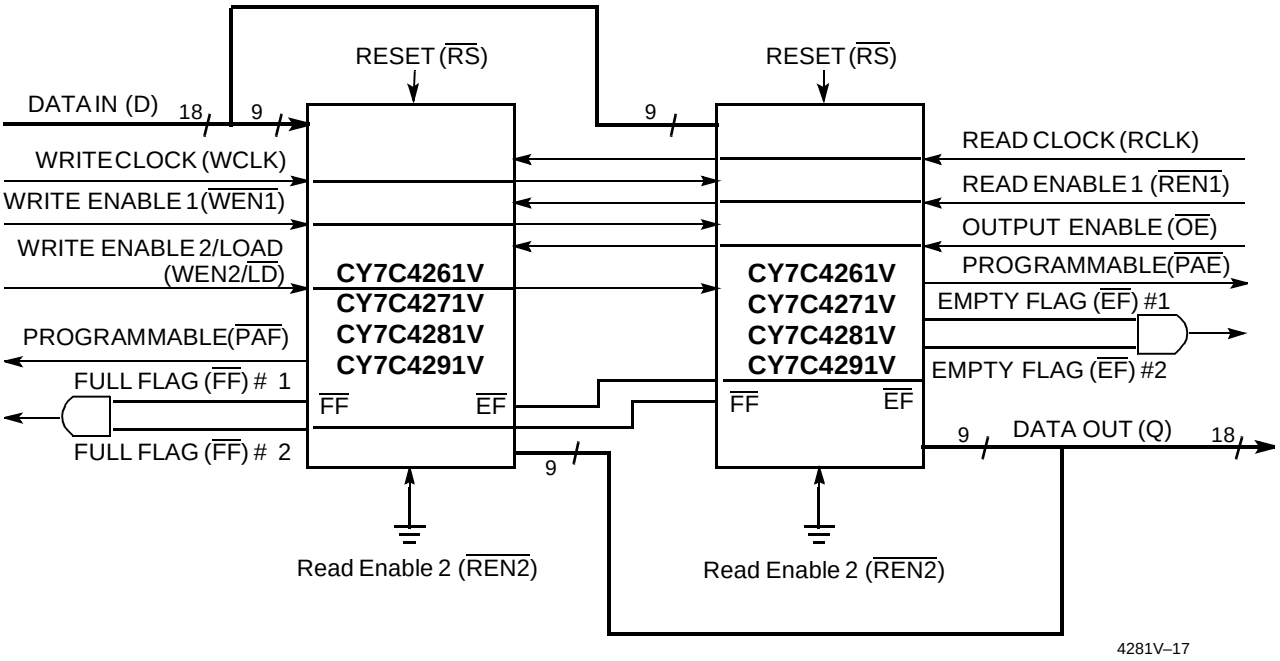


Figure 2. Block Diagram of 16k/32k/64k/128k x 9 Low Voltage Deep Sync FIFO Memory Used in a Width Expansion Configuration

Ordering Information

16Kx9 Low Voltage Deep Sync FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4261V-10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
15	CY7C4261V-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C4261V-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
25	CY7C4261V-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial

32Kx9 Low Voltage Deep Sync FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4271V-10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
15	CY7C4271V-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C4271V-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
25	CY7C4271V-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial

64kx9 Low Voltage Deep Sync FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4281V-10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
15	CY7C4281V-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C4281V-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
25	CY7C4281V-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial

Ordering Information

128kx9 Low Voltage Deep Sync FIFO

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C4291V-10JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
15	CY7C4291V-15JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial
	CY7C4291V-15JI	J65	32-Lead Plastic Leaded Chip Carrier	Industrial
25	CY7C4291V-25JC	J65	32-Lead Plastic Leaded Chip Carrier	Commercial

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Package Diagram

32-Lead Plastic Leaded Chip Carrier J65