Ultra Low Power/Voltage CMOS SRAM
256K X 8 bit

BS62UV2006

■ FEATURES

- Wide Vcc operation voltage :
  C-grade: 1.8V~3.6V
  I-grade: 1.9V~3.6V
  (Vcc_min.=1.65V at 25ºC)
- Ultra low power consumption :
  Vcc = 2.0V C-grade : 8mA (Max.) operating current
  I- grade : 10mA (Max.) operating current
  0.20uA (Typ.) CMOS standby current
  Vcc = 3.0V C-grade : 11mA (Max.) operating current
  I- grade : 13mA (Max.) operating current
  0.30uA (Typ.) CMOS standby current
- High speed access time :
  -85 85ns (Max.)
  -10 100ns (Max.)
- Automatic power down when chip is deselected
- Three state outputs and TTL compatible
- Fully static operation
- Data retention supply voltage as low as 1.0V
- Easy expansion with CE2, $\overline{CE1}$, and $\overline{OE}$ options

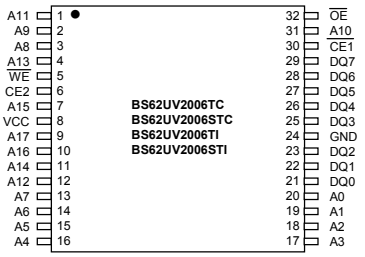
■ DESCRIPTION

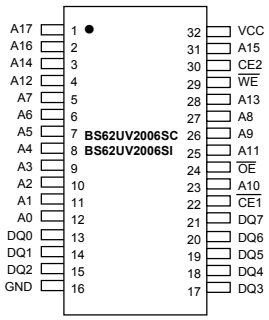
The BS62UV2006 is a high performance, ultra low power CMOS Static Random Access Memory organized as 262,144 words by 8 bits and operates from a wide range of 1.8V to 3.6V supply voltage.
Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.2uA at 2.0V/25ºC and maximum access time of 85ns at 85ºC.
Easy memory expansion is provided by an active LOW chip enable ($\overline{CE1}$), an active HIGH chip enable (CE2), and active LOW output enable ($\overline{OE}$) and three-state output drivers.
The BS62UV2006 has an automatic power down feature, reducing the power consumption significantly when chip is deselected.
The BS62UV2006 is available in DICE form, JEDEC standard 32 pin 450mil Plastic SOP, 8mmx13.4mm STSOP and 8mmx20mm TSOP.

■ PRODUCT FAMILY

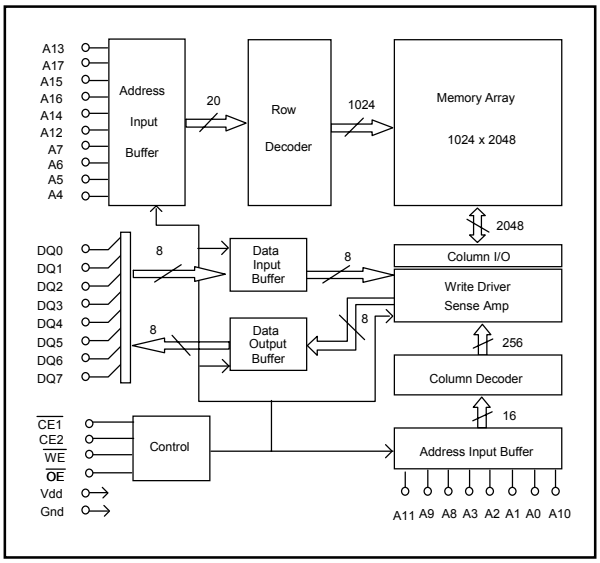
PRODUCT FAMILY	OPERATING TEMPERATURE	Vcc RANGE	SPEED (ns)	POWER DISSIPATION				PKG TYPE
				STANDBY (I_{CCSB1}, Max)		Operating (I_{CC}, Max)		
			C-grade:1.8~3.6V I-grade:1.9~3.6V	Vcc=3.0V	Vcc=2.0V	Vcc=3.0V	Vcc=2.0V	
BS62UV2006DC	+0 ºC to +70 ºC	1.8V ~3.6V	85/100	3.0uA	2.0uA	11mA	8mA	DICE
BS62UV2006TC								TSOP-32
BS62UV2006STC								STSOP-32
BS62UV2006SC								SOP-32
BS62UV2006DI	-40 ºC to +85 ºC	1.9V ~ 3.6V	85/100	5.0uA	3.0uA	13mA	10mA	DICE
BS62UV2006TI								TSOP-32
BS62UV2006STI								STSOP-32
BS62UV2006SI								SOP-32

■ PIN CONFIGURATIONS





■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

Name	Function
A0-A17 Address Input	These 18 address inputs select one of the 262,144 x 8-bit words in the RAM
$\overline{CE1}$ Chip Enable 1 Input **CE2 Chip Enable 2 Input**	$\overline{CE1}$ is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and is in a standby power mode. The DQ pins will be in the high impedance state when the device is deselected.
$\overline{WE}$ Write Enable Input	The write enable input is active LOW and controls read and write operations. With the chip selected, when $\overline{WE}$ is HIGH and $\overline{OE}$ is LOW, output data will be present on the DQ pins; when $\overline{WE}$ is LOW, the data present on the DQ pins will be written into the selected memory location.
$\overline{OE}$ Output Enable Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when $\overline{OE}$ is inactive.
DQ0-DQ7 Data Input/Output Ports	These 8 bi-directional ports are used to read data from or write data into the RAM.
Vcc	Power Supply
Gnd	Ground

■ TRUTH TABLE

MODE	$\overline{WE}$	$\overline{CE1}$	CE2	$\overline{OE}$	I/O OPERATION	Vcc CURRENT
Not selected (Power Down)	X	H	X	X	High Z	I_{CCSB}, I_{CCSB1}
	X	X	L	X		
Output Disabled	H	L	H	H	High Z	I_{CC}
Read	H	L	H	L	D_{OUT}	I_{CC}
Write	L	L	H	X	D_{IN}	I_{CC}

■ ABSOLUTE MAXIMUM RATINGS(1)

SYMBOL	PARAMETER	RATING	UNITS
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +85	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	20	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ OPERATING RANGE

RANGE	AMBIENT TEMPERATURE	Vcc
Commercial	$0^{O}C$ to $+70^{O}C$	1.8V ~ 3.6V
Industrial	$-40^{O}C$ to $+85^{O}C$	1.9V ~ 3.6V

■ CAPACITANCE (1) (TA = 25ºC, f = 1.0 MHz)

SYMBOL	PARAMETER	CONDITIONS	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

1. This parameter is guaranteed and not 100% tested.

■ DC ELECTRICAL CHARACTERISTICS (TA = -40ºC to + 85ºC)

PARAMETER NAME	PARAMETER	TEST CONDITIONS		MIN.	TYP. (1)	MAX.	UNITS
V_{IL}	Guaranteed Input Low Voltage(2)		Vcc=2.0V	-0.3(5)	--	0.6	V
			Vcc=3.0V		--	0.8	
V_{IH}	Guaranteed Input High Voltage(2)		Vcc=2.0V	1.4	--	Vcc+0.3	V
			Vcc=3.0V	2.0	--		
I_{IL}	Input Leakage Current	Vcc = Max, V_{IN} = 0V to Vcc		--	--	1	uA
I_{LO}	Output Leakage Current	Vcc = Max, $\overline{CE1}$ = V_{IH} or CE2=V_{IL} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0V to Vcc		--	--	1	uA
V_{OL}	Output Low Voltage	Vcc = Max, I_{OL} = 0.1mA	Vcc=2.0V	--	--	0.2	V
		Vcc = Max, I_{OL} = 2.0mA	Vcc=3.0V	--	--	0.4	
V_{OH}	Output High Voltage	Vcc = Min, I_{OH} = -0.1mA	Vcc=2.0V	Vcc-0.2	--	--	V
		Vcc = Min, I_{OH} = -1.0mA	Vcc=3.0V	2.4	--	--	
I_{CC}	Operating Power Supply Current	Vcc = Max, $\overline{CE1}$= V_{IL}, CE2=V_{IH} I_{DQ} = 0mA, F = Fmax(3)	Vcc=2.0V	--	--	10	mA
			Vcc=3.0V	--	--	13	
I_{CCSB}	Standby Current-TTL	Vcc = Max, $\overline{CE1}$ = V_{IH} or CE2=V_{IL} I_{DQ} = 0mA	Vcc=2.0V	--	--	0.1	mA
			Vcc=3.0V	--	--	0.5	
I_{CCSB1}(4)	Standby Current-CMOS	Vcc = Max, $\overline{CE1}$ ≧ Vcc-0.2V or CE2 ≦ 0.2V ; V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	Vcc=2.0V	--	0.20	3.0	uA
			Vcc=3.0V	--	0.30	5.0	

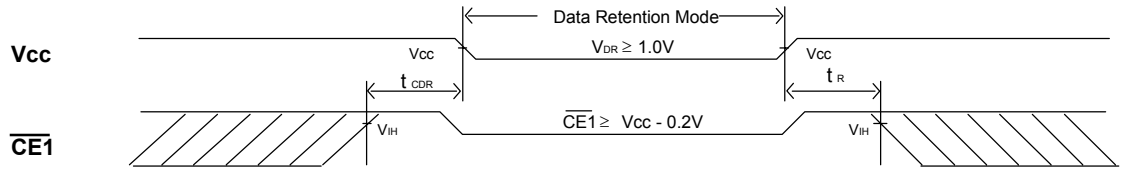
1. Typical characteristics are at TA = 25ºC.
2. These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.
3. Fmax = $1/t_{RC}$. 4. I_{CCSB1} is 2.0uA/3.0uA at Vcc=2.0V/3.0V and TA=70ºC. 5. V_{IL} = -1.5V for pulse width less than 30ns.

■ DATA RETENTION CHARACTERISTICS (TA = -40ºC to + 85ºC)

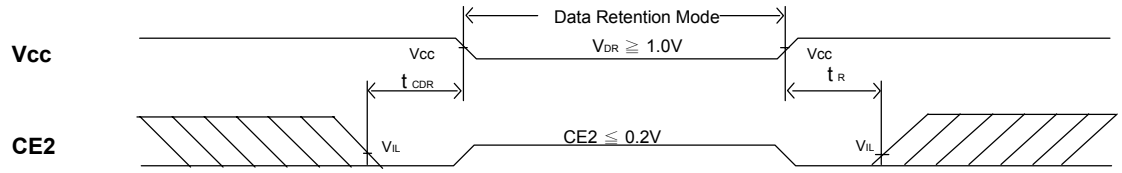
SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP. (1)	MAX.	UNITS
V_{DR}	Vcc for Data Retention	$\overline{CE1}$ ≧ Vcc - 0.2V or CE2 ≦ 0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	1.0	--	--	V
I_{CCDR}(3)	Data Retention Current	$\overline{CE1}$ ≧ Vcc - 0.2V or CE2 ≦ 0.2V, V_{IN} ≧ Vcc - 0.2V or V_{IN} ≦ 0.2V	--	0.1	1.0	uA
t_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0	--	--	ns
t_R	Operation Recovery Time		T_{RC} (2)	--	--	ns

1. Vcc = 1.0V, T_A = + 25ºC
2. t_{RC} = Read Cycle Time
3. I_{CCDR} is 0.7uA at TA=70ºC.

■ LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CE1}$ Controlled)



■ LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)



■AC TEST CONDITIONS

(Test Load and Input/Output Reference)

Input Pulse Levels	Vcc / 0V
Input Rise and Fall Times	1V/ns
Input and Output Timing Reference Level	0.5Vcc
Output Load	C_L = 100pF+1TTL C_L = 30pF+1TTL

■ KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGE : STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF "STATE

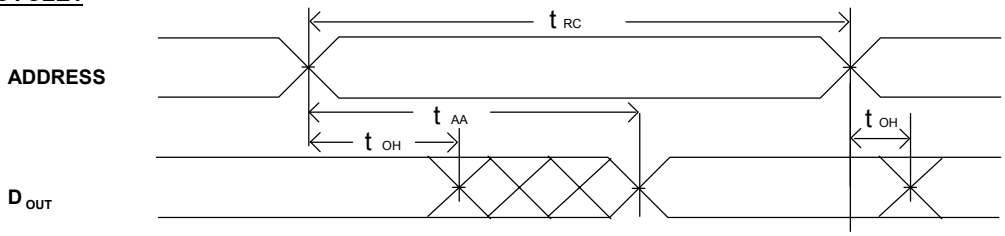
■ AC ELECTRICAL CHARACTERISTICS (TA = -40°C to + 85°C)

READ CYCLE

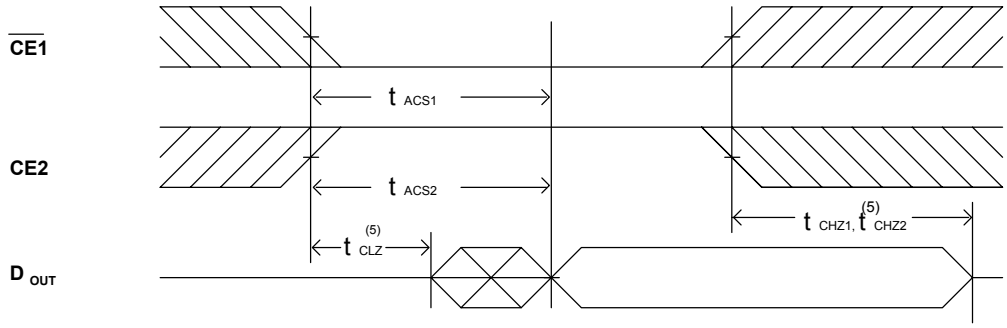
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION		CYCLE TIME : 100ns (Vcc = 1.9~3.6V) MIN.	TYP.	MAX.	CYCLE TIME : 85ns (Vcc = 1.9~3.6V) MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{RC}	Read Cycle Time		100	--	--	85	--	--	ns
t_{AVQV}	t_{AA}	Address Access Time		--	--	100	--	--	85	ns
t_{E1LQV}	t_{ACS1}	Chip Select Access Time	($\overline{CE1}$)	--	--	100	--	--	85	ns
t_{E2HOV}	t_{ACS2}	Chip Select Access Time	(CE2)	--	--	100	--	--	85	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		--	--	45	--	--	40	ns
t_{E1LQX}	t_{CLZ1}	Chip Select to Output Low Z	($\overline{CE1}$)	15	--	--	15	--	--	ns
t_{E2HOX}	t_{CLZ2}	Chip Select to Output Low Z	(CE2)	15	--	--	15	--	--	ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z		15	--	--	10	--	--	ns
t_{E1HQZ}	t_{CHZ1}	Chip Deselect to Output in High Z	($\overline{CE1}$)	--	--	40	--	--	35	ns
t_{E2HQZ}	t_{CHZ2}	Chip Deselect to Output in High Z	(CE2)	--	--	40	--	--	35	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z		--	--	35	--	--	30	ns
t_{AXOX}	t_{OH}	Data Hold from Address Change		15	--	--	15	--	--	ns

■ SWITCHING WAVEFORMS (READ CYCLE)

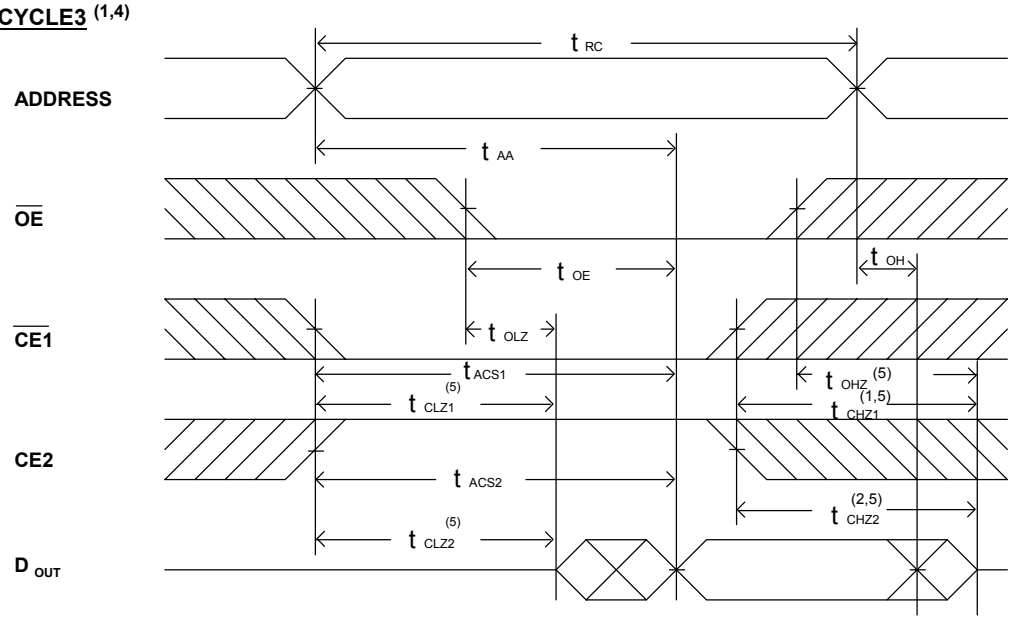
READ CYCLE1 (1,2,4)



READ CYCLE2 (1,3,4)



READ CYCLE3 (1,4)



NOTES:
1. WE is high in read Cycle.
2. Device is continuously selected when $\overline{CE1}$ = V_{IL} and CE2= V_{IH}.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low and/or CE2 transition high.
4. $\overline{OE}$ = V_{IL} .
5. The parameter is guaranteed but not 100% tested.

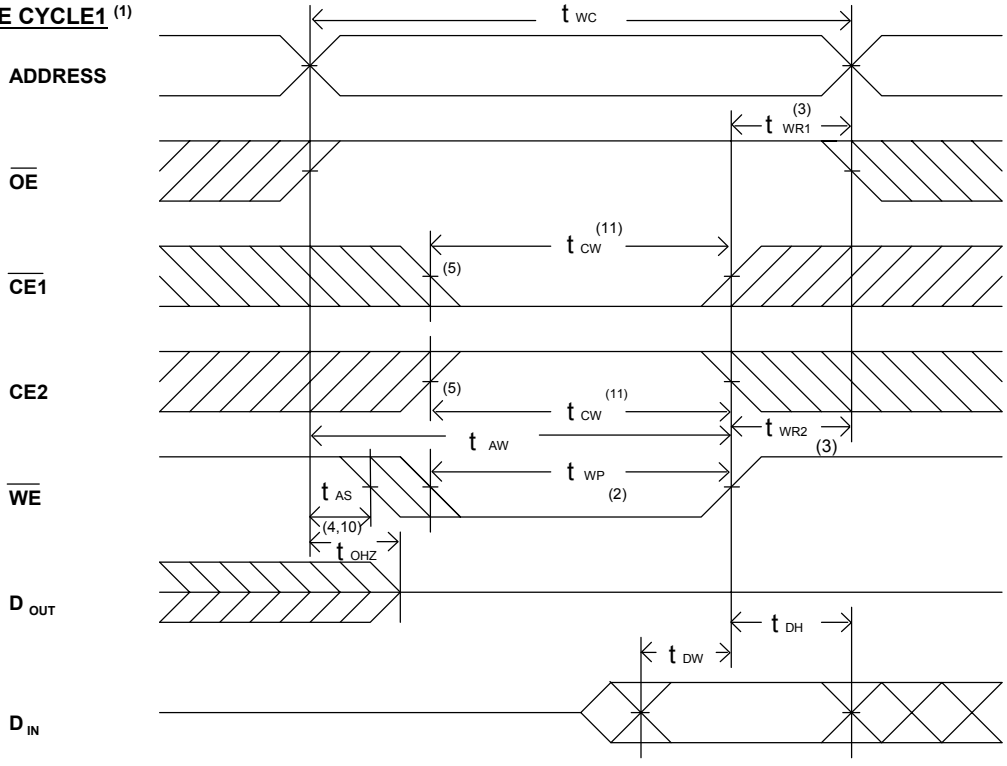
■ AC ELECTRICAL CHARACTERISTICS (TA = -40°C to + 85°C)

WRITE CYCLE

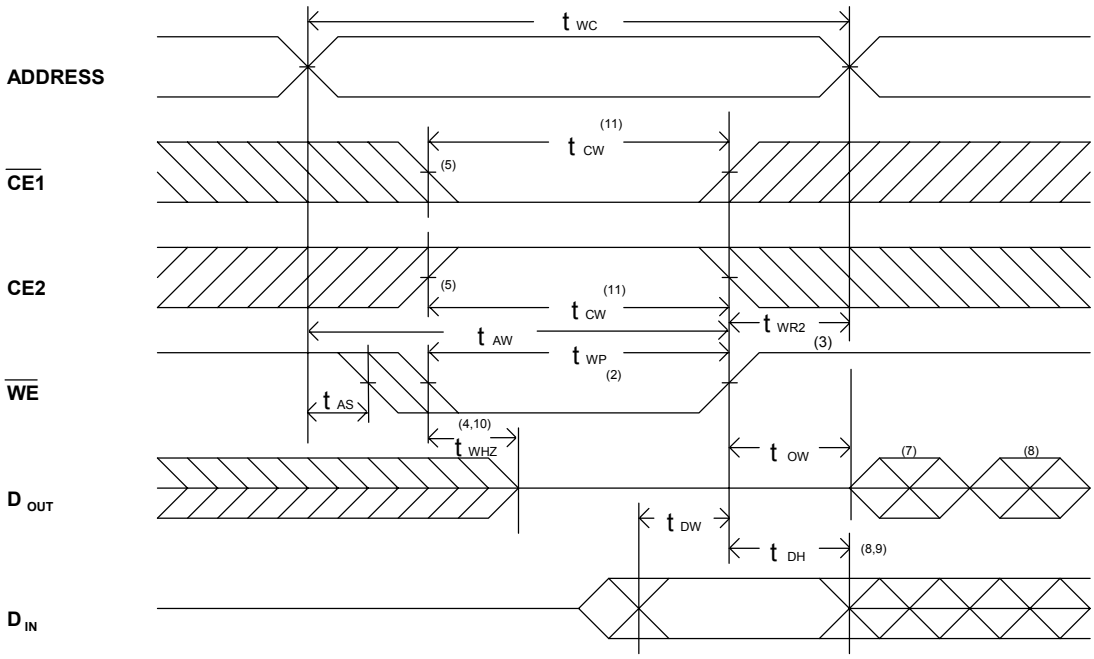
JEDEC PARAMETER NAME	PARAMETER NAME	DESCRIPTION	CYCLE TIME : 100ns (Vcc = 1.9~3.6V) MIN.	TYP.	MAX.	CYCLE TIME : 85ns (Vcc = 1.9~3.6V) MIN.	TYP.	MAX.	UNIT
t_{AVAX}	t_{WC}	Write Cycle Time	100	--	--	85	--	--	ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	100	--	--	85	--	--	ns
t_{AVWL}	t_{AS}	Address Setup Time	0	--	--	0	--	--	ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	100	--	--	85	--	--	ns
t_{WLWH}	t_{WP}	Write Pulse Width	50	--	--	40	--	--	ns
t_{WHAX}	t_{WR1}	Write recovery Time ($\overline{CE1}$,$\overline{WE}$)	0	--	--	0	--	--	ns
t_{E2LAX}	t_{WR2}	Write recovery Time (CE2)	0	--	--	0	--	--	ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z	--	--	40	--	--	35	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	40	--	--	35	--	--	ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0	--	--	0	--	--	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	--	--	40	--	--	35	ns
t_{WHOX}	t_{OW}	End of Write to Output Active	10	--	--	10	--	--	ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

WRITE CYCLE1 (1)



WRITE CYCLE2 (1,6)



NOTES:
1. $\overline{WE}$ must be high during address transitions.
2. The internal write time of the memory is defined by the overlap of $\overline{CE1}$ and CE2 active and $\overline{WE}$ low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.
3. T_{WR} is measured from the earlier of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low at the end of write cycle.
4. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, output remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. D_{OUT} is the read data of next address.
9. If $\overline{CE1}$ is low and CE2 is high during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
10. The parameter is guaranteed but not 100% tested.
11. T_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of write.

■ ORDERING INFORMATION

BS62UV2006 X X Z Y Y

SPEED
85: 85ns
10: 100ns

PKG MATERIAL
-: Normal
G: Green
P: Pb free

GRADE
C: +0°C ~ +70°C
I: -40°C ~ +85°C

PACKAGE
S: SOP
T: TSOP (8mm x 20mm)
ST: Small TSOP (8mm x 13.4mm)
D: DICE

Note:
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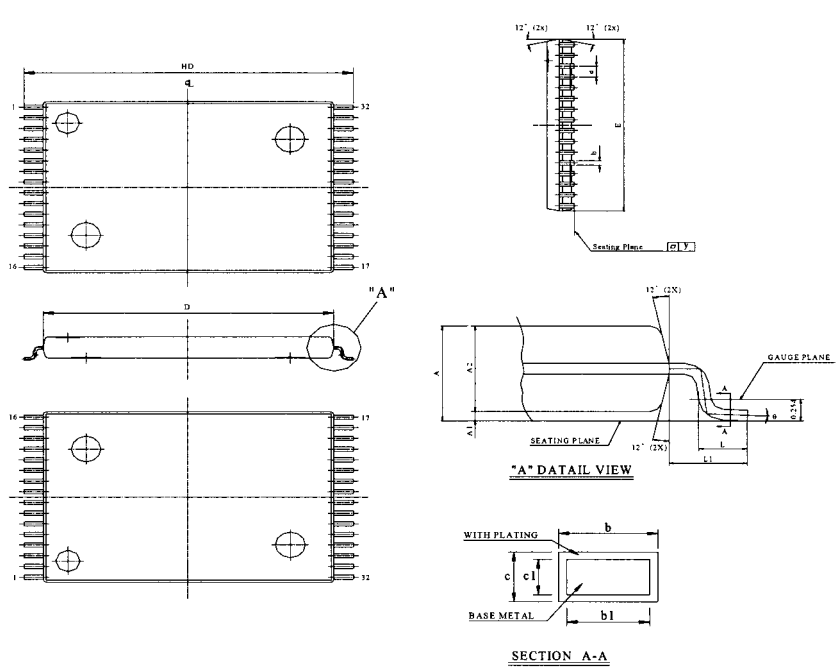
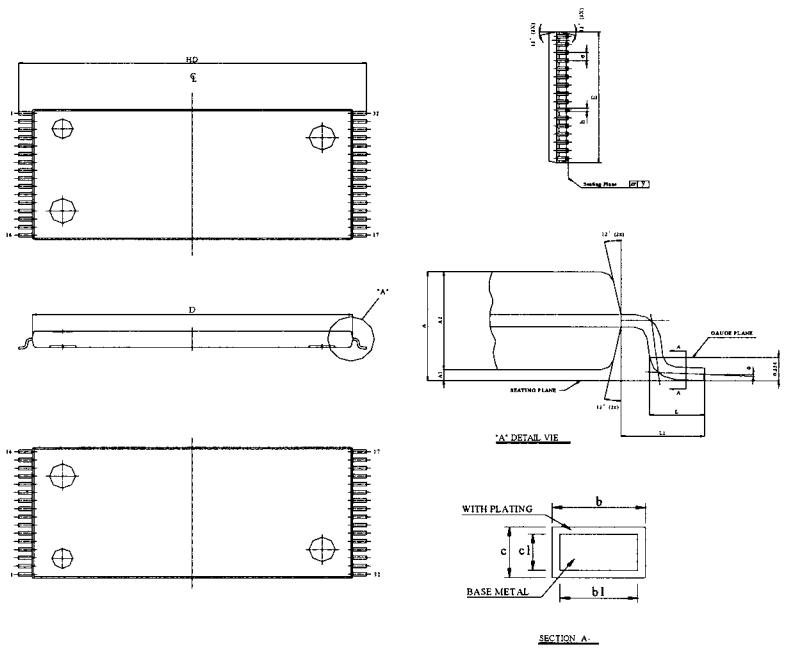
■ PACKAGE DIMENSIONS



UNIT / SYMBOL	INCH	MM
A	0.0433± 0.004	1.10± 0.10
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.009± 0.002	0.22± 0.05
b1	0.008± 0.001	0.20± 0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.465± 0.004	11.80± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.020± 0.004	0.50± 0.10
HD	0.528± 0.008	13.40± 0.20
L	0.0197 $^{+0.008}_{-0.004}$	0.50 $^{+0.2}_{-0.1}$
L1	0.0315± 0.004	0.80± 0.10
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°

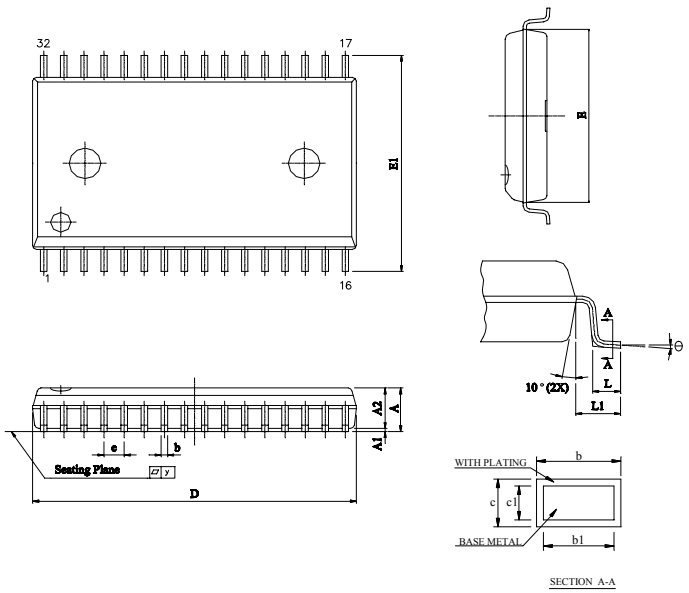
STSOP - 32

■ **PACKAGE DIMENSIONS (continued)**



SYMBOL \ UNIT	INCH	MM
A	0.0433± 0.004	1.10± 0.10
A1	0.004± 0.002	0.10± 0.05
A2	0.039± 0.002	1.00± 0.05
b	0.009± 0.002	0.22± 0.05
b1	0.008± 0.001	0.20± 0.03
c	0.004 ~ 0.008	0.10 ~ 0.21
c1	0.004 ~ 0.006	0.10 ~ 0.16
D	0.724± 0.004	18.40± 0.10
E	0.315± 0.004	8.00± 0.10
e	0.020± 0.004	0.50± 0.10
HD	0.787± 0.008	20.00± 0.20
L	0.0197 $^{+0.008}_{-0.004}$	0.50 $^{+0.2}_{-0.1}$
L1	0.0315± 0.004	0.80± 0.10
y	0.004 Max.	0.1 Max.
θ	0° ~ 8°	0° ~ 8°

TSOP - 32



SYMBOL \ UNIT	INCH	MM
A	0.111±0.007	2.821±0.176
A1	0.009±0.005	0.229±0.127
A2	0.1055±0.0055	2.680±0.140
b	0.014 ~ 0.020	0.35 ~ 0.50
b1	0.014 ~ 0.018	0.35 ~ 0.46
c	0.006 ~ 0.012	0.15 ~ 0.32
c1	0.006 ~ 0.011	0.15 ~ 0.28
D	0.805±0.005	20.447±0.127
E	0.445±0.005	11.303±0.127
E1	0.555±0.012	14.097±0.305
e	0.050±0.006	1.270±0.152
L	0.033±0.010	0.834±0.25
L1	0.055±0.008	1.397±0.203
y	0.004 Max.	0.1 Max.
θ	0° ~ 10°	0° ~ 10°

SOP -32