

Specification for BTHQ 42003AV-SRE-06 W.C. (KS 0073)

Version June 2003

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**Specification
of
LCD Module Type
Model No.: BTHQ 42003AV-07**

1. General Description

- ⌘ 20 characters(5x8 dots) x 4 lines STN Positive Reflective Yellow Dot Matrix LCD module.
- ⌘ Viewing Angle: 6 O'clock direction.
- ⌘ Driving duty: 1/33 Duty, 1/5 bias.
- ⌘ SAMSUNG' KS0073P-00CC (Die form) LCD Controller & Driver.
- ⌘ 'SAMSUNG' KS0065B-PCC (Die form) LCD Segment Driver or equivalent.
- ⌘ Temperature compensation.
- ⌘ Connector CON-16X1-35: 16 pins x 1 row, pitch=1.00mm, SMD
(“FULLCONN”, P/N:T03-2000-2160).

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	65.0(W) x 28.4(H) x 9.0 MAX.(D) (Excluded connector)	mm
Viewing area	46.0(W) x 18.4(H)	mm
Display format	20 characters x 4 lines	-
Character size	1.85(W) x 3.153(H) (5 x 8 dots)	mm
Character spacing	0.30(W) x 1.097(H)	mm
Character pitch	2.15(W) x 4.250(H)	mm
Dot size	0.358(W) x 0.381(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.373(W) x 0.396(H)	mm
Weight	Approx. 16.0	grams

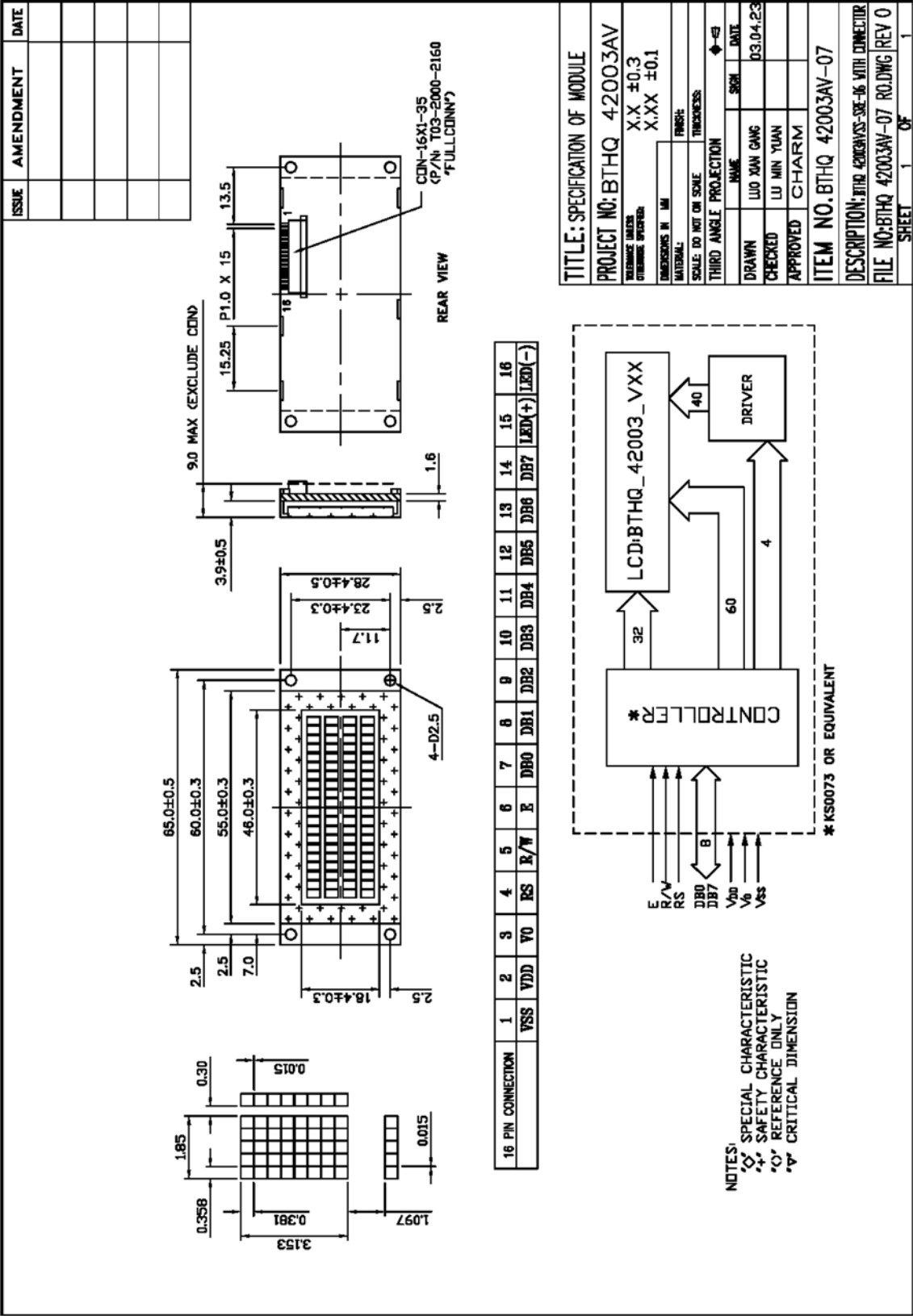


Figure 1: Outline Drawing

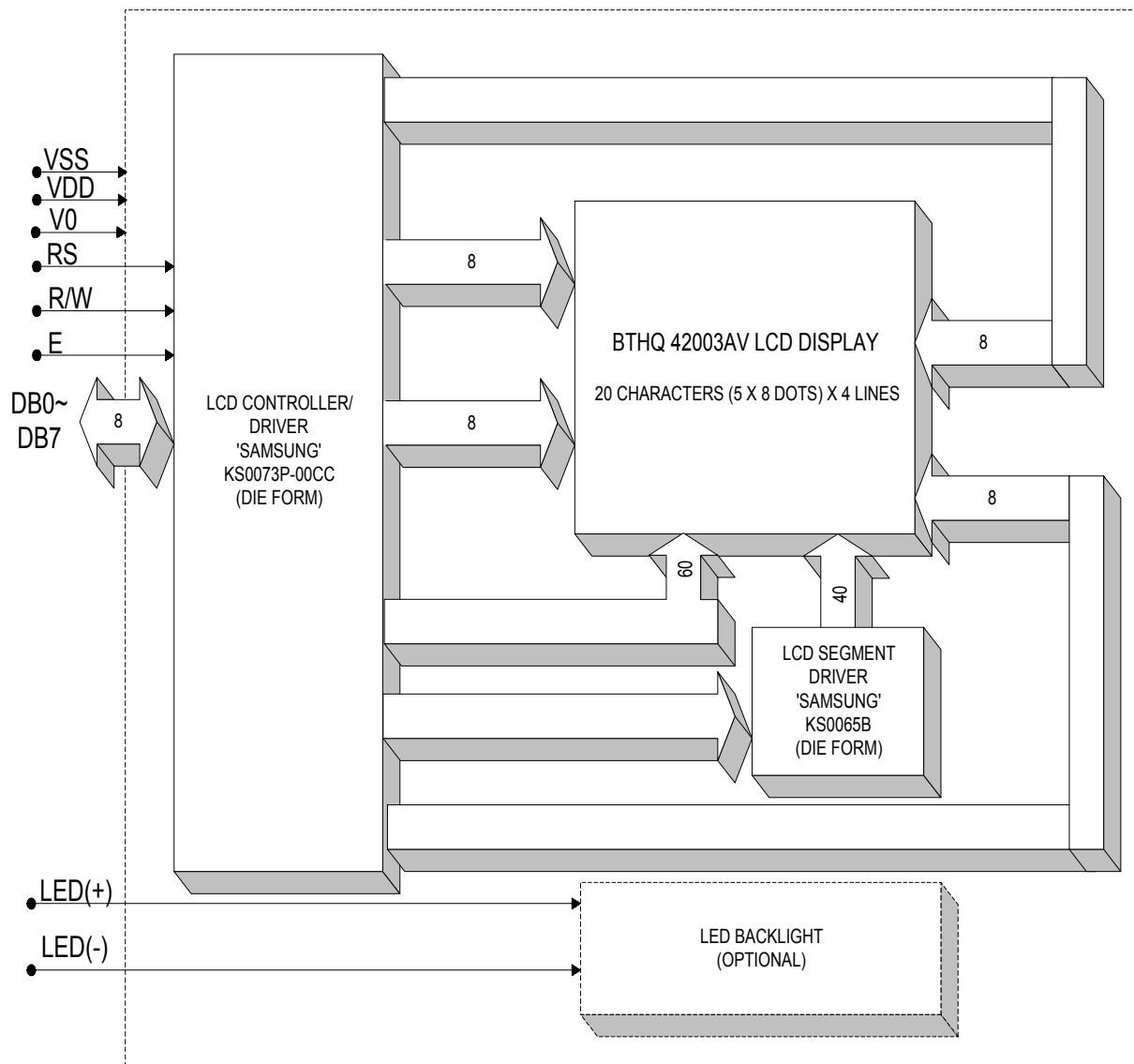


Figure 2: Block Diagram

3. Interface signals

Table 2

Pin No.	Symbol	Description
1	VSS	Ground (0V).
2	VDD	Power supply for logic (+5.0V)
3	V0	Inputs voltage to the booster to generate the liquid crystal display drive voltage. It is the reference voltage and power supply for the booster.
4	RS	Register Select Input: “High” for Data register (for read and write) “Low” for Instruction register (for write), Busy flag, address counter (for read)
5	R/W	Read/Write signal: ‘High’ for Read mode. ‘Low’ for Write mode.
6	E	Enable. Start signal for data read /write.
7	DB0	Data input/output (LSB)
8	DB1	Data input/output
9	DB2	Data input/output
10	DB3	Data input/output
11	DB4	Data input/output
12	DB5	Data input/output
13	DB6	Data input/output
14	DB7	Data input/output (MSB)
15	LED(+)	Anode of LED Backlight (Optional).
16	LED(-)	Cathode of LED Backlight (Optional).

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings (Ta = 25 °C)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Power Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Power Supply voltage (LCD drive)	VLCD	-0.3	+15.0	V
Input voltage	Vin	-0.3	VDD+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0℃	+50℃	-10℃	+60℃	Dry
Humidity	95% max. RH for Ta ≤ 40℃ < 95% RH for Ta > 40℃				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At $T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	$V_{DD} - V_{SS}$		4.75	5.0	5.25	V
Supply voltage (LCD) (Built-in)	$V_{LCD} = V_{DD} - V_5$	$T_a = 0\text{ }^{\circ}\text{C}$, $V_{DD} = 5\text{V}$, Note (1)	-	5.5	-	V
		$T_a = 25\text{ }^{\circ}\text{C}$ $V_{DD} = 5\text{V}$, Note (1)	4.9	5.3	5.7	V
		$T_a = 50\text{ }^{\circ}\text{C}$ $V_{DD} = 5\text{V}$, Note (1)	-	5.0	-	V
Input signal voltage for E,DB0-DB7,R/W,RS	V_{IH}	“High” level	$0.7V_{DD}$	-	V_{DD}	V
	V_{IL}	“Low” level	-0.3	-	0.6	V
Supply Current (Logic & LCD)	I_{DD}	Character mode, $V_{DD} = 5\text{V}$	-	2.3	3.5	mA
		Checker board mode, $V_{DD} = 5\text{V}$	-	2.3	3.5	mA

Note (1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

At $T_a = 0^{\circ}\text{C}$ To $+50^{\circ}\text{C}$, $V_{DD} = +5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$.

Refer to Fig. 3, the bus timing diagram for write mode.

Table 6

Parameter	Symbol	Min.	Max.	Unit
E Cycle Time	t_c	500	-	ns
E Pulse Width (High, Low)	t_w	230	-	ns
E Rise time	t_R	-	20	ns
E Fall time	t_F	-	20	ns
R/W and RS Setup Time	t_{su1}	40	-	ns
R/W and RS Hold Time	t_{H1}	10	-	ns
Data setup time	t_{su2}	60	-	ns
Data hold time	t_{H2}	10	-	ns

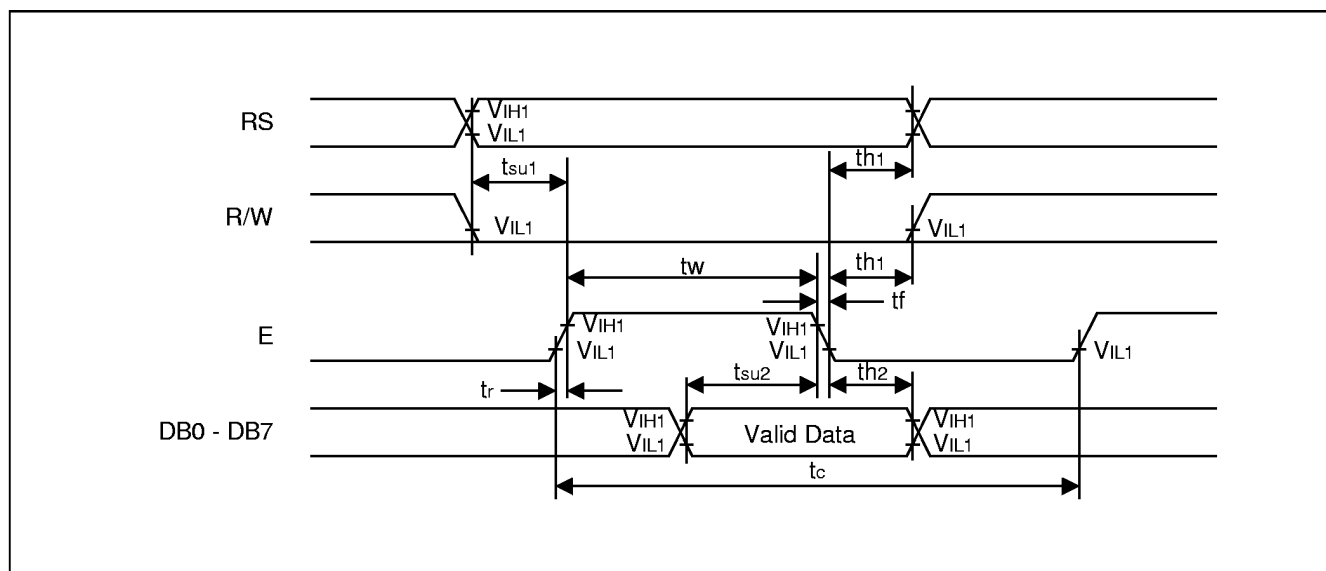


Figure 3: The bus timing diagram for write mode.

Refer to Fig. 4, the bus timing diagram for read mode.

Table 7

Parameter	Symbol	Min.	Max.	Unit
E Cycle Time	t_C	500	-	ns
E Pulse Width (High, Low)	t_W	230	-	ns
E Rise time	t_R	-	20	ns
E Fall time	t_F	-	20	ns
R/W and RS Setup Time	t_{SU}	40	-	ns
R/W and RS Hold Time	t_H	10	-	ns
Data Output Delay Time	t_D	-	160	ns
Data Hold Time	t_{DH}	5	-	ns

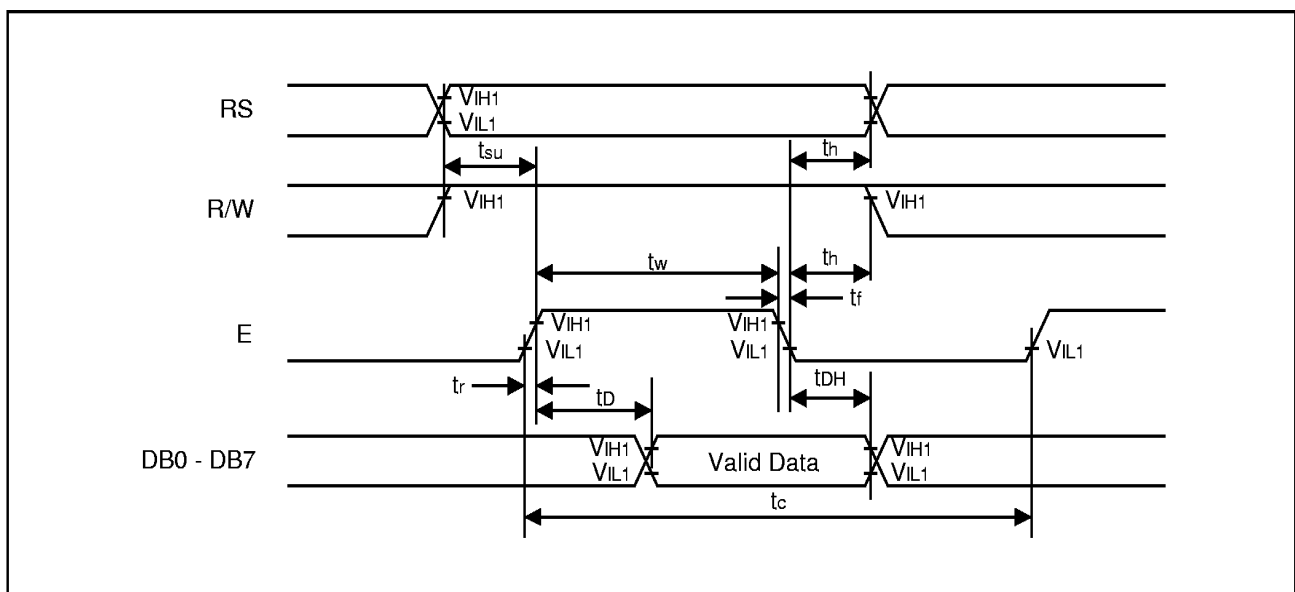


Figure 4: The bus timing diagram for read mode.

6. Character Generator ROM (KS0073-00)

KS0073-00																
Upper 4bit Lower 4bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)															
LLLH	(2)															
LLHL	(3)															
LLHH	(4)															
LHLL	(5)															
LHLH	(6)															
LHHL	(7)															
LHHH	(8)															
HLLL	(1)															
HLLH	(2)															
HLHL	(3)															
HLHH	(4)															
HHLL	(5)															
HHLH	(6)															
HHHL	(7)															
HHHH	(8)															