

Specification

BTHQ 128064AVC1-SMN-06-LED WHITE-COG

Version January 2005

BTHQ 128064AVC1-SMN-06-LED WHITE-COG

JAN/2005

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DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2005.01.05	First Release. Based on a.) VL-QUA-012B REV.W 2004.03.20 According to VL-QUA-012B, LCD size is small because Unit Per Laminate=15 which is more than 6pcs/Laminate.	ZHANG YAN FANG	LIN RONG SHOU

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**Specification
of
LCD Module Type
Item No.: COG-BTC12864-09**

1. General Description

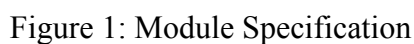
- 128 x 64 dots STN Blue Negative Transmissive STD LCD Graphic Module.
- Viewing Direction: 6 O'clock.
- Driving duty: 1/65 Duty, 1/9 bias.
- "ULTRA CHIP" UC1601 (COG) LCD Controller-Driver or equivalent.
- Logic Power Supply: +3V.
- FPC connection.
- White LED05 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	76.5 (W) x 82.5(H) x 8.5(D) (Include FPC and Backlight)	mm
Viewing area (V.A.)	60.0 MIN. (W) x 40.0 MIN.(H)	mm
Active area (A.A.)	56.945 (W) x 37.425 (H)	mm
Display format	128 x 64	dots
Dot size	0.43(W) x 0.57(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.445(W) x 0.585(H)	mm
Weight:	TBD	grams



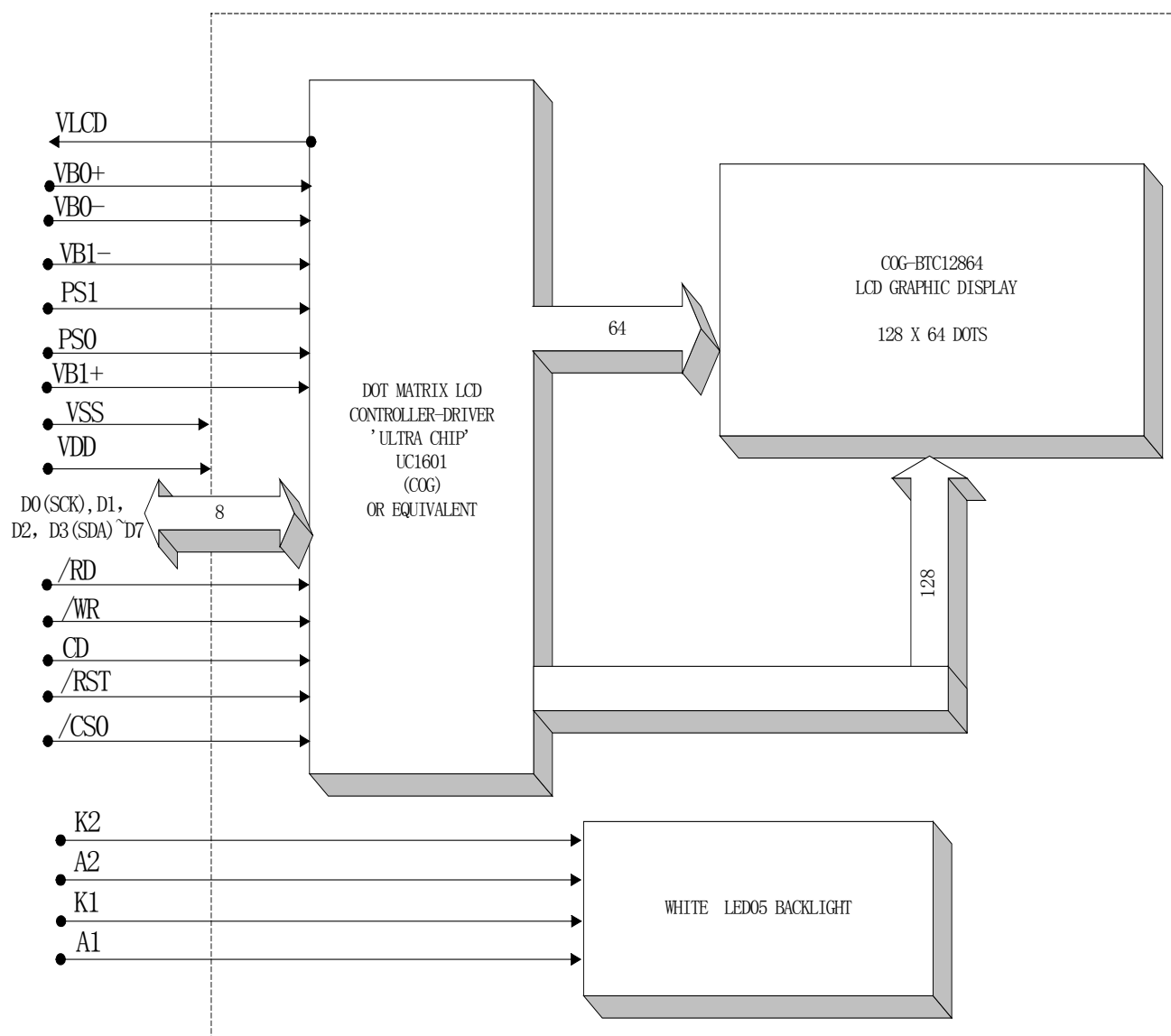


Figure 2: Block diagram

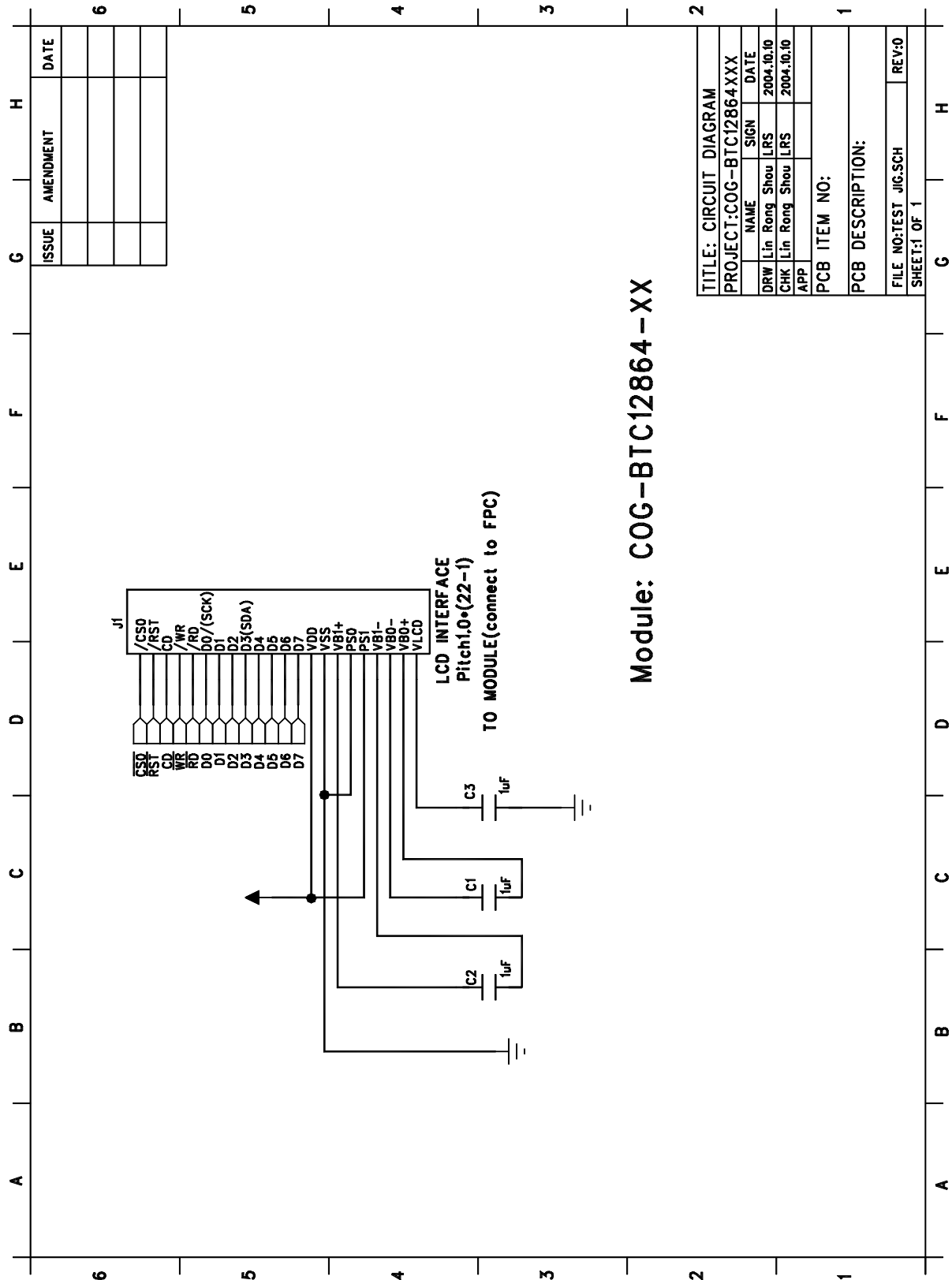


Figure 3: Application Circuit

3. Interface signals

Table 2

Pin No.	Symbol	Description																															
1	$\overline{CS0}$	Chip Select. In parallel mode and S8 mode, chip is selected when $\overline{CS0}$ = “L” and CS1= “H”. When the chip is not selected, D[7:0] may be high impedance.																															
2	$\overline{RST}$	When $\overline{RST}$ = “L”, all control registers are re-initialized by their default states. When $\overline{RST}$ is not used, connect the pin to VDD.																															
3	CD	Select Command or Display Data for read/write operation. “L”: Command “H”: Display data																															
4	$\overline{WR}$	$\overline{RD}/\overline{WR}$ (WR[1:0]) controls the read/write operation of the host interface.																															
5	$\overline{RD}$	In parallel mode, RD/WR(WR[1:0]) meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used. Connect to VSS.																															
6	D0(SCK)	<table><tr><td colspan="2">Bi-directional bus for both serial and parallel host interfaces.</td></tr><tr><td colspan="2">In S8 and S9 mode, connect unused pins to VDD or VSS.</td></tr><tr><td></td><td>PS=1x</td><td>Ps=0x</td></tr><tr><td>D0</td><td>D0</td><td>SCK</td></tr><tr><td>D1</td><td>D1</td><td></td></tr><tr><td>D2</td><td>D2</td><td></td></tr><tr><td>D3</td><td>D3</td><td>SDA</td></tr><tr><td>D4</td><td>D4</td><td></td></tr><tr><td>D5</td><td>D5</td><td></td></tr><tr><td>D6</td><td>D6</td><td></td></tr><tr><td>D7</td><td>D7</td><td></td></tr></table>	Bi-directional bus for both serial and parallel host interfaces.		In S8 and S9 mode, connect unused pins to VDD or VSS.			PS=1x	Ps=0x	D0	D0	SCK	D1	D1		D2	D2		D3	D3	SDA	D4	D4		D5	D5		D6	D6		D7	D7	
Bi-directional bus for both serial and parallel host interfaces.																																	
In S8 and S9 mode, connect unused pins to VDD or VSS.																																	
	PS=1x		Ps=0x																														
D0	D0		SCK																														
D1	D1																																
D2	D2																																
D3	D3		SDA																														
D4	D4																																
D5	D5																																
D6	D6																																
D7	D7																																
7	D1																																
8	D2																																
9	D3(SDA)																																
10	D4																																
11	D5																																
12	D6																																
13	D7																																
14	VDD	VDD1 is the digital power supply and it should be connected to a voltage source that is no higher than VDD2&3. VDD2&3 is the analog power supply and it should be connected to the same power source. Minimize the trace resistance for VDD2&3.																															
15	VSS	Ground.																															
17	PS0	PS[1:0] Parallel/Serial.																															
18	PS1	Serial modes: “LL”: serial (S8) “LH”: serial (S9) Parallel modes: “HL”: 8080 “HH”: 6800																															
16	VB1+	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of CBX value between VBX+ and VBX-. The resistance of these four traces directly affects the SEG driving strength of the resulting LCD module. Minimize the trace resistance is critical in achieving high quality image.																															
19	VB1-																																
20	VB0-																																
21	VB0+																																
22	VLCD	Main LCD Power Supply. A by-pass capacitor CL is optional. When CL is used, connect CL between VLCD and VSS, and keep the trace resistance under 300 Ohm.																															
-	A	Anode of LED Backlight.																															
-	K	Cathode of LED Backlight.																															

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings – for IC Only

Table 3

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	V_{DD}	-0.3	+3.3	V
LCD generator supply voltage	V_{DD2}	-0.3	+3.3	V
Analog circuit supply voltage	V_{DD3}	-0.3	+3.3	V
Voltage difference between V_{DD} and $V_{DD2/3}$	$V_{DD2/3} - V_{DD}$		1.2	V
LCD generated voltage	V_{LCD}	-0.3	+12	V
Any input/output	V_{IN}/V_{OUT}	-0.4	$V_{DD}+0.3$	V

Note:

1. V_{DD} is based on $V_{SS} = 0V$.
2. Stress values listed above may cause permanent damages to the device.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for $T_a \leq 40^\circ C$ < 95% RH for $T_a > 40^\circ C$				No condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: $981 \text{ m/s}^2 = 100g$ Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 3V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic & booster)	VDD-VSS		2.85	3.0	3.15	V
LCD driving voltage (Built-in)	VLCD-VSS	At Ta = 0°C, Character mode, VDD = 3V, Note 1	-	9.3	-	V
		At Ta = +25°C, Character mode, VDD = 3V, Note 1	8.7	8.9	9.1	V
		At Ta = +50°C, Character mode, VDD = 3V, Note 1	-	8.6	-	V
Input signal voltage	V _{IH}	“H” level	0.8 VDD	-	-	V
	V _{IL}	“L” level	-	-	0.2VDD	V
Supply Current (Logic & booster)	IDD	Character mode, Note 1	-	0.5	0.75	mA
		Checker board mode, Note 1	-	0.54	0.81	mA
Supply Voltage of White LED05 backlight	VLED05	Forward current =30mA	3.4	3.6	3.8	V
Luminance (on the backlight surface) of backlight		No. of LED chips =1x2=2.	33	45	-	cd/ m ²

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

Parallel bus timing characteristics (for 8080 MCU)

At $T_a = 0^\circ\text{C}$ to $+50^\circ\text{C}$, $V_{DD} = 3\text{V} \pm 5\%$.

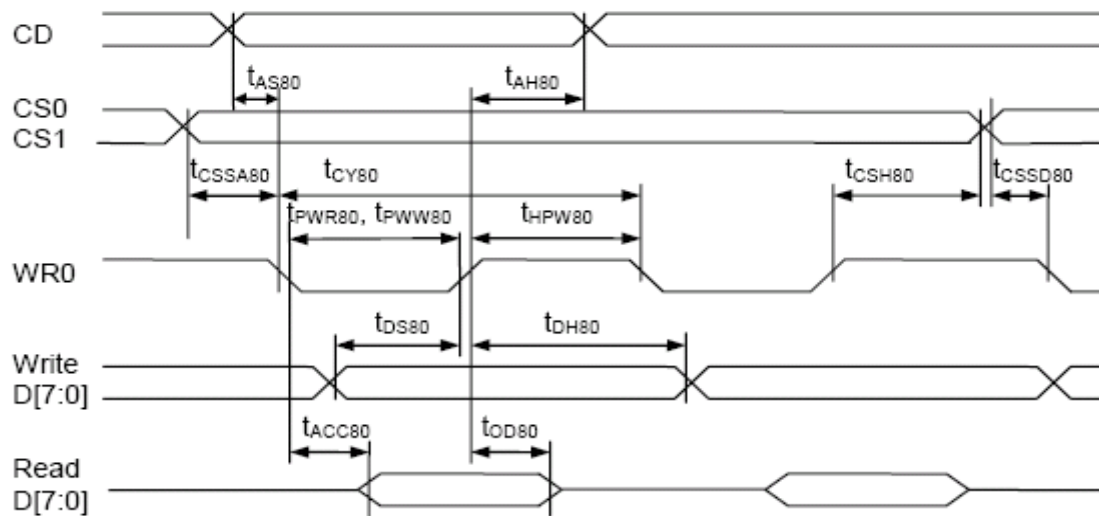


Figure: 4 Parallel Bus Timing Characteristics (for 8080 MCU)

At $T_a = 0^\circ\text{C}$ to $+50^\circ\text{C}$, $V_{DD} = 3\text{V} \pm 5\%$.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80}	CD	Address setup time		0	—	nS
t_{AH80}	CD	Address hold time		40	—	nS
t_{CY80}		System cycle time		135	—	nS
t_{PWR80}	WR1	Pulse width (read)		65	—	nS
t_{PWW80}	WR0	Pulse width (write)		65	—	nS
t_{HPW80}	WR0, WR1	High pulse width		65	—	nS
t_{DS80}	D0~D7	Data setup time		30	—	nS
t_{DH80}	D0~D7	Data hold time		20	—	nS
t_{ACC80}		Read access time	$C_L = 100\text{pF}$	—	50	nS
t_{OD80}		Output disable time	$C_L = 100\text{pF}$	10	50	nS
t_{CSSA80}	CS1/CS0	Chip select setup time		10	—	nS
t_{CSSD80}	CS1/CS0	Chip select setup time		10	—	nS
t_{CSH80}	CS1/CS0	Chip select setup time		20	—	nS

Parallel bus timing characteristics (for 6800 MCU)

At Ta= 0°C to +50°C,VDD=3V±5%.

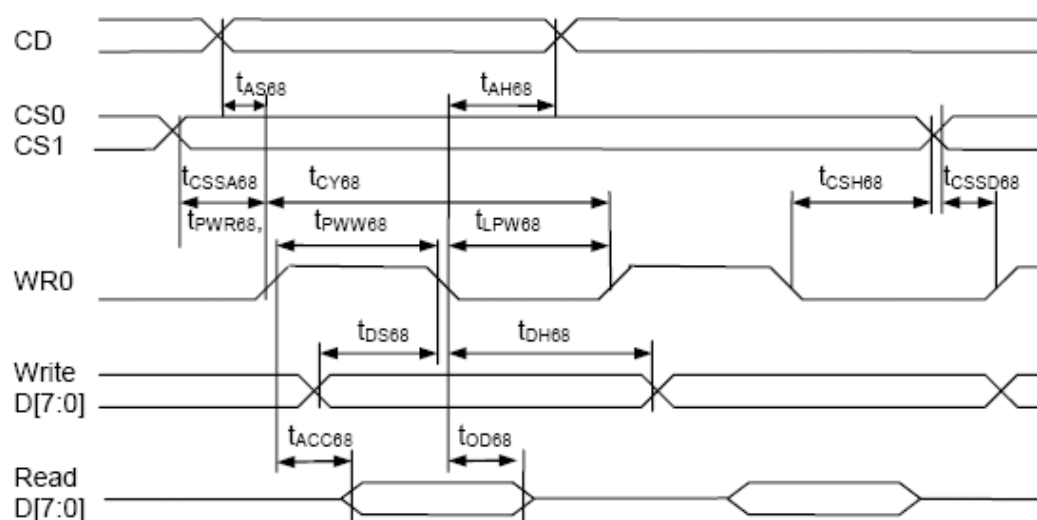


Figure: 5 Parallel Bus Timing Characteristics (for 6800 MCU)

At Ta= 0°C to +50°C,VDD=3V±5%.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{AS68}	CD	Address setup time		0	–	nS
t _{AH68}		Address hold time		40	–	nS
t _{CY68}		System cycle time		135	–	nS
t _{PWR68}	WR1	Pulse width (read)		65	–	nS
t _{PWW68}		Pulse width (write)		65	–	nS
t _{LPW68}		Low pulse width		65	–	nS
t _{DS68}	D0~D7	Data setup time		30	–	nS
t _{DH68}		Data hold time		15	–	nS
t _{ACC68}		Read access time	C _L = 100pF	–	50	nS
t _{OD68}		Output disable time		10	50	nS
t _{CSSA68}	CS1/CS0	Chip select setup time		10		nS
t _{CSSD68}				10		nS
t _{CSH68}				20		nS

Serial Bus Timing Characteristics (for S8)

At $T_a = 0^\circ\text{C}$ to $+50^\circ\text{C}$, $V_{DD} = 3V \pm 5\%$.

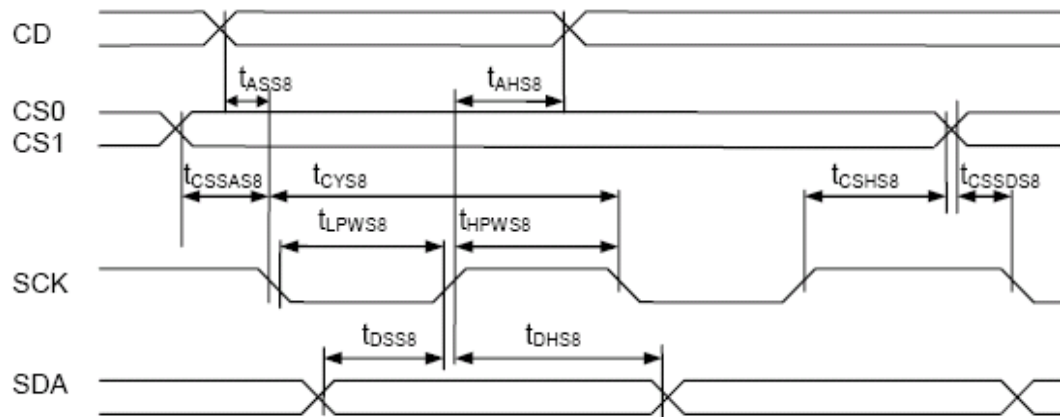


Figure: 6 Serial Bus Timing Characteristics (for S8)

At $T_a = 0^\circ\text{C}$ to $+50^\circ\text{C}$, $V_{DD} = 3V \pm 5\%$.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		40	–	nS
t_{CYS8}	SCK	System cycle time		135	–	nS
t_{LPWS8}		Low pulse width		65	–	nS
t_{HPWS8}		High pulse width		65	–	nS
t_{DSS8}	SDA	Data setup time		30	–	nS
t_{DHS8}		Data hold time		15	–	nS
t_{CSSAS8}	CS1/CS0	Chip select setup time		10		nS
t_{CSSDS8}				10		
t_{CSHS8}				20		

Serial bus timing characteristics (for S9)

At $T_a = 0^\circ\text{C}$ to $+50^\circ\text{C}$, $V_{DD} = 3V \pm 5\%$.

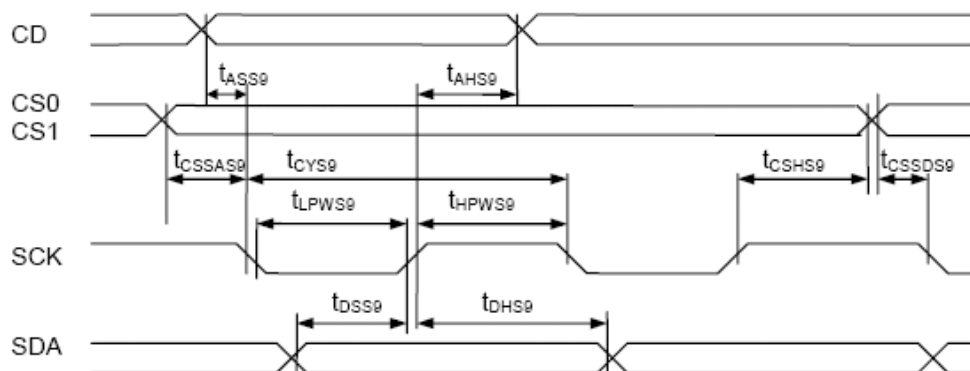


Figure: 7 Serial Bus Timing Characteristics (for S9)

At Ta= 0°C to +50°C,VDD=3V±5%.

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS0}	CD	Address setup time		0	–	nS
t_{AHS0}		Address hold time		40	–	nS
t_{CYS0}	SCK	System cycle time		135	–	nS
t_{LPWS0}		Low pulse width		65	–	nS
t_{HPWS0}		High pulse width		65	–	nS
t_{DSS0}	SDA	Data setup time		30	–	nS
t_{DHS0}		Data hold time		15	–	nS
t_{CSSAS0}	CS1/CS0	Chip select setup time		10		nS
t_{CSSDS0}				10		
t_{CSHS0}				20		

Reset characteristics

At Ta= 0°C to +50°C,VDD=3V±5%.

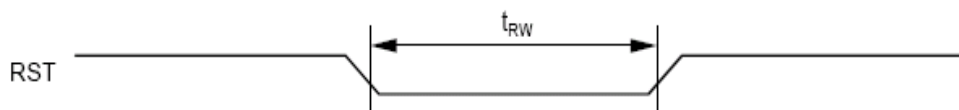


Figure: 8 Reset Characteristics

At Ta= 0°C to +50°C,VDD=3V±5%

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		1	–	μS

6. Appendix –LED Specifications

6.1. 极限参数 ABSOLUTE MAXIMUM RATINGS

(除非特别说明,环境温度 $T_a=25^{\circ}\text{C}$. Unless specified, The Ambient temperature $T_a=25^{\circ}\text{C}$)

项目 Item	符号 Symbol	条件 Conditions	值 Rating	单位 Unit
* 极限直流正向电流 Absolute maximum forward current	Ifm		25x2	mA
* 脉冲驱动时极限正向电流 Peak forward current	Ifp	1 msec 脉冲, 1/10 占空比 1 msec Plus 10% Duty Cycle	60x2	mA
反向电压 Reverse Voltage	Vr		5	V
* 极限功耗 Power dissipation	Pd		100x2	mW
工作温度 Operating Temperature Range	Topr		$-30\sim+70^{\circ}\text{C}$	$^{\circ}\text{C}$
贮存温度 Storage Temperature Range	Tstg		$-40\sim+80^{\circ}\text{C}$	$^{\circ}\text{C}$

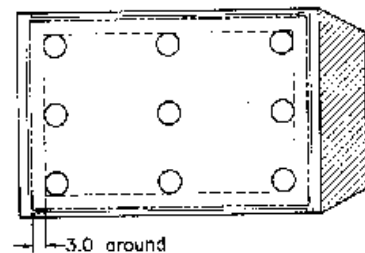
- * 当工作温度高于 25°C 时, Ifm, Ifp 和 Pd 必须降低; 电流降低率是 $-0.36\text{mA}/^{\circ}\text{C}$ (直流驱动), 或 $-0.86\text{mA}/^{\circ}\text{C}$ (脉冲驱动), 功耗降低率是 $-0.75\text{mW}/^{\circ}\text{C}$. 产品的工作电流不能大于对应工作温度条件 Ifm 或 Ifp 的 50 %.
- For operation above 25°C , The Ifm Ifp & Pd must be derated, the Current derating is $-0.36\text{mA}/^{\circ}\text{C}$ for DC drive and $-0.86\text{mA}/^{\circ}\text{C}$ for Pulse drive, the Power dissipation is $-0.75\text{mW}/^{\circ}\text{C}$. The product working current must not more than the 50 % of the Ifm or Ifp according to the working temperature.

6.2. 电、光特性 ELECTRICAL-OPTICAL CHARACTERISTICS

(除非特别说明,环境温度 $T_a=25^{\circ}\text{C}$. Unless specified, The Ambient temperature $T_a=25^{\circ}\text{C}$)

项目 Item	符号 Symbol	最小值 min.	典型值 typ.	最大值 max.	单位 Unit	测定条件 Condition
正向电压 Forward Voltage	Vf	3.4	3.6	3.8	V	If= 15x2 mA
反向电流 Reverse Current	Ir			15x2	μA	Vr= 3 V
峰值波长 Peak wave length	λ_p				nm	If= 15x2 mA
频谱半宽度 Spectral Line Half width	$\Delta\lambda$				nm	If= 15x2 mA
* 亮度 Luminance	Lv	33	45		cd/m^2	If= 15x2 mA

- * 亮度值是 9 个测量点的平均值, 亮度最大值比最小值一般小于 1.5 (最大 1.7). 使用 BM-7 亮度色度仪测量, 测量光圈 $\phi 5\text{mm}$.
- The luminance is the average value of 9 points, and The Lvmax./Lvmin. is less than 1.5 Typical (max 1.7). The measurement instrument is BM-7 luminance Colorimeter. The aperture is $\phi 5\text{mm}$.

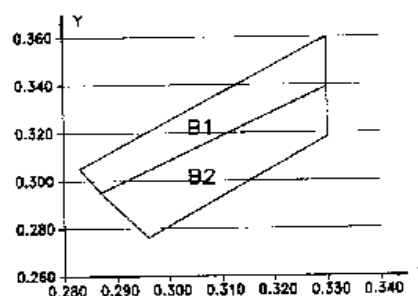


Colour Coordinate see the form.

	Rank B1 Limiting Region				Rank B2 Limiting Region			
X	0.287	0.283	0.330	0.330	0.296	0.287	0.330	0.330
Y	0.295	0.305	0.360	0.339	0.276	0.295	0.339	0.318

注: 色度坐标值公差±0.01

每批出货产品的色度坐标只能在B1区或只能在B2区。

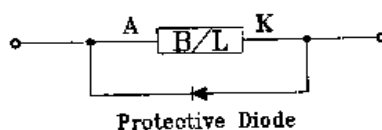


6.3. STATIC ELECTRICITY AND SURGE

- * Static electricity and surge will damage the LEDs. It is recommended to use a wrist band or anti-electrostatic glove when handling the LEDs.
- * All devices, equipment and machinery must be properly grounded.
- * When inspecting own final products on which LEDs were mounted, it is recommended to check also whether the mounted LEDs are damaged by static electricity or not. It is easy to find static-damaged LEDs by light emission test at lower current (below 1mA is recommended). Damaged LEDs will show some unusual characteristics such as leak current remarkably increases, starting forward voltage becomes lower, or the LEDs get unlighted at the low current.

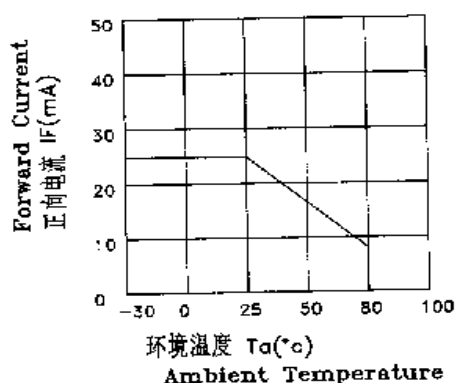
6.4. RECOMMEND CONNECTION OF STATIC-ELECTRICITY RESISTANCE

- * This circuit diagram is a common ESD protection circuit for all super bright blue, white and green color LED backlight application.

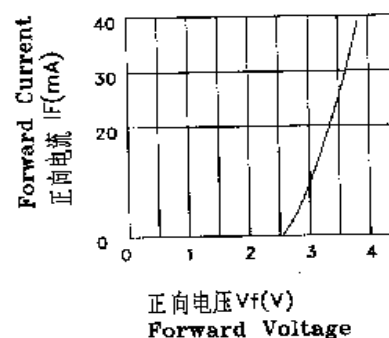


6.5. LED ELECTRICAL CHARACTERISTICS

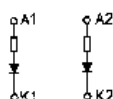
- (1) 正向电流-周围温度
Forward Current VS. Ambient Temperature



- (2) 正向电流-正向电压特性
Forward Current VS. Forward Voltage



6.6. 电路图 CIRCUIT DIAGRAM (LED 2x(1x1)=2 dies)



7. LCD Cosmetic Conditions

- a.) Reference document follow VL-QUA-012B.
- b.) LCD size of the product is small.

8. Remark:

- a.) Identification labels will be stuck on the module without obstructing the viewing area of display,
- b.) Data Modul does not responsible for any polarizer defect after the protective film has been removed from the display.
- c.) The stiffener on FPC/FFC/COF must not be bent during or after assembly.

- END -