

DOCUMENT NUMBER AND REVISION

VL-PS-COG-BT12864W-02 REV. A

(COG-BT12864-B-LED05-W-6; STN, BLUE, -VE, TRANSMISSIVE, LED05 WHITE, STD)

DOCUMENT TITLE:
 PRELIMINARY SPECIFICATION
 OF
 LCD MODULE TYPE

CUSTOMER	DATA MODUL
MODEL NUMBER	COG-BT12864W-02
CUSTOMER APPROVAL	
DATE	

DEPARTMENT	NAME	SIGNATURE	DATE
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**Preliminary Specification
of
LCD Module Type
Item No.: COG-BT12864W-02**

1. General Description

- 128 x 64 dots STN Blue Negative Transmissive STD LCD Module.
- Viewing Direction: 6 O'clock.
- Driving duty: 1/65 Duty, 1/9 bias.
- 'ULTRA CHIP' UC1606 (COG) LCD Controller-Driver or equivalent.
- Logic Power Supply: +3V.
- FPC.
- White LED05 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	76.5(W) x 82.5(H) x 8.5(D)	mm
Effective viewing area (V.A.)	60.00 MIN.(W) x 40.00 MIN.(H)	mm
Active area (A.A.)	56.945(W) x 37.425(H)	mm
Display format	128 x 64	dots
Dot size	0.43(W) x 0.57(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.445(W) x 0.585(H)	mm
Weight:	TBD	grams

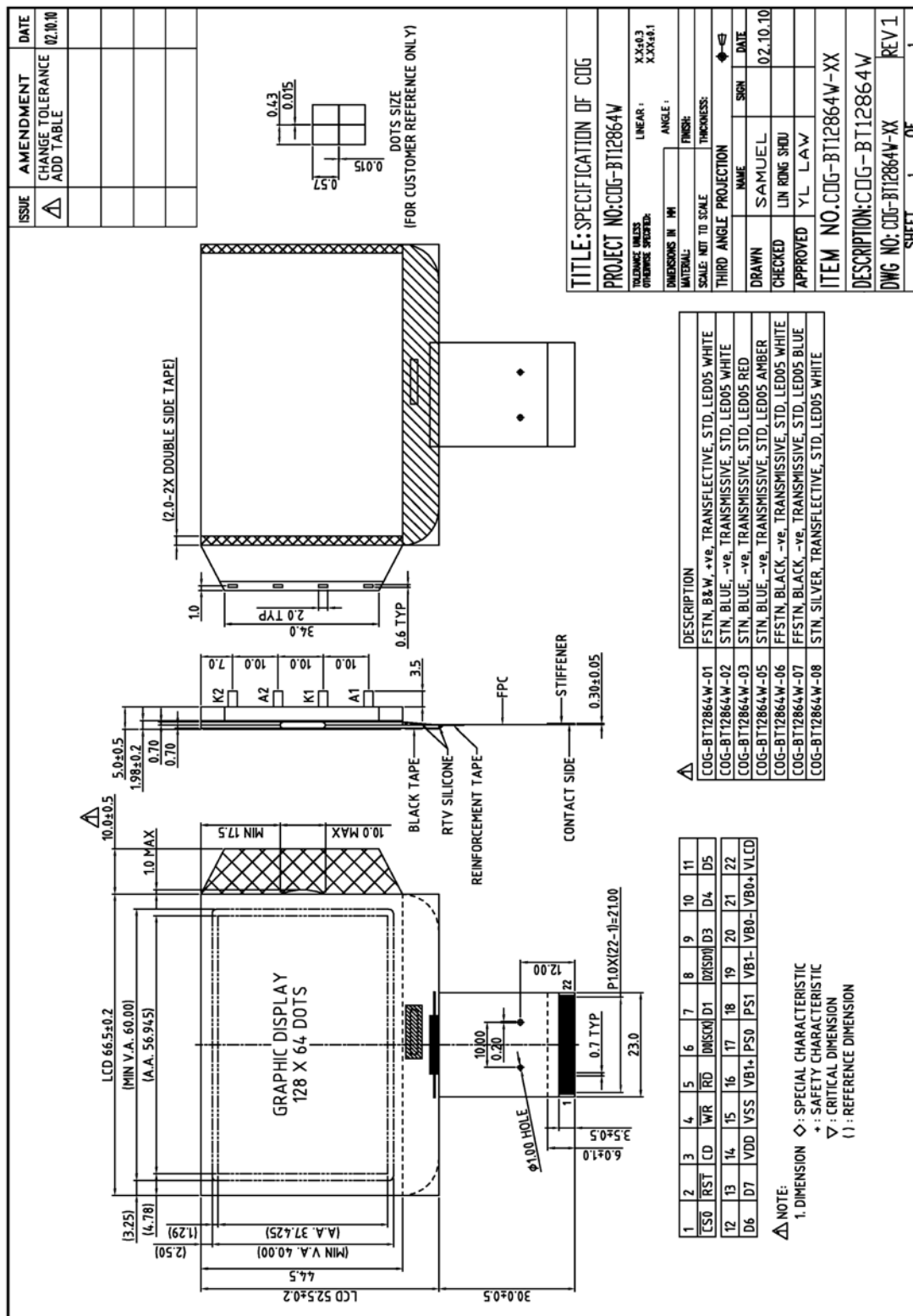


Figure 1: Outline Drawing.

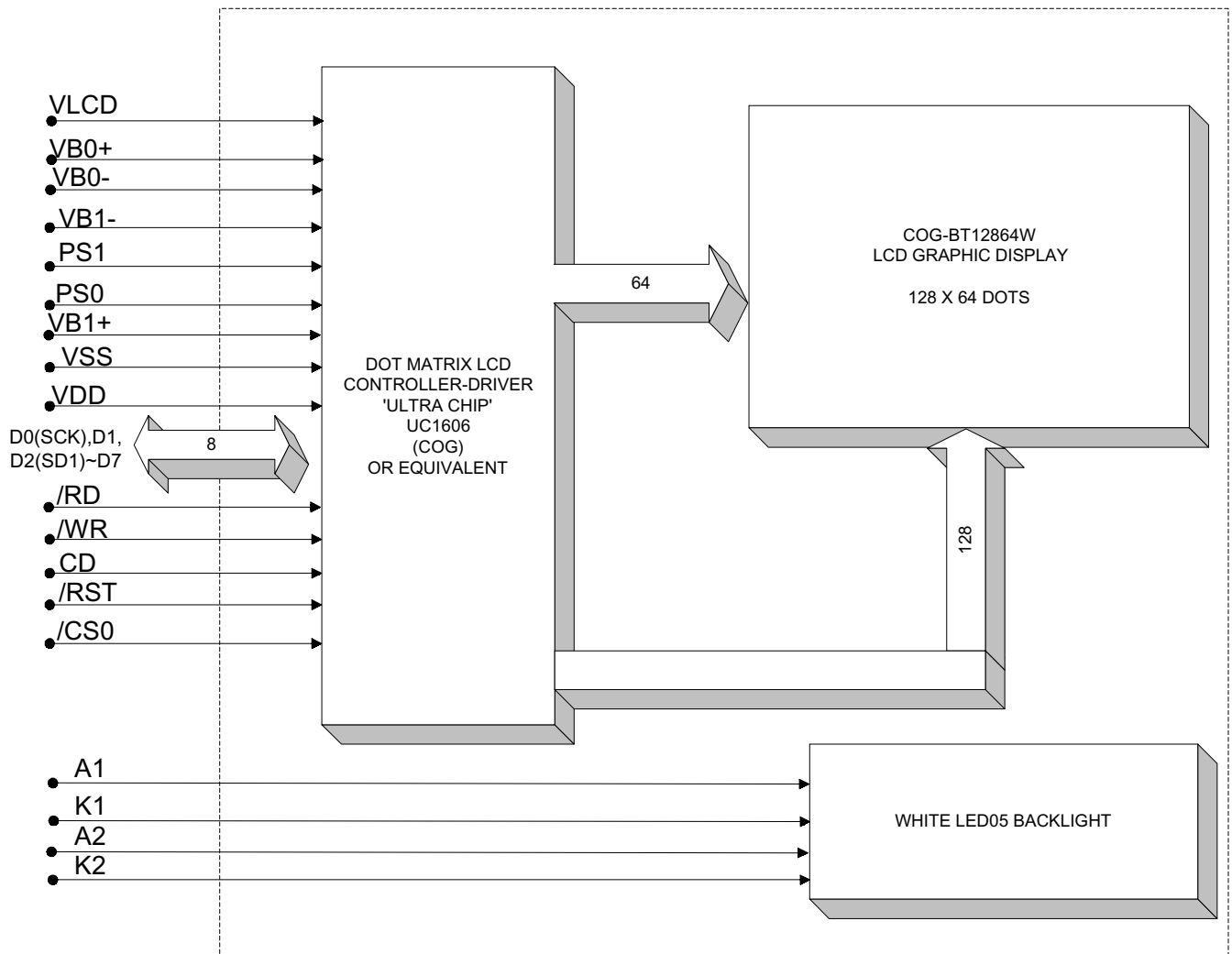


Figure 2: Block diagram

3. Interface signals

Table 2

Pin No.	Symbol	Description																											
1	$\overline{CS0}$	Chip Select. In parallel mode and S8 mode, chip is selected when $\overline{CS0}$ ="L" and CS1="H". When the chip is not selected, D[7:0] may be high impedance.																											
2	$\overline{RST}$	When $\overline{RST}$ ="L", all control registers are re-initialized by their default states. When RST is not used, connect the pin to VDD.																											
3	CD	Select Command or Display Data for read/write operation. "L": Command "H": Display data																											
4	$\overline{WR}$	$\overline{RD}/\overline{WR}$ (WR[1:0]) controls the read/write operation of the host interface.																											
5	$\overline{RD}$	In parallel mode, RD/WR(WR[1:0]) meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used. Connect to VSS.																											
6	D0(SCK)	Bi-directional bus for both serial and parallel host interfaces.																											
7	D1	In S8 and S9 mode, connect unused pins to VDD or VSS.																											
8	D2(SD1)	<table><tr><td></td><td>PS=1x</td><td>Ps=0x</td></tr><tr><td>D0</td><td>D0</td><td>SCK</td></tr><tr><td>D1</td><td>D1</td><td></td></tr><tr><td>D2</td><td>D2</td><td>SD1</td></tr><tr><td>D3</td><td>D3</td><td></td></tr><tr><td>D4</td><td>D4</td><td></td></tr><tr><td>D5</td><td>D5</td><td></td></tr><tr><td>D6</td><td>D6</td><td></td></tr><tr><td>D7</td><td>D7</td><td></td></tr></table>		PS=1x	Ps=0x	D0	D0	SCK	D1	D1		D2	D2	SD1	D3	D3		D4	D4		D5	D5		D6	D6		D7	D7	
	PS=1x	Ps=0x																											
D0	D0	SCK																											
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D6	D6																												
D7	D7																												
9	D3																												
10	D4																												
11	D5																												
12	D6																												
13	D7																												
14	VDD	VDD1 is the digital power supply and it should be connected to a voltage source that is no higher than VDD2&3. VDD2&3 is the analog power supply and it should be connected to the same power source. Minimize the trace resistance for VDD2&3.																											
15	VSS	Ground.																											
17	PS0	PS[1:0] Parallel/Serial.																											
18	PS1	Serial modes: "LL": serial (S8) "LH": serial (S9) Parallel modes: "HL": 8080 "HH": 6800																											
16	VB1+	LCD Bias Voltages. These are the voltage sources to provide SEG driving currents.																											
19	VB1-	These voltages are generated internally. Connect capacitors of CBX value between																											
20	VB0-	VBX+ and VBX-. The resistance of these four traces directly affects the SEG																											
21	VB0+	driving strength of the resulting LCD module. Minimize the trace resistance is critical in achieving high quality image.																											
22	VLCD	Main LCD Power Supply. A by-pass capacitor CL is optional. When CL is used, connect CL between VLCD and VSS, and keep the trace resistance under 300 Ohm.																											
-	A1	Anode 1 of LED Backlight																											
-	K1	Cathode 1 of LED Backlight																											
-	A2	Anode 2 of LED Backlight																											
-	K3	Cathode 2 of LED Backlight																											

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 °C)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD1 - VSS	-0.3	+5.5	V
LCD generator supply voltage	VDD2 - VSS	-0.3	+5.5	V
Analog circuit supply voltage	VDD3 - VSS	-0.3	+5.5	V
LCD generated voltage	VLCD	-0.3	+15.5	V
Any input voltage	Vin	-0.3	VDD+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

VDD=VDD1=VDD2=VDD3.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 3V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic & booster)	VDD-VSS		2.85	3.0	3.15	V
LCD driving voltage	VLCD-VSS		9.3	9.6	9.9	V
Input signal voltage	V _{IH}	"H" level	0.8 VDD1	-	-	V
	V _{IL}	"L" level	-	-	0.2VDD1	V
Supply Current (Logic & booster)	IDD	Character mode, Note 1	-	0.2	0.3	mA
Supply voltage of white LED05 backlight (2 LED dies)	VA1K1	Forward current = 20 mA Number of LED dies =1x1 =1. LED color: White (Rank B)	3.4	3.6	3.8	V
	VA2K2	Forward current = 20 mA Number of LED dies =1x1 =1. LED color: White (Rank B)	3.4	3.6	3.8	V

Note

(1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

Parallel bus timing characteristics (for 8080 MCU)

At Ta= 0°C to +50°C

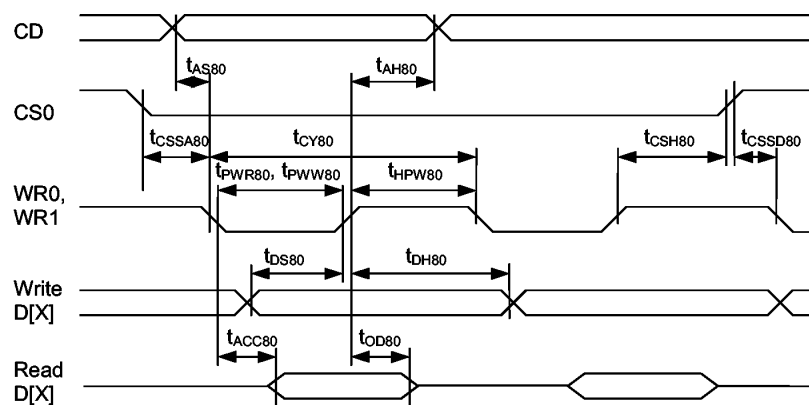


Figure 3 : Parallel Bus Timing Characteristics (for 8080 MCU)

(VDD=2.4V to 3.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{AS80}	CD	Address setup time		25	—	ns
t _{AH80}	CD	Address hold time		50	—	ns
t _{CY80}		System cycle time		300	—	ns
t _{PWR80}	WR1	Pulse width (read)		85	—	ns
t _{PWW80}	WR0	Pulse width (write)		85	—	ns
t _{HPW80}	WR0, WR1	High pulse width		85	—	ns
t _{DS80}	D0~D7	Data setup time		40	—	ns
t _{DH80}	D0~D7	Data hold time		15	—	ns
t _{ACC80}		Read access time	C _L = 100pF	—	140	ns
t _{OD80}		Output disable time		10	100	ns
t _{CSSA80}	CS1/CS0	Chip select setup time		15	—	ns
t _{CSSD80}	CS1/CS0	Chip select setup time		15	—	ns
t _{CSH80}	CS1/CS0	Chip select setup time		30	—	ns

(VDD=3.0V to 4.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{AS80}	CD	Address setup time		20	—	ns
t _{AH80}	CD	Address hold time		45	—	ns
t _{CY80}		System cycle time		166	—	ns
t _{PWR80}	WR1	Pulse width (read)		65	—	ns
t _{PWW80}	WR0	Pulse width (write)		65	—	ns
t _{HPW80}	WR0, WR1	High pulse width		65	—	ns
t _{DS80}	D0~D7	Data setup time		30	—	ns
t _{DH80}	D0~D7	Data hold time		10	—	ns
t _{ACC80}		Read access time	C _L = 100pF	—	65	ns
t _{OD80}		Output disable time		10	45	ns
t _{CSSA80}	CS1/CS0	Chip select setup time		10	—	ns
t _{CSSD80}	CS1/CS0	Chip select setup time		10	—	ns
t _{CSH80}	CS1/CS0	Chip select setup time		20	—	ns

Parallel bus timing characteristics (for 6800 MCU)

At Ta= 0°C to +50°C

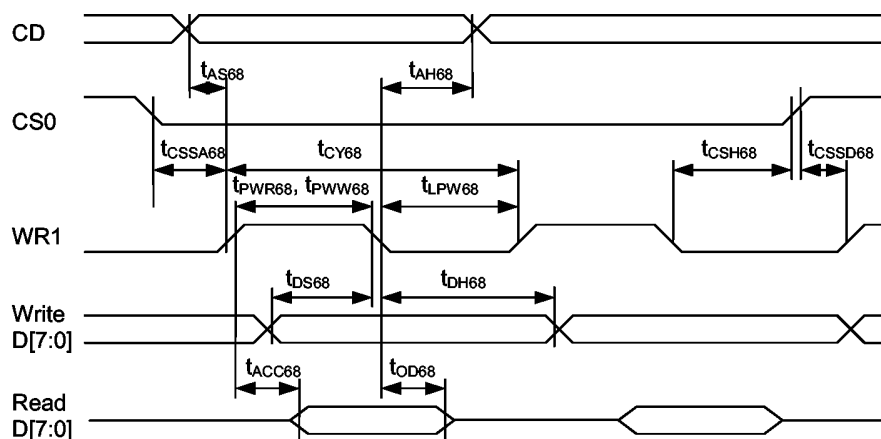


Figure 4 : Parallel Bus Timing Characteristics (for 6800 MCU)

(VDD=2.4V to 3.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{AS68}	CD	Address setup time		25	—	ns
t _{AH68}		Address hold time		50	—	ns
t _{CY68}		System cycle time		300	—	ns
t _{PWR68}	WR1	Pulse width (read)		85	—	ns
t _{PWW68}		Pulse width (write)		85	—	ns
t _{LPW68}		Low pulse width		85	—	ns
t _{DS68}	D0~D7	Data setup time		40	—	ns
t _{DH68}		Data hold time		15	—	ns
t _{ACC68}		Read access time	C _L = 100pF	—	140	ns
t _{OD68}		Output disable time		10	100	ns
T _{CSSA68}	CS1/CS0	Chip select setup time		15	—	ns
T _{CSD68}				15	—	ns
T _{CSH68}				30	—	ns

(VDD=3.0V to 4.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t _{AS68}	CD	Address setup time		20	—	ns
t _{AH68}		Address hold time		45	—	ns
t _{CY68}		System cycle time		166	—	ns
t _{PWR68}	WR1	Pulse width (read)		65	—	ns
t _{PWW68}		Pulse width (write)		65	—	ns
t _{LPW68}		Low pulse width		65	—	ns
t _{DS68}	D0~D7	Data setup time		30	—	ns
t _{DH68}		Data hold time		10	—	ns
t _{ACC68}		Read access time	C _L = 100pF	—	70	ns
t _{OD68}		Output disable time		10	50	ns
T _{CSSA68}	CS1/CS0	Chip select setup time		10	—	ns
T _{CSD68}				10	—	ns
T _{CSH68}				20	—	ns

Serial bus timing characteristics

At Ta= 0°C to +50°C

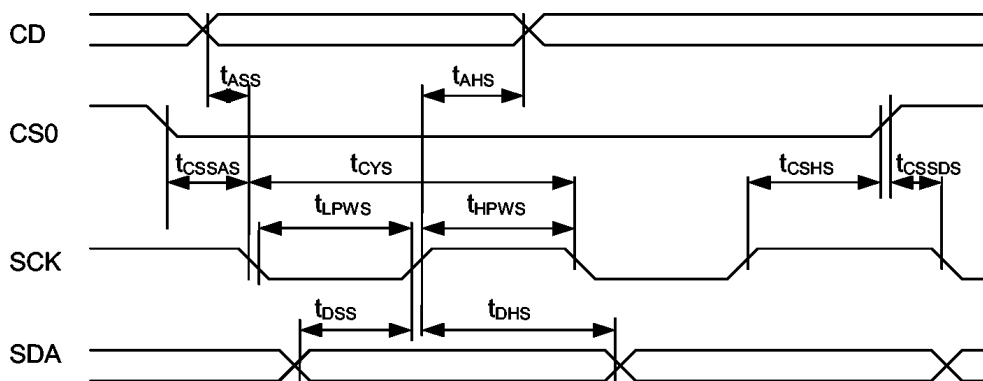


Figure 5 : Serial Bus Timing Characteristics

(VDD=2.4V to 3.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS}	CD	Address setup time		15	—	ns
t_{AHS}		Address hold time		40	—	ns
t_{CYS}	SCK	System cycle time		250	—	ns
t_{LPWS}		Low pulse width		100	—	ns
t_{HPWS}		High pulse width		100	—	ns
t_{DSS}	SDA	Data setup time		90	—	ns
t_{DHS}		Data hold time		90	—	ns
t_{CSSAS}	CS1/CS0	Chip select setup time		10		ns
t_{CSSDS}				10		ns
t_{CSHS}				150		ns

(VDD=3.0V to 4.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS}	CD	Address setup time		10	—	ns
t_{AHS}		Address hold time		20	—	ns
t_{CYS}	SCK	System cycle time		200	—	ns
t_{LPWS}		Low pulse width		75	—	ns
t_{HPWS}		High pulse width		75	—	ns
t_{DSS}	SDA	Data setup time		50	—	ns
t_{DHS}		Data hold time		50	—	ns
t_{CSSAS}	CS1/CS0	Chip select setup time		10		ns
t_{CSSDS}				10		ns
t_{CSHS}				100		ns

Serial bus timing characteristics

At Ta= 0°C to +50°C

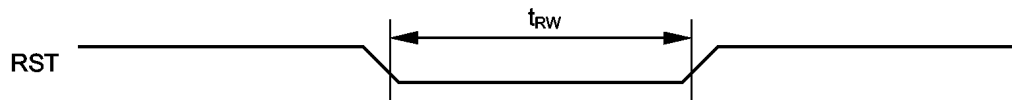


Figure 6 : Reset Characteristics

(VDD=2.4V to 3.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		240	—	ns

(VDD=3.0V to 4.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		200	—	ns

6. APPENDIX

These specifications shall be applied to the White LED-Lamp (LED or LEDs), NSPWF50BS, which is supplied by Nichia Corporation (Nichia).

1.SPECIFICATIONS

(1) Absolute Maximum Rating

(Ta=25℃)

Item	Symbol	Absolute Maximum Rating	Unit
Forward Current	IF	30	mA
Pulse Forward Current	IFP	100	mA
Reverse Voltage	VR	5	V
Power Dissipation	PD	120	mW
Operating Temperature	Topr	-30 ~ +85	℃
Storage Temperature	Tstg	-40 ~ +100	℃
Lead Soldering Temperature	Tsol	260±5℃ for 5sec. (3.0mm from the base of the epoxy bulb)	

IFP Conditions : Pulse Width ≤ 10msec. and Duty ≤ 1/10

(2) Initial Electrical/Optical Characteristics

(Ta=25℃)

Electrical & Optical Characteristics (Ta=25°C)							
Item		Symbol	Condition	Min.	Typ.	Max.	Unit
Forward Voltage		VF	IF=20[mA]	—	3.6	4.0	V
Reverse Current		IR	VR= 5[V]	—	—	50	μ A
Luminous Intensity	Rank S	Iv	IF=20[mA]	300	360	420	mcd
	Rank R	Iv	IF=20[mA]	210	260	300	mcd
	Rank Q	Iv	IF=20[mA]	150	180	210	mcd

※ One delivery will include three different ranks of products. The quantity-ratio of the three ranks is decided by Nichia.

Measurement Uncertainty of the Luminous Intensity : ±10%

Color Ranks

(IF=20mA, Ta=25℃)

	Rank a			
x	0.250	0.250	0.290	0.290
y	0.205	0.250	0.305	0.260

	Rank b			
x	0.290	0.290	0.330	0.330
y	0.260	0.305	0.365	0.320

	Rank c			
x	0.330	0.330	0.370	0.370
y	0.320	0.365	0.420	0.375

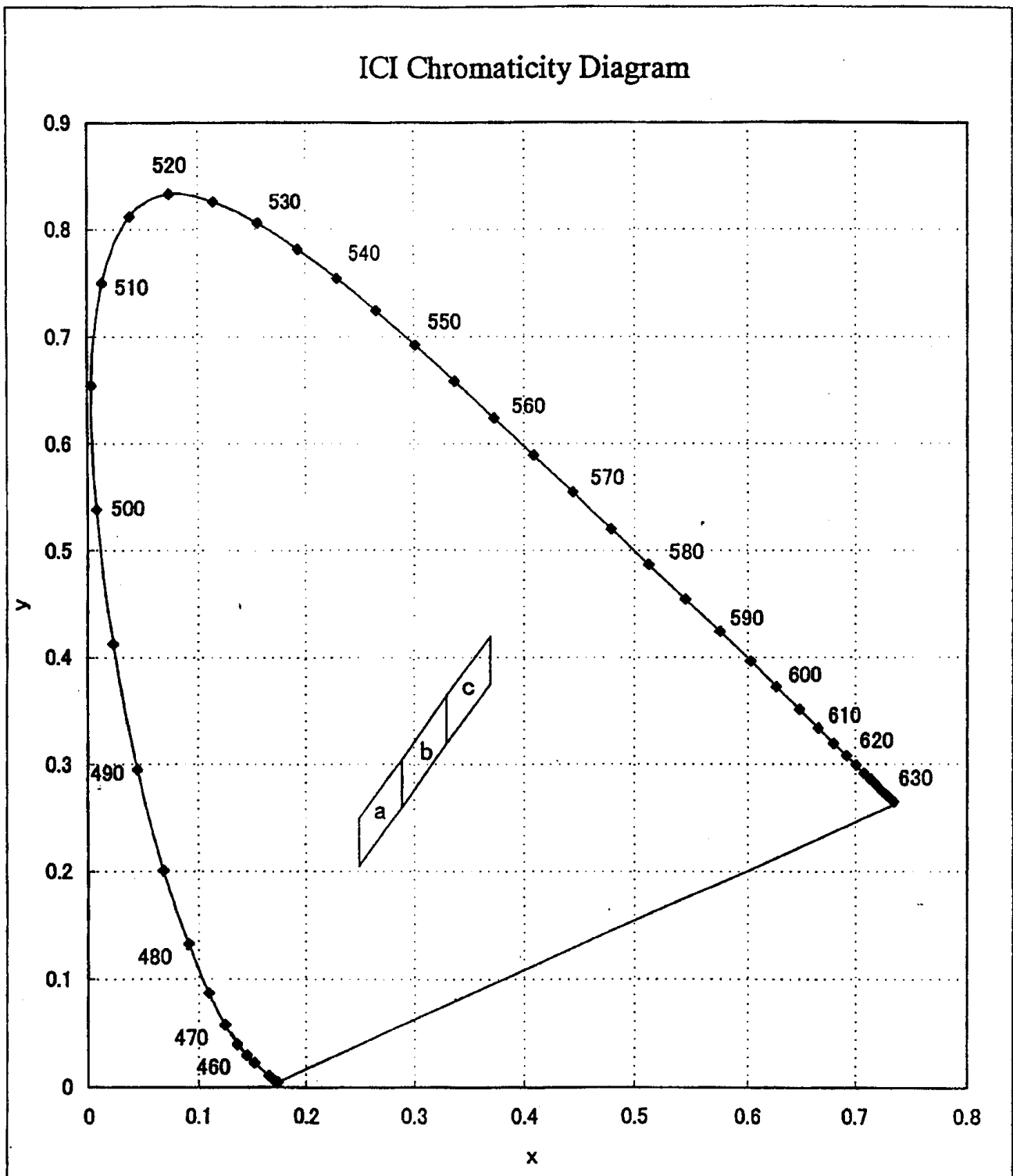
※ One delivery will include the consecutive two ranks of products.

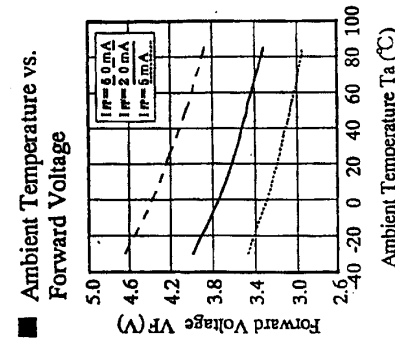
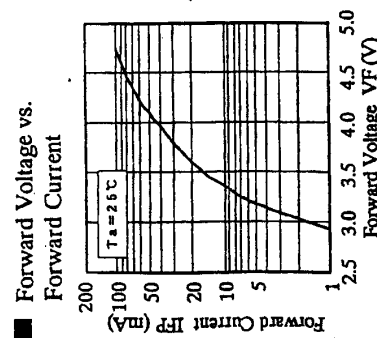
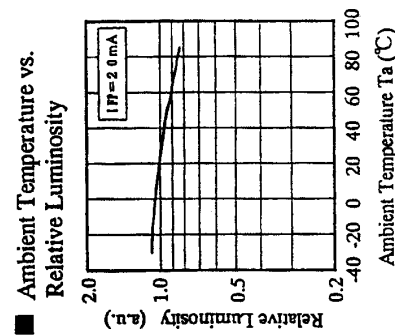
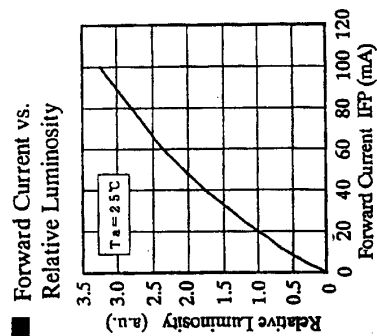
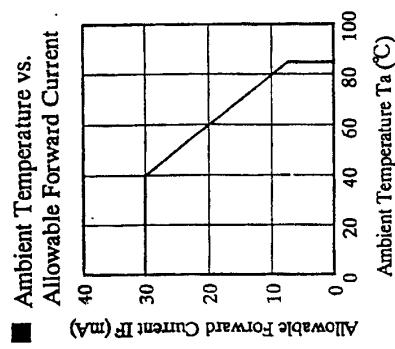
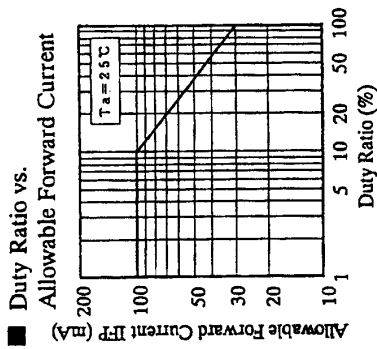
The quantity-ratio of the two ranks is decided by Nichia.

Measurement Uncertainty of the Color Coordinates : ±0.02

2.TYPICAL INITIAL OPTICAL/ELECTRICAL CHARACTERISTICS

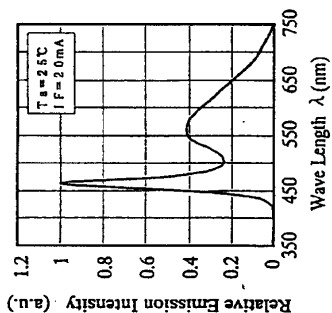
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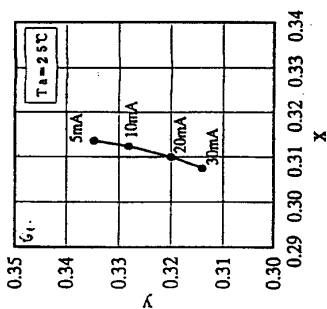


Rev.1	Section	Approve	Check	Draw
Rev.2	ST	Bando	Yanaseki	Tamura
Rev.3	Date	Jun.1,1999		
Rev.4	Model	NSPWxxxx		
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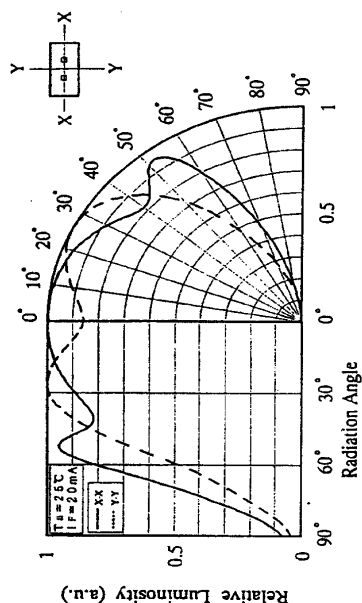
■ Spectrum



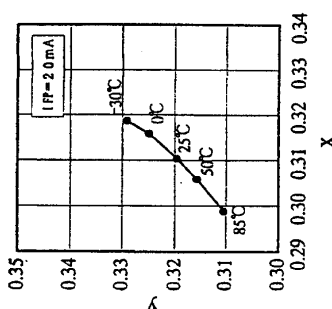
■ Forward Current vs. Chromaticity diagram



■ Directivity (NSPWF50BS)



■ Ambient Temperature vs. Chromaticity diagram



Rev.1	Section	Approve	Check	Draw
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Rev.3		Date	Jun.1.1999	
Rev.4		Model	NSPWF50BS	
NICHIA CORPORATION		Title TYP.CHARACTERISTICS		
		No.	STLZ-A801473	