DOCUMENT NUMBER AND REVISION

VL-PS-COG-BT12864-01 REV. A

(COG-BT12864-G-6; STN, YELLOW, +VE, REFLECTIVE, STD)

DOCUMENT TITLE:

PRELIMINRY SPECIFICATION

OF

LCD MODULE TYPE

CUSTOMER	**DATA MODUL**
MODEL NUMBER	**COG-BT12864-01**
CUSTOMER APPROVAL	
DATE	

DEPARTMENT	NAME	SIGNATURE	DATE
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DISTRIBUTION LIST: MARKETING

DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2002.11.06	First Release. (Based on Test Specification: VL-TS-COG-BT12864-XX, REV. A, 2002.10.28)	PHILIP CHENG	R.S.LIN

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Preliminary Specification
of
LCD Module Type
Item No.: COG-BT12864-01

1. General Description

- 128 x 64 dots STN Yellow Positive Reflective STD LCD Module.
- Viewing Direction: 6 O'clock.
- Driving duty: 1/65 Duty, 1/9 bias.
- 'ULTRA CHIP' UC1606 (COG) LCD Controller-Driver or equivalent.
- Logic Power Supply: +3V.
- FPC.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	67.5(W) x 82.5(H) x 1.98(D)	mm
Effective viewing area (V.A.)	60.00 MIN.(W) x 40.00 MIN.(H)	mm
Active area (A.A.)	56.945(W) x 37.425(H)	mm
Display format	128 x 64	dots
Dot size	0.43(W) x 0.57(H)	mm
Dot spacing	0.015(W) x 0.015(H)	mm
Dot pitch	0.445(W) x 0.585(H)	mm
Weight:	TBD	grams

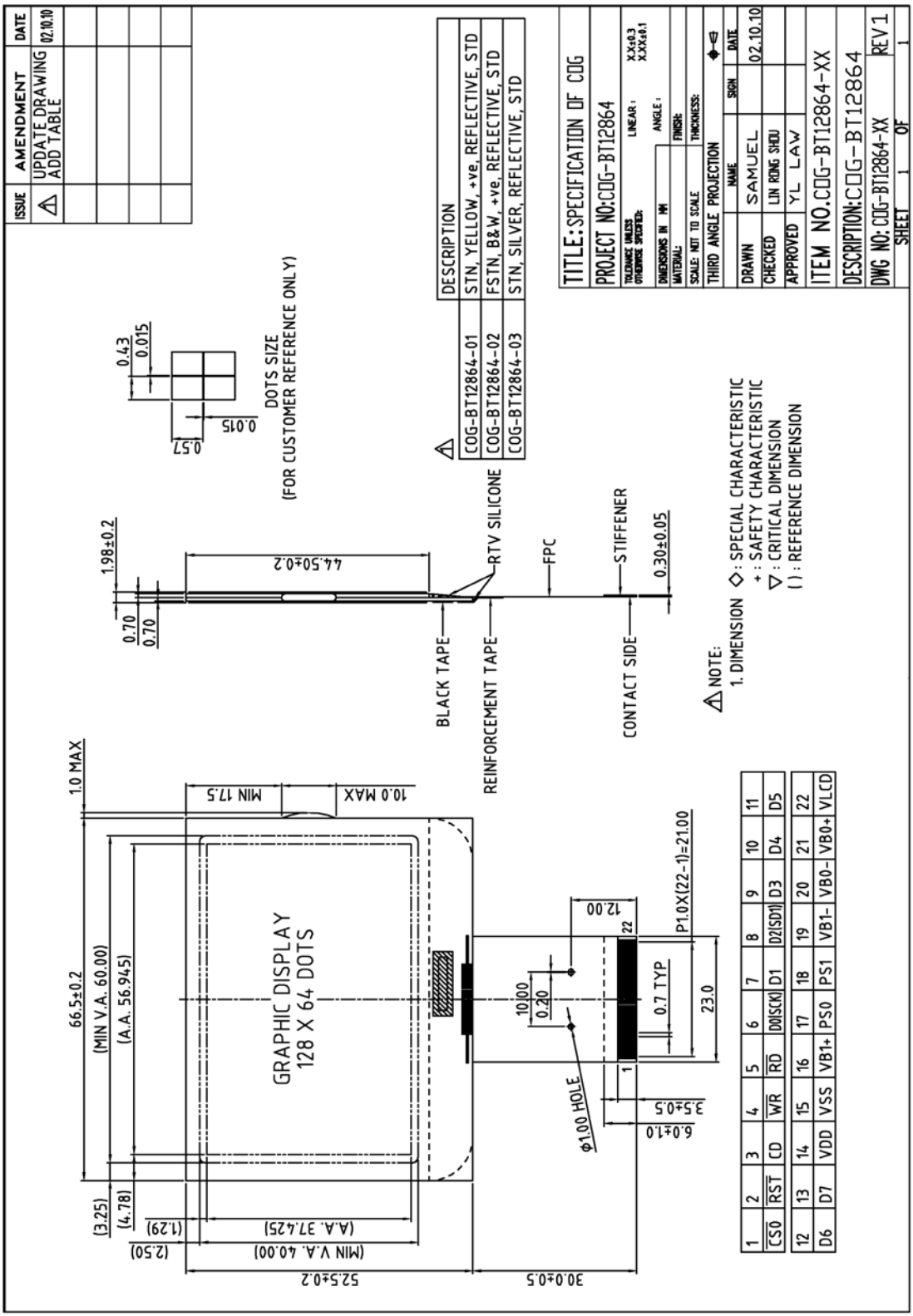

Figure 1: Outline Drawing.

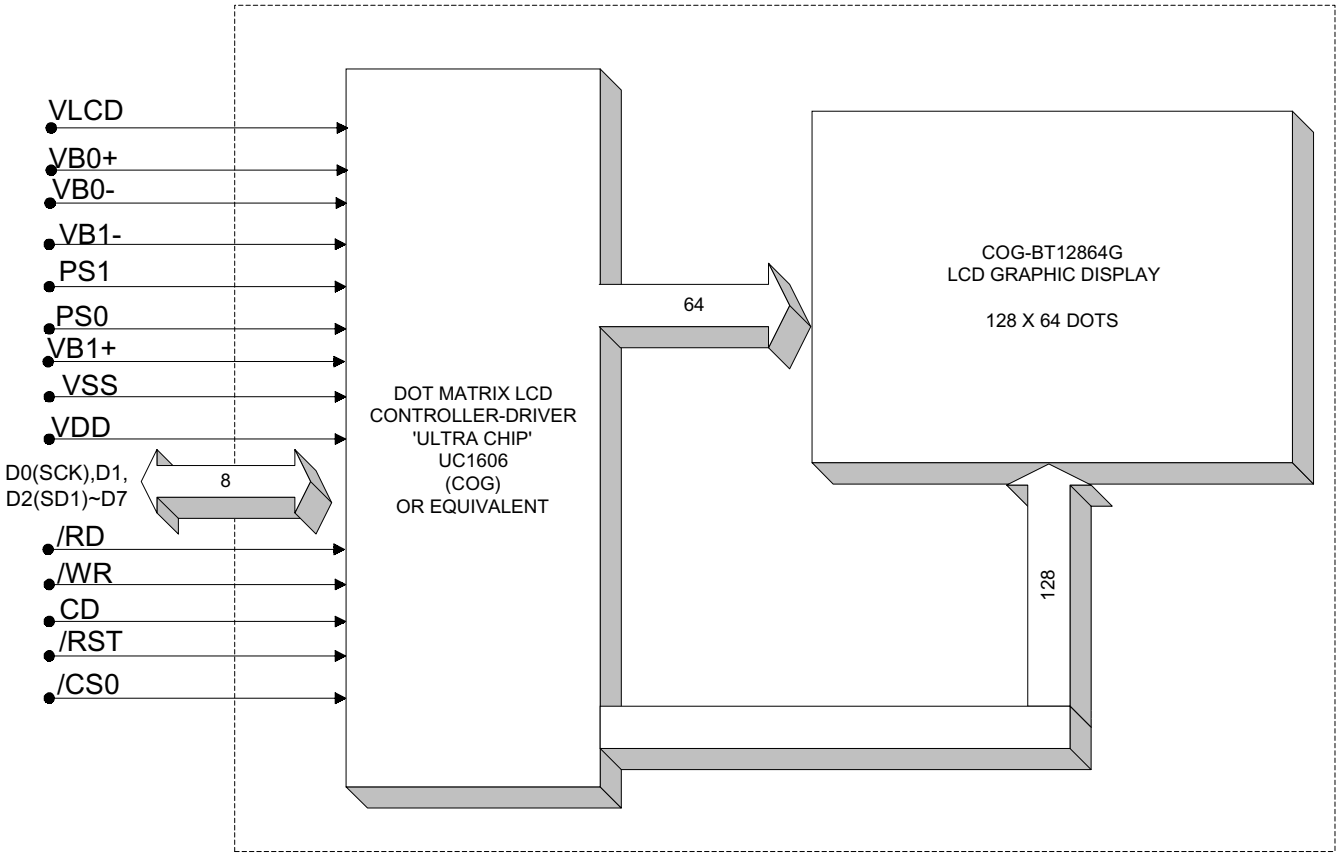

Figure 2: Block diagram

3. Interface signals

Table 2

<table>
<tr><th>Pin No.</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>$\overline{CS0}$</td><td>Chip Select. In parallel mode and S8 mode, chip is selected when $\overline{CS0}$=”L” and CS1=”H”. When the chip is not selected, D[7:0] may be high impedance.</td></tr>
<tr><td>2</td><td>$\overline{RST}$</td><td>When $\overline{RST}$ =”L”, all control registers are re-initialized by their default states. When RST is not used, connect the pin to VDD.</td></tr>
<tr><td>3</td><td>CD</td><td>Select Command or Display Data for read/write operation.
“L”: Command ”H”: Display data</td></tr>
<tr><td>4</td><td>$\overline{WR}$</td><td rowspan="2">$\overline{RD}$/$\overline{WR}$(WR[1:0]) controls the read/write operation of the host interface.
In parallel mode, RD/WR(WR[1:0]) meaning depends on whether the interface is in the 6800 mode or the 8080 mode. In serial interface modes, these two pins are not used. Connect to VSS.</td></tr>
<tr><td>5</td><td>$\overline{RD}$</td></tr>
<tr><td>6</td><td>D0(SCK)</td><td rowspan="8">Bi-directional bus for both serial and parallel host interfaces.
In S8 and S9 mode, connect unused pins to VDD or VSS.
<table>
<tr><th></th><th>PS=1x</th><th>Ps=0x</th></tr>
<tr><td>D0</td><td>D0</td><td>SCK</td></tr>
<tr><td>D1</td><td>D1</td><td></td></tr>
<tr><td>D2</td><td>D2</td><td>SD1</td></tr>
<tr><td>D3</td><td>D3</td><td></td></tr>
<tr><td>D4</td><td>D4</td><td></td></tr>
<tr><td>D5</td><td>D5</td><td></td></tr>
<tr><td>D6</td><td>D6</td><td></td></tr>
<tr><td>D7</td><td>D7</td><td></td></tr>
</table></td></tr>
<tr><td>7</td><td>D1</td></tr>
<tr><td>8</td><td>D2(SD1)</td></tr>
<tr><td>9</td><td>D3</td></tr>
<tr><td>10</td><td>D4</td></tr>
<tr><td>11</td><td>D5</td></tr>
<tr><td>12</td><td>D6</td></tr>
<tr><td>13</td><td>D7</td></tr>
<tr><td>14</td><td>VDD</td><td>VDD1 is the digital power supply and it should be connected to a voltage source that is no higher than VDD2&3.
VDD2&3 is the analog power supply and it should be connected to the same power source. Minimize the trace resistance for VDD2&3.</td></tr>
<tr><td>15</td><td>VSS</td><td>Ground.</td></tr>
<tr><td>17</td><td>PS0</td><td rowspan="2">PS[1:0] Parallel/Serial.
Serial modes: “LL”: serial (S8) “LH”: serial (S9)
Parallel modes: “HL”: 8080 “HH”: 6800</td></tr>
<tr><td>18</td><td>PS1</td></tr>
<tr><td>16</td><td>VB1+</td><td rowspan="4">LCD Bias Voltages. These are the voltage sources to provide SEG driving currents. These voltages are generated internally. Connect capacitors of CBX value between VBX+ and VBX–. The resistance of these four traces directly affects the SEG driving strength of the resulting LCD module. Minimize the trace resistance is critical in achieving high quality image.</td></tr>
<tr><td>19</td><td>VB1-</td></tr>
<tr><td>20</td><td>VB0-</td></tr>
<tr><td>21</td><td>VB0+</td></tr>
<tr><td>22</td><td>VLCD</td><td>Main LCD Power Supply. A by-pass capacitor CL is optional. When CL is used, connect CL between VLCD and VSS, and keep the trace resistance under 300 Ohm.</td></tr>
</table>

4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings(Ta = 25 ºC)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Logic supply voltage	VDD1 - VSS	-0.3	+5.5	V
LCD generator supply voltage	VDD2 - VSS	-0.3	+5.5	V
Analog circuit supply voltage	VDD3 - VSS	-0.3	+5.5	V
LCD generated voltage	VLCD	-0.3	+15.5	V
Any input voltage	Vin	-0.3	VDD+0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

VDD=VDD1=VDD2=VDD3.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	0°C	+50°C	-10°C	+60°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration : 11 ms Peak acceleration: 981 m/s^2 = 100g Number of shocks : 3 shocks in 3 mutually perpendicular axes.				3 directions

5. Electrical Specifications

5.1 Typical Electrical Characteristics

At Ta = 25 °C, VDD = 3V±5%, VSS=0V.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic & booster)	VDD-VSS		2.85	3.0	3.15	V
LCD driving voltage	VLCD-VSS		9.3	9.6	9.9	V
Input signal voltage	V_{IH}	”H” level	0.8 VDD1	-	-	V
	V_{IL}	” L” level	-	-	0.2VDD1	V
Supply Current (Logic & booster)	IDD	Character mode, Note 1	-	0.2	0.3	mA

Note

(1) : There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

5.2 Timing Specifications

Parallel bus timing characteristics (for 8080 MCU)

At Ta= 0°C to +50°C

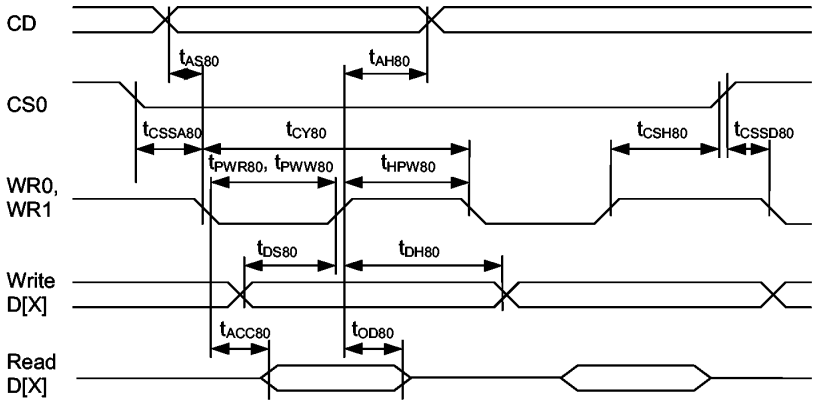

Figure 3 : Parallel Bus Timing Characteristics (for 8080 MCU)

(VDD=2.4V to 3.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		25 50	–	ns
t_{CY80}		System cycle time		300	–	ns
t_{PWR80}	WR1	Pulse width (read)		85	–	ns
t_{PWW80}	WR0	Pulse width (write)		85	–	ns
t_{HPW80}	WR0, WR1	High pulse width		85	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		40 15	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	140 100	ns
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		15 15 30		ns

(VDD=3.0V to 4.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		20 45	–	ns
t_{CY80}		System cycle time		166	–	ns
t_{PWR80}	WR1	Pulse width (read)		65	–	ns
t_{PWW80}	WR0	Pulse width (write)		65	–	ns
t_{HPW80}	WR0, WR1	High pulse width		65	–	ns
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC80} t_{OD80}		Read access time Output disable time	C_L = 100pF	– 10	65 45	ns
t_{CSSA80} t_{CSSD80} t_{CSH80}	CS1/CS0	Chip select setup time		10 10 20		ns

Parallel bus timing characteristics (for 6800 MCU)

At Ta= 0°C to +50°C

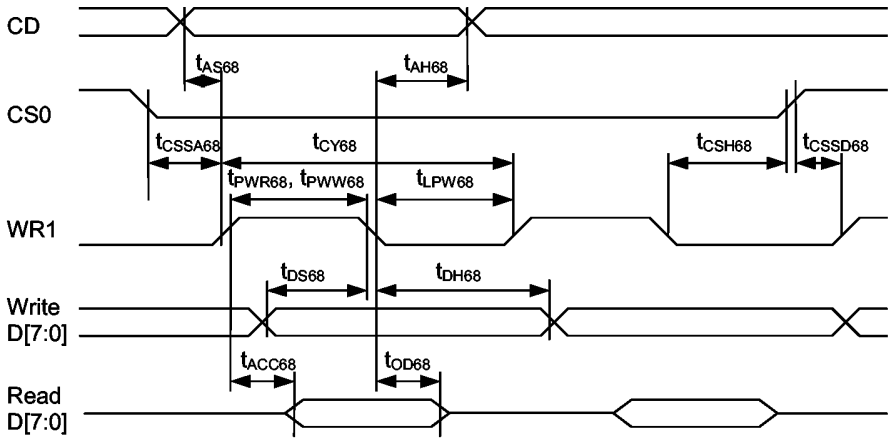

Figure 4 : Parallel Bus Timing Characteristics (for 6800 MCU)

(VDD=2.4V to 3.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		25 50	–	ns
t_{CY68}		System cycle time		300	–	ns
t_{PWR68}	WR1	Pulse width (read)		85	–	ns
t_{PWW68}		Pulse width (write)		85	–	ns
t_{LPW68}		Low pulse width		85	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		40 15	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	140 100	ns
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		15 15 30		ns

(VDD=3.0V to 4.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		20 45	–	ns
t_{CY68}		System cycle time		166	–	ns
t_{PWR68}	WR1	Pulse width (read)		65	–	ns
t_{PWW68}		Pulse width (write)		65	–	ns
t_{LPW68}		Low pulse width		65	–	ns
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 10	–	ns
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 10	70 50	ns
T_{CSSA68} T_{CSSD68} T_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		ns

Serial bus timing characteristics

At Ta= 0°C to +50°C

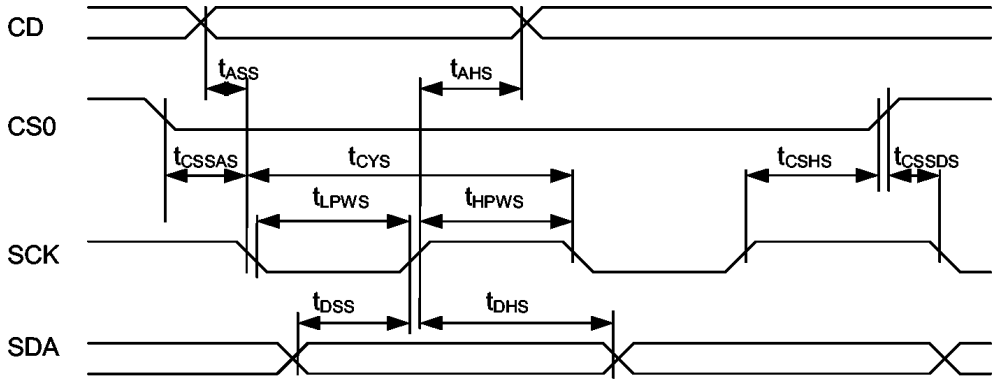

Figure 5 : Serial Bus Timing Characteristics

(VDD=2.4V to 3.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS}	CD	Address setup time		15	–	ns
t_{AHS}		Address hold time		40	–	ns
t_{CYS}	SCK	System cycle time		250	–	ns
t_{LPWS}		Low pulse width		100	–	ns
t_{HPWS}		High pulse width		100	–	ns
t_{DSS} t_{DHS}	SDA	Data setup time Data hold time		90 90	–	ns
t_{CSSAS} t_{CSSDS} t_{CSHS}	CS1/CS0	Chip select setup time		10 10 150		ns

(VDD=3.0V to 4.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS}	CD	Address setup time		10	–	ns
t_{AHS}		Address hold time		20	–	ns
t_{CYS}	SCK	System cycle time		200	–	ns
t_{LPWS}		Low pulse width		75	–	ns
t_{HPWS}		High pulse width		75	–	ns
t_{DSS} t_{DHS}	SDA	Data setup time Data hold time		50 50	–	ns
t_{CSSAS} t_{CSSDS} t_{CSHS}	CS1/CS0	Chip select setup time		10 10 100		ns

Serial bus timing characteristics

At Ta= 0°C to +50°C

Figure 6 : Reset Characteristics

(VDD=2.4V to 3.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		240	–	ns

(VDD=3.0V to 4.0V)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		200	–	ns