SPECIFICATION

FOR

LCD MODULE TYPE

ITEM NO.: BT 21605AVB-03

BT 21605AVB-YETF-LED04-I2C(HD66717) WITHOUT CONNECTOR

(DOC. REVISION 0.0)

DEPARTMENT	NAME	SIGNATURE	EFFECTIVE DATE
PREPARED BY	PHILIP CHENG		2000.11.03
APPROVED BY	K.P.HO		2000.11.03

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DOCUMENT REVISION HISTORY

DOCUMENT REVISION FROM TO	DATE (YY.MM.DD)	DESCRIPTION	CHANGED BY	CHECKED BY
0.0	2000.11.03		PHILIP CHENG	JOE LAM

CONTENT

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1. General Description

- 2 lines x 16 characters in a 5 x 8 dot matrix STN Positive Green-Yellow Transflective LCD Character Module.
- Driving scheme: 1/34 multiplexed drive, 1/6 bias.
- Optimal view direction: 6 o'clock.
- Driving IC : 'HITACHI' HCD66717A03BP (Gold Bump) or equivalent LCD Controller/Driver.
- Serial interfacing: I^2C-bus or clock-synchronized serial interface.
- Built-in Booster circuit.
- Temperature compensation.
- Yellow-green LED04 backlight.

2. Mechanical Specifications

The mechanical detail is shown in Figure 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	80.0(W) x 36.0(H) x 13.0 MAX.(D)	mm
Viewing area	61.0(W) x 15.8(H)	mm
Display format	2 lines x 16 characters (5 x 8 dots)	-
Character size	2.95(W) x 5.55(H)	mm
Character spacing	0.60(W) x 0.40(H)	mm
Character pitch	3.55(W) x 5.95(H)	mm
Dot size	0.55(W) x 0.65(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.60(W) x 0.70(H)	mm
Weight	Approx. 36.6	grams

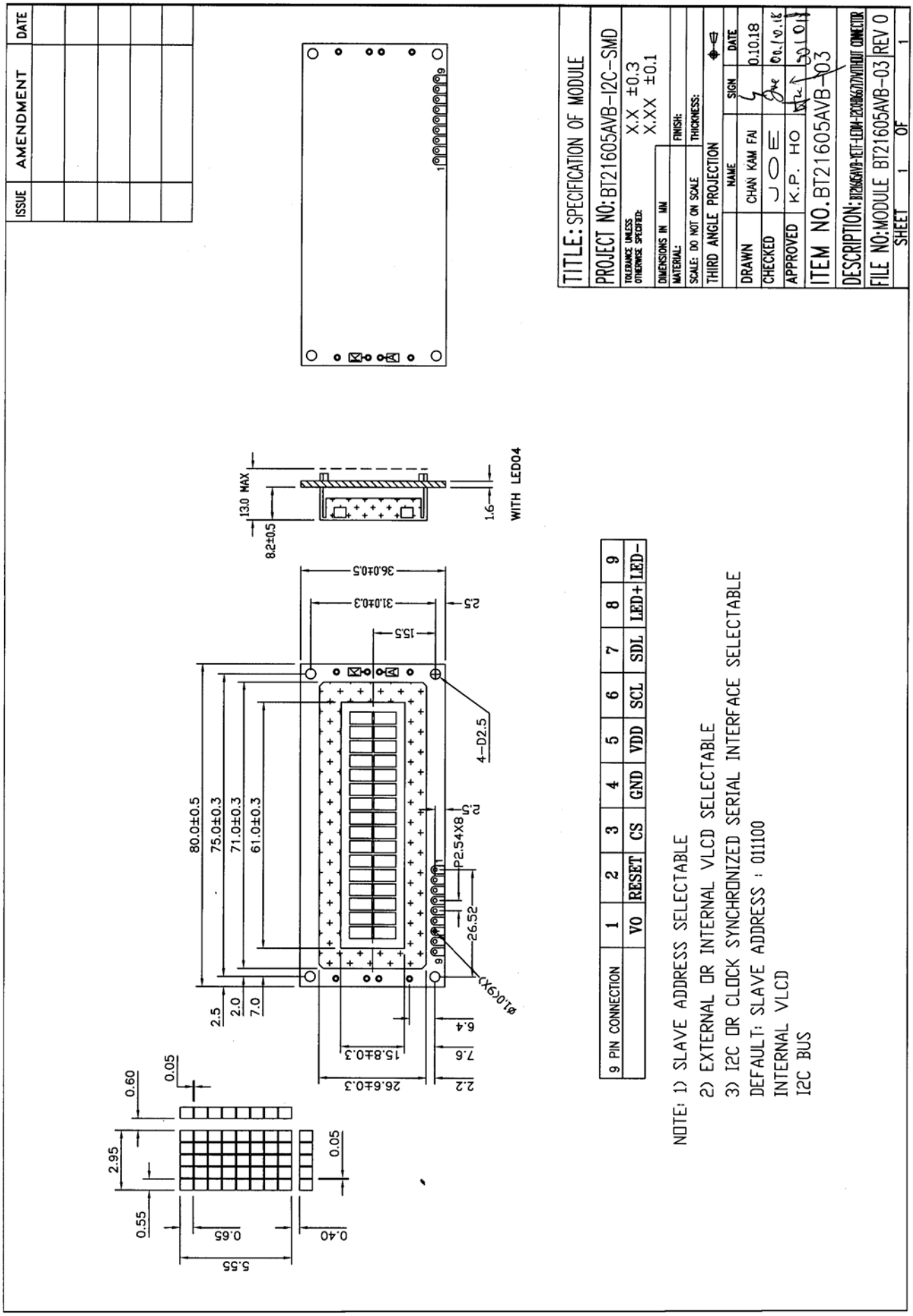


Figure 1: Outline drawing.

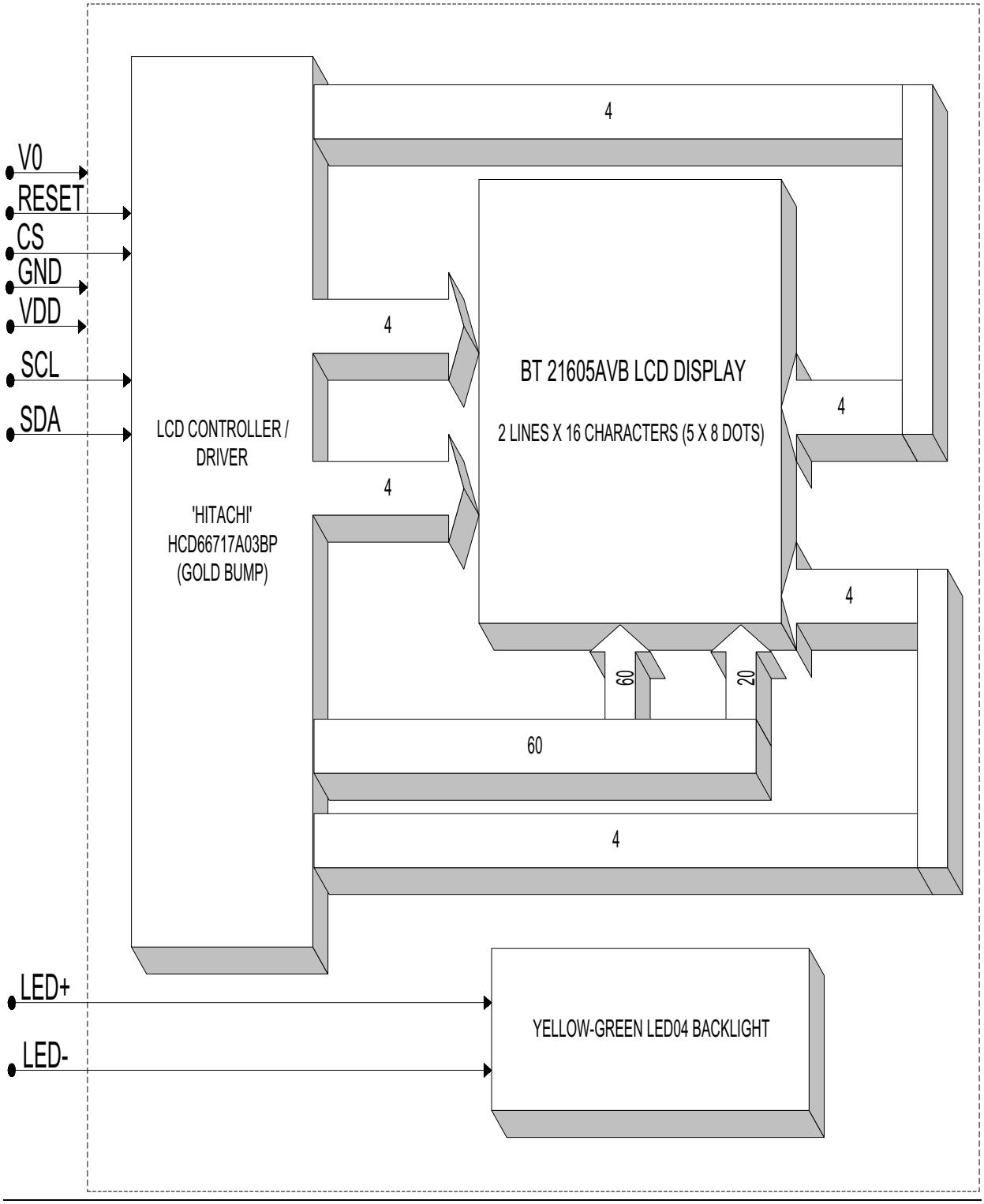


Figure 2: Block Diagram

3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings (Ta = +25 °C)

Table 2

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage range (Logic)	VDD - GND	-0.3	+7.0	V	1
Supply voltage	VDD-V0	-0.3	+15.0	V	1,2
Input voltage range	Vi	-0.3	VDD +0.3	V	1

Note
1) The modules may be destroyed if they are used beyond the absolute maximum ratings.
All voltage values are referenced to GND = 0V.

2.) VDD≧V1≧V2≧V3≧V4≧V5≧V0 must be maintained.

3.2 Environmental Conditions

Table 3

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity	Note 1		Note 1		no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Note 2		Note 2		3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Note 3		Note 3		3 directions

Note 1: 95% max. RH for Ta ≤ 40°C
< 95% RH for Ta > 40°C

Note 2: Frequency: 10 ~ 55 Hz
Amplitude: 0.75 mm
Duration: 20 cycles in each direction.

Note 3: Pulse duration: 11 ms
Peak acceleration: 981 m/s^2 = 100g
Number of shocks: 3 shocks in 3 mutually perpendicular axes.

4. Electrical Specifications

4.1 Interface signals

Table 4: Pin assignment of 9 pin connection

Pin No.	Symbol	Description
1	V0	Negative power supply for LCD driving voltage.
2	RESET	Reset pin. Initializes the LSI when low.
3	CS	Selects the HD66717 during clock-synchronized serial mode: Low: HD66717 is selected and can be accessed. High: HD66717 is not selected and cannot be accessed. Must be grounded (CS="L") for I^2C bus mode.
4	GND	Ground (0V)
5	VDD	Power supply for logic.
6	SCL	Inputs serial clock pulses during I^2C bus mode and clock-synchronized serial mode.
7	SDL	Inputs serial (receive) data and outputs the acknowledge bit during I^2C bus mode; Inputs serial (receive) data during clock-synchronized serial mode.
8	LED+	Anode of LED backlight
9	LED-	Cathode of LED backlight

4.2 Typical Electrical Characteristics

At Ta = +25 °C, VDD = +3.0V±5%, GND=0V.

Table 5(A)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage (Logic)	VDD-GND		2.85	3.0	3.15	V
Operating voltage for LCD	V_{LCD} =VDD-V5	VDD=3V, Note 1 & 2	6.9	7.2	7.5	V
Operating supply current (Logic & LCD)	I_{DD}	VDD=3V, Checker board mode	-	0.3	0.45	mA
Operating current for negative LCD power supply	I0	VDD=3V, Checker board mode, Note 1	-	0.06	0.1	mA
Input signal voltage low	V_{IL}	VDD=2.85V to 3.0V	-0.3	-	0.5VDD	V
		VDD=3.0V to 3.15V	-0.3	-	0.6	
Input signal voltage high	V_{IH}		0.7VDD	-	VDD	V
Supply voltage of yellow-green LED04 backlight	VLED	Supply current =90mA. Number of LED chips=18.	3.8	4.1	4.5	V

At Ta = +25 °C, VDD = +5.0V±5%, GND=0V.

Table 5(B)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage (Logic)	VDD-GND		4.75	5.0	5.25	V
Operating voltage for LCD	V_{LCD} =VDD-V5	VDD=5V, Note 1 & 2	6.9	7.2	7.5	V
Operating supply current (Logic & LCD)	I_{DD}	VDD=5V, Checker board mode	-	0.6	0.9	mA
Operating current for negative LCD power supply	I0	VDD=5V, Checker board mode, Note 1	-	0.06	0.1	mA
Input signal voltage low	V_{IL}		-0.3	-	0.6	V
Input signal voltage high	V_{IH}		0.7VDD	-	VDD	V
Supply voltage of yellow-green LED04 backlight	VLED	Supply current =90mA. Number of LED chips=18.	3.8	4.1	4.5	V

Note 1:
There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Note 2:
V5 is represented by the test point V0 in the silk screen in PCB.

4.3 Timing Specifications

I²C Bus Interface Operation

At Ta = -20 °C to +70 °C, VDD = +3.0V±5%, GND=0V.
Refer to Fig.2, I²C Bus interface timing diagram.

Table 6

Item	Symbol	Min	Typ	Max	Unit	Test Condition
SCL clock cycle time	t_{SCL}	2	—	20	µs	Figure 2
SCL clock high-level width	t_{SCLH}	500	—	—	ns	
SCL clock low-level width	t_{SCLL}	1000	—	—		
SCL/SDA rise/fall time	t_{Sr}, t_{Sf}	—	—	300		
Bus free time	t_{BUF}	140	—	—		
Start hold time	t_{STAH}	500	—	—		
Retransmit start set-up time	t_{STAS}	500	—	—		
Stop set-up time	t_{STOS}	500	—	—		
SDA data set-up time	t_{SDAS}	140	—	—		
SDA data hold time	t_{SDAH}	0	—	—		

At Ta = -20 °C to +70 °C, VDD = +5.0V±5%, GND=0V.
Refer to Fig.2, I²C Bus interface timing diagram.

Table 7

Item	Symbol	Min	Typ	Max	Unit	Test Condition
SCL clock cycle time	t_{SCL}	2	—	20	µs	Figure 2
SCL clock high-level width	t_{SCLH}	500	—	—	ns	
SCL clock low-level width	t_{SCLL}	1000	—	—		
SCL/SDA rise/fall time	t_{Sr}, t_{Sf}	—	—	300		
Bus free time	t_{BUF}	100	—	—		
Start hold time	t_{STAH}	500	—	—		
Retransmit start set-up time	t_{STAS}	500	—	—		
Stop set-up time	t_{STOS}	500	—	—		
SDA data set-up time	t_{SDAS}	100	—	—		
SDA data hold time	t_{SDAH}	0	—	—		

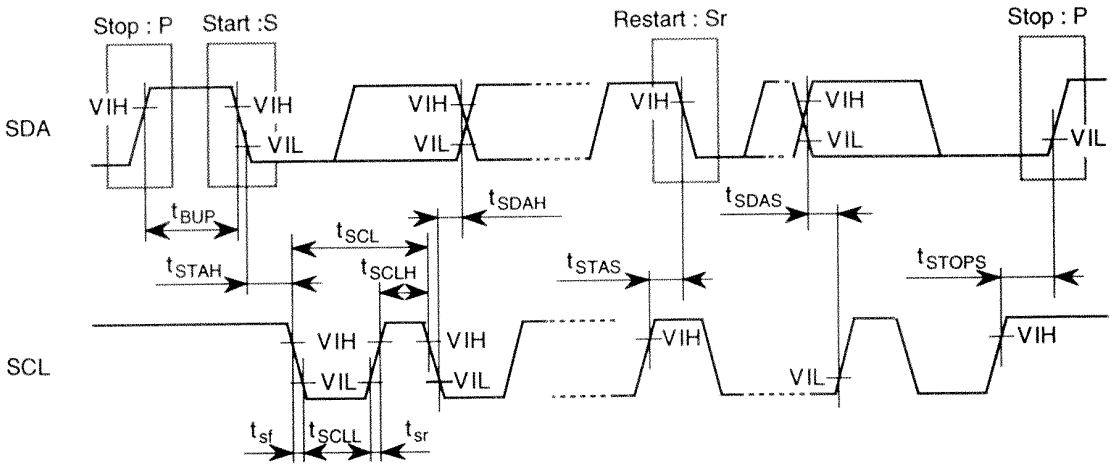


Figure 2 : I²C Bus Interface Timing.

Clock-Synchronized Serial Interface Operation

At Ta = -20 °C to +70 °C, VDD = +3.0V±5% or VDD = +5.0V±5%, GND=0V.

Refer to Fig.3, Clock-Synchronized Serial Interface Timing.

Table 8

Item	Symbol	Min	Typ	Max	Unit	Test Condition
Serial clock cycle time	t_{SCYC}	1	—	20	µs	Figure 3
Serial clock high-level width	t_{SCH}	400	—	—	ns	
Serial clock low-level width	t_{SCL}	400	—	—		
Serial clock rise/fall time	t_{SCr}, t_{SCf}	—	—	50		
Chip select set-up time	t_{CSU}	60	—	—		
Chip select hold time	t_{CH}	200	—	—		
Serial input data set-up time	t_{SISU}	200	—	—		
Serial input data hold time	t_{SIH}	200	—	—		

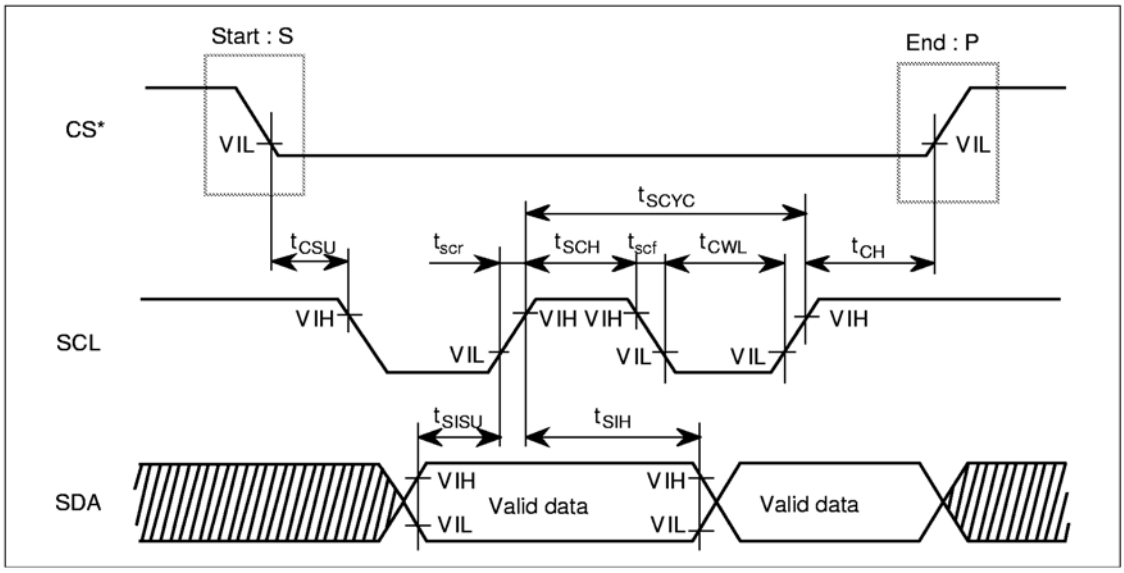


Figure 3: Clock-Synchronized Serial Interface Timing

Reset Timing

At Ta = -20 °C to +70 °C, VDD=+3.0V±5% or VDD=+5.0V±5%, GND=0V.
Refer to Fig.4, Reset timing diagram.

Table 9

Parameters	Symbol	Min.	Typ.	Max.	Unit
Reset low-level width	t_{RES}	10	-	-	ms

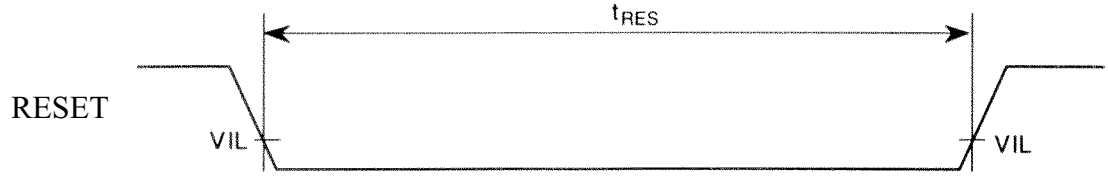
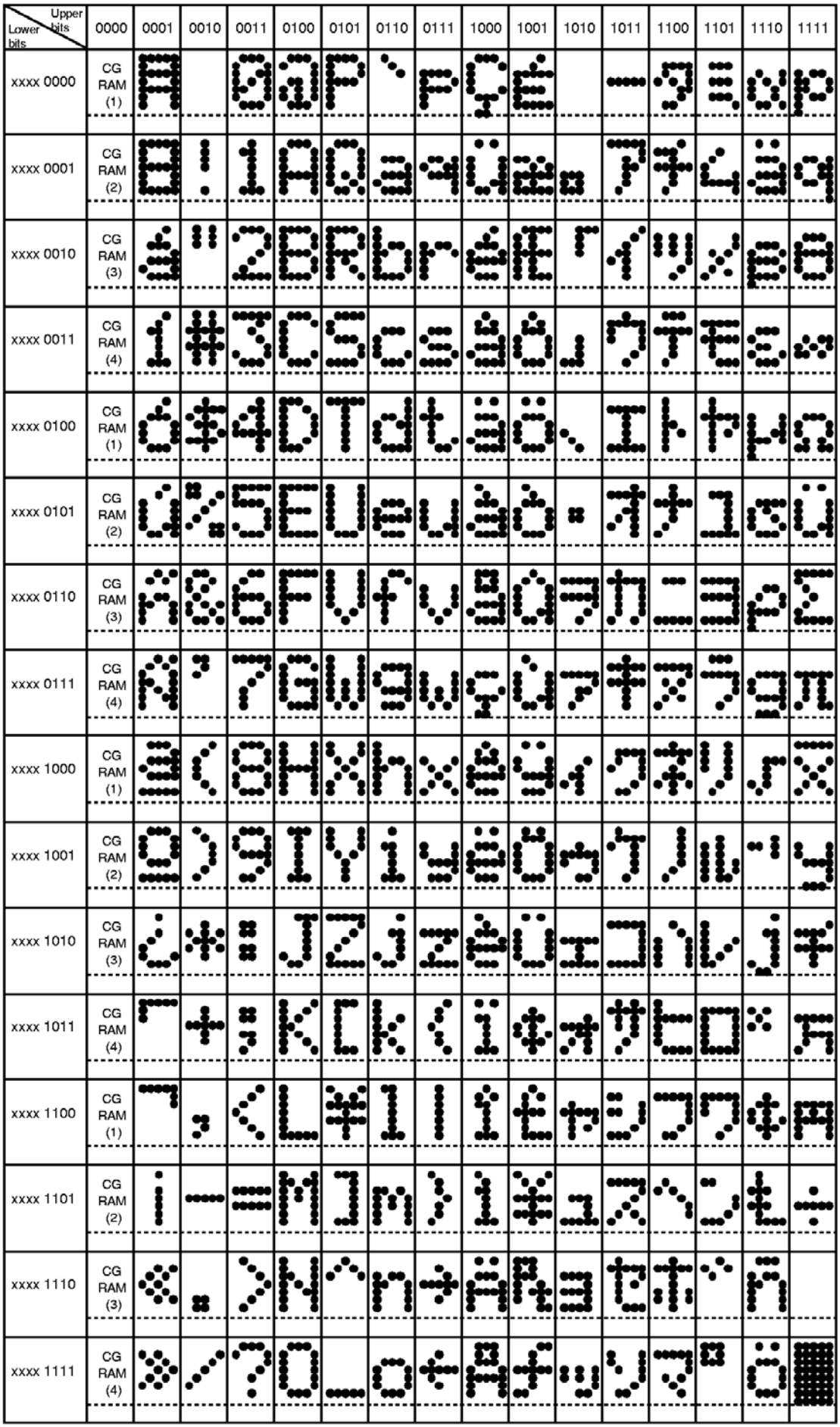


Figure 4 : Reset Timing Diagram

4.4 Relation between Character Codes and Character Patterns (ROM code: A03)



4.5 Slave Address Selectable. (Jumper Set)

	ID 5	ID4	ID3	ID2	ID1	ID0
1	JP1	JP3	JP5	JP7	JP9	JP11
0	JP2	JP4	JP6	JP8	JP10	JP12

Default. 011100 Short JP 2, 3, 5, 7, 10, 12

4.6 I^2C or Clock Synchronized Serial Interface Selectable

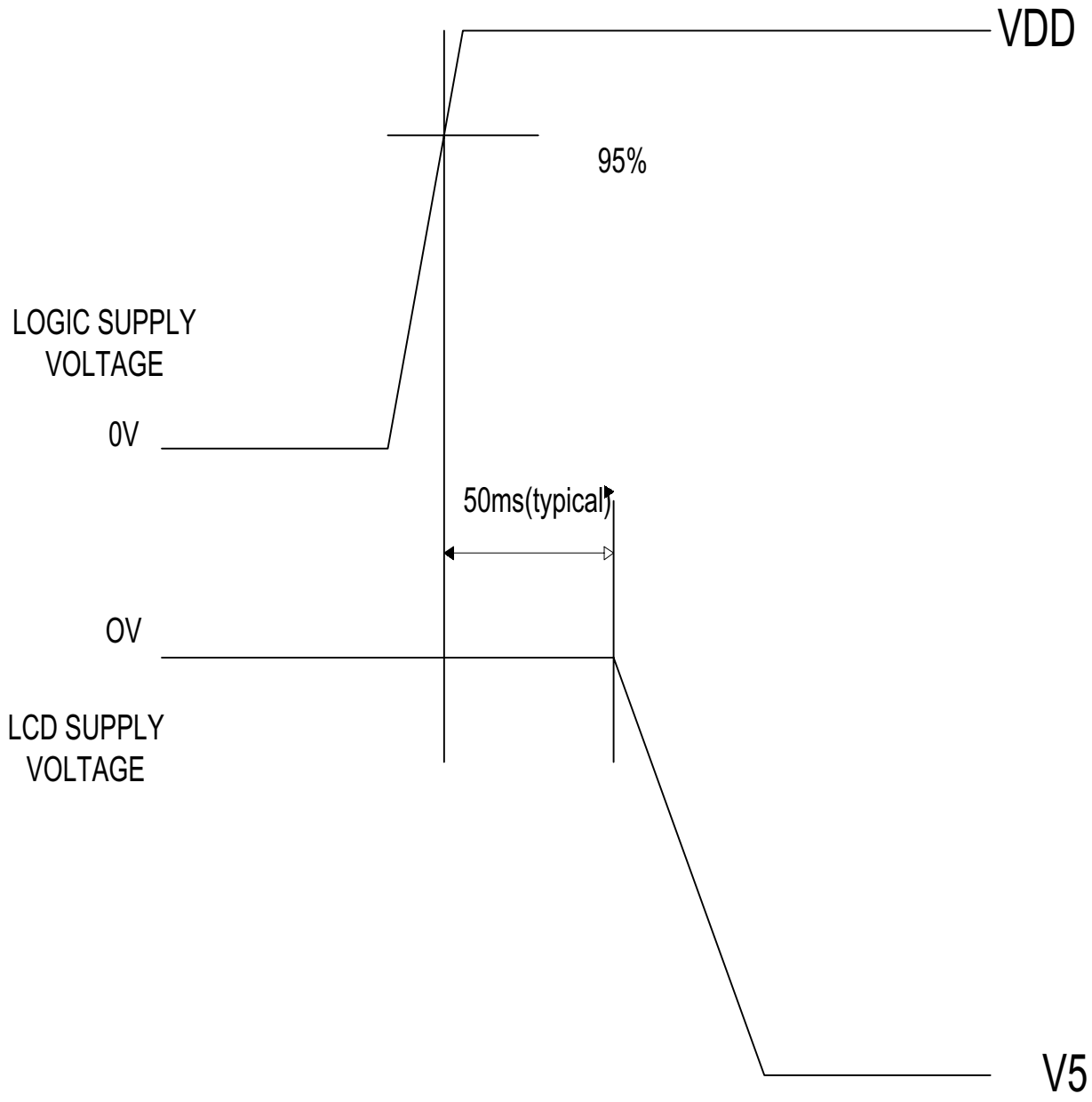
	Short	Open
I^2C (Default)	JP15, 17, 21	Jp22
Clock Synchronized Serial	JP14, 17, 22	JP21

4.7 External or Internal VLCD Selectable

	Open	Short
External VLCD (V0)	JP 18, 19, 20	/
Internal VLCD (5V Input)	JP 13,18, 19	JP 20
Internal VLCD (3V Input)	JP 20	JP 13,18, 19

4.8 Timing Diagram of V_{DD} Against V5.

Power on sequence shall meet the requirement of Figure 5, the timing diagram of V_{DD} against V5.



Note :
V5 is represented by the test point V0 in the silk screen in PCB.

Figure 5: Timing Diagram of V_{DD} Against V5.