



DRAM

256K x 4 DRAM

FAST PAGE MODE

AVAILABLE AS MILITARY SPECIFICATION

- SMD 5962-90617
- MIL-STD-883

FEATURES

- Industry standard pinout and timing
- All inputs, outputs and clocks are fully TTL compatible
- Single +5V±10% power supply
- Low power, 5mW standby; 175mW active, typical
- Optional FAST PAGE MODE access cycle
- Refresh modes: RAS\-ONLY, CAS\-BEFORE-RAS\ and HIDDEN
- 512-cycle refresh distributed across 8ms
- Specifications guaranteed over full military temperature range (-55°C to +125°C)

OPTIONS

- **Timing**
80ns access
100ns access
120ns access

- **Packages**

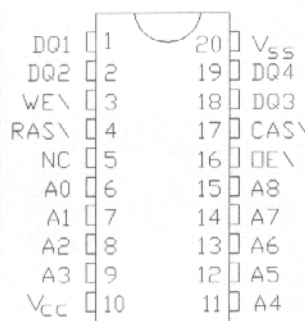
Ceramic DIP (300 mil)
Ceramic LCC
Ceramic Flatpack

MARKING

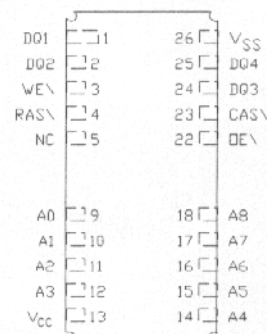
C	No. 103
EC	No. 202
F	No. 301

PIN ASSIGNMENT (Top View)

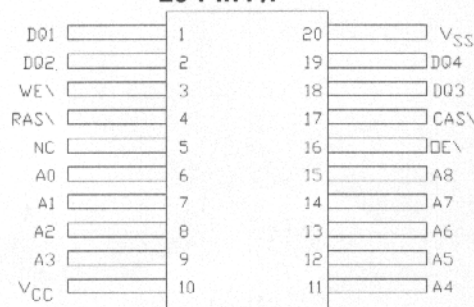
20-Pin LCC



20-Pin DIP



20-Pin F/P



GENERAL DESCRIPTION

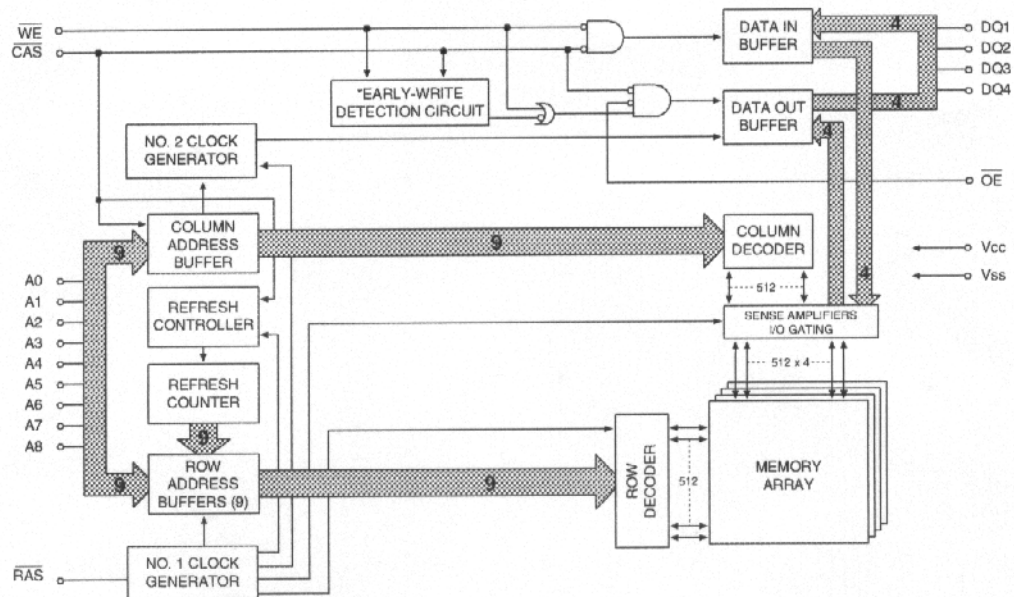
The AS4C4256 883C is a randomly accessed solid-state memory containing 1,048,576 bits organized in a 262,144 x 4 configuration. During READ or WRITE cycles, each 4-bit word is uniquely addressed through the 18 address bits which are entered 9 bits (A0-A8) at a time. RAS\ is used to latch the first 9 bits and CAS\ the latter 9 bits. A READ or WRITE cycle is selected with the WE\ input. A logic HIGH on WE\ dictates READ mode while a logic LOW on WE\ dictates WRITE mode. During a WRITE cycle, data in (D) is latched by the falling edge of WE\ or CAS\, whichever occurs last. If WE\ goes LOW prior to CAS\ going LOW, the output pins (Qs) remain open (High-Z) until the next CAS\ cycle. If WE\ goes LOW after data reaches the outputs (Qs), the outputs are activated and retain the selected cells' data as long as CAS\ remains LOW (regardless of WE\ or RAS\). This late WE\ pulse results in a READ-WRITE cycle. The four data inputs and four data outputs are routed through four leads using common I/O, and information

direction is controlled by WE\ and OE\.

FAST PAGE MODE operations allow faster data operations (READ, WRITE or READ-MODIFY-WRITE) within a row address (A0 -A8) defined page boundary. The FAST PAGE MODE cycle is always initiated with a row address strobed-in by RAS\ followed by a column address strobed-in by CAS\.

CAS\ may be toggled-in by holding RAS\ LOW and strobing-in different column addresses, thus executing faster memory cycles. Returning RAS\ HIGH terminates the FAST PAGE MODE operation. Returning RAS\ and CAS\ HIGH terminates a memory cycle and decreases chip current to a reduced standby level. Also, the chip is preconditioned for the next cycle during the RAS\ high time. Memory cell data is retained in its correct state by maintaining power and executing any RAS\ cycle (READ, WRITE, RAS\-ONLY, CAS\-BEFORE-RAS\, or HIDDEN refresh) so that all 512 combinations of RAS\ addresses (A0-A8) are executed at least every 8ms, regardless of sequence.



FUNCTIONAL BLOCK DIAGRAM
FAST PAGE MODE

*NOTE: $\overline{WE}$ LOW prior to $\overline{CAS}$ LOW, EW detection circuit output is a HIGH (EARLY-WRITE)
 $\overline{CAS}$ LOW prior to $\overline{WE}$ LOW, EW detection circuit output is a LOW (LATE-WRITE)

TRUTH TABLE

FUNCTION		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	ADDRESSES		DATA IN/OUT
						t_R	t_C	DQ1-DQ4
Standby		H	H→X	X	X	X	X	High-Z
READ		L	L	H	L	ROW	COL	Data Out
EARLY-WRITE		L	L	L	X	ROW	COL	Data In
READ-WRITE		L	L	H→L	L→H	ROW	COL	Data Out, Data In
FAST-PAGE-MODE READ	1st Cycle	L	H→L	H	L	ROW	COL	Data Out
	2nd Cycle	L	H→L	H	L	n/a	COL	Data Out
FAST-PAGE-MODE EARLY-WRITE	1st Cycle	L	H→L	L	X	ROW	COL	Data In
	2nd Cycle	L	H→L	L	X	n/a	COL	Data In
FAST-PAGE-MODE READ-WRITE	1st Cycle	L	H→L	H→L	L→H	ROW	COL	Data Out, Data In
	2nd Cycle	L	H→L	H→L	L→H	n/a	COL	Data Out, Data In
$\overline{RAS}$ -ONLY REFRESH		L	H	X	X	ROW	n/a	High-Z
HIDDEN REFRESH	READ	L→H→L	L	H	L	ROW	COL	Data Out
	WRITE	L→H→L	L	L	X	ROW	COL	Data In
$\overline{CAS}$ -BEFORE- $\overline{RAS}$ REFRESH		H→L	L	H	X	X	X	High-Z

**ABSOLUTE MAXIMUM RATINGS***

Voltage on Any Pin Relative to Vss -1.5V to +7.0V
 Storage Temperature Range -65°C to +150°C
 Power Dissipation 1W
 Lead Temperature (Soldering 5 Seconds) 270°C
 Junction Temperature (T_j) +175°C
 Short Circuit Output Current 50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC ELECTRICAL PERFORMANCE CHARACTERISTICS

(Notes: 1, 6, 7) (-55°C ≤ T_C ≤ +125°C; V_{CC} = 5V ± 10%)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V _{CC}	4.5	5.5	V	
Input High (Logic 1) Voltage, All Inputs	V _{IH}	2.4	V _{CC} +0.5	V	
Input Low (Logic 0) Voltage, All Inputs	V _{IL}	-0.5	0.8	V	
INPUT LEAKAGE CURRENT Any Input (0V ≤ V _{IN} ≤ 6.5V), All other pins not under test = 0V	I _I	-5	5	μA	
OUTPUT LEAKAGE CURRENT (Q is Disabled, 0V ≤ V _{OUT} ≤ 6.5V)	I _{OZ}	-5	5	μA	
OUTPUT LEVELS Output High Voltage (I _{OUT} = -5mA)	V _{OH}	2.4		V	
Output Low Voltage (I _{OUT} = 4.2mA)	V _{OL}		0.4	V	

PARAMETER/CONDITION	SYMBOL	MAX			UNITS	NOTES
		-8	-10	-12		
STANDBY CURRENT: (TTL) ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$)	I _{CC1}	3	3	3	mA	
STANDBY CURRENT: (CMOS) ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2V$; all other inputs = V _{CC} -0.2V)	I _{CC2}	1	1	1	mA	
OPERATING CURRENT: Random READ/WRITE Average power supply current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling: t _{RC} = t _{RC} (MIN))	I _{CC3}	90	80	70	mA	3, 4
OPERATING CURRENT: FAST PAGE MODE Average power supply current ($\overline{\text{RAS}} = V_{IL}$, $\overline{\text{CAS}}$, Address Cycling: t _{PC} = t _{PC} (MIN))	I _{CC4}	70	60	50	mA	3, 4
REFRESH CURRENT: $\overline{\text{RAS}}$ -ONLY Average power supply current ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{IH}$: t _{RC} = t _{RC} (MIN))	I _{CC5}	90	80	70	mA	3
REFRESH CURRENT: $\overline{\text{CAS}}$ -BEFORE- $\overline{\text{RAS}}$ Average power supply current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling: t _{RC} = t _{RC} (MIN))	I _{CC6}	90	80	70	mA	3, 5



CAPACITANCE

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Input Capacitance: (A0-A8), D	C _{i1}		7	pF	2
Input Capacitance: RAS, CAS, WE, OE	C _{i2}		7	pF	2
Input/Output Capacitance: (DQ1-DQ4)	C _o		8	pF	2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) (-55°C ≤ T_C ≤ +125°C; V_{CC} = 5V ±10%)

AC CHARACTERISTICS		-8		-10		-12		UNITS	NOTES
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX		
Random READ or WRITE cycle time	¹ RC	150		180		210		ns	
READ-WRITE cycle time	¹ RWC	195		235		275		ns	
FAST-PAGE-MODE READ or WRITE cycle time	¹ PC	45		55		65		ns	
FAST-PAGE-MODE READ-WRITE cycle time	¹ PRWC	90		110		130		ns	
Access time from RAS	¹ RAC		80		100		120	ns	14
Access time from CAS	¹ CAC		20		25		30	ns	15
Output Enable	¹ OE		20		25		30	ns	23
Access time from column address	¹ AA		40		50		60	ns	
Access time from CAS precharge	¹ CPA		40		50		60	ns	
RAS pulse width	¹ RAS	80	10,000	100	10,000	120	10,000	ns	
RAS pulse width (FAST PAGE MODE)	¹ RASP	80	100,000	100	100,000	120	100,000	ns	
RAS hold time	¹ RSH	20		25		30		ns	
RAS precharge time	¹ RP	60		70		80		ns	
CAS pulse width	¹ CAS	20	10,000	25	10,000	30	10,000	ns	
CAS hold time	¹ CSH	80		100		120		ns	
CAS precharge time	¹ CPN	10		12		15		ns	16
CAS precharge time (FAST PAGE MODE)	¹ CP	10		12		15		ns	
RAS to CAS delay time	¹ RCD	20	60	25	75	25	90	ns	17
CAS to RAS precharge time	¹ CRP	5		5		10		ns	
Row address setup time	¹ ASR	0		0		0		ns	
Row address hold time	¹ RAH	10		15		15		ns	
RAS to column address delay time	¹ RAD	15	40	20	50	20	60	ns	18
Column address setup time	¹ ASC	0		0		0		ns	
Column address hold time	¹ CAH	15		20		20		ns	
Column address hold time (referenced to RAS)	¹ AR	60		70		80		ns	
Column address to RAS lead time	¹ RAL	40		50		60		ns	
Read command setup time	¹ RCS	0		0		0		ns	
Read command hold time (referenced to CAS)	¹ RCH	0		0		0		ns	19
Read command hold time (referenced to RAS)	¹ RRH	0		0		0		ns	19
CAS to output in Low-Z	¹ CLZ	0		0		0		ns	



ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

(Notes: 6, 7, 8, 9, 10, 11, 12, 13) ($-55^{\circ}\text{C} \leq T_C \leq 125^{\circ}\text{C}$, $V_{CC} = 5.0V \pm 10\%$)

AC CHARACTERISTICS		-8		-10		-12			
PARAMETER	SYM	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
Output buffer turn-off delay	t_{OFF}	0	20	0	20	0	25	ns	20,26
Output disable	t_{OD}		20		20		25	ns	26
WRITE command set-up time	t_{WCS}	0		0		0		ns	21
WRITE command hold time	t_{WCH}	15		20		25		ns	
WRITE command hold time (referenced to RAS\)	t_{WCR}	60		70		80		ns	
WRITE command pulse width	t_{WP}	15		15		20		ns	
WRITE command to RAS\ lead time	t_{RWL}	20		25		30		ns	
WRITE command to CAS\ lead time	t_{CWL}	20		25		30		ns	
Data-in set-up time	t_{DS}	0		0		0		ns	22
Data-in hold time	t_{DH}	15		20		25		ns	22
Data-in hold time referenced to RAS\	t_{DHR}	60		70		80		ns	
RAS\ to WRITE delay	t_{RWD}	105		125		150		ns	21
Column address to WE\ delay time	t_{AWD}	65		75		90		ns	21
CAS\ to WRITE delay	t_{CWD}	45		50		60		ns	21
Transition time (rise or fall)	t_T	3	50	3	50	3	50	ns	
Refresh period (512 cycles)	t_{REF}		8		8		8	ms	
RAS\ to CAS\ precharge time	t_{RPC}	0		0		0		ns	
CAS\ set-up time (CAS-BEFORE-RAS REFRESH)	t_{CSR}	10		10		10		ns	5
CAS\ hold time (CAS-BEFORE-RAS REFRESH)	t_{CHR}	15		20		25		ns	5
OE\ hold time from WE\ during READ-MODIFY-WRITE cycle	t_{OEH}	20		20		25		ns	25
OE\ setup prior to RAS\ during HIDDEN REFRESH cycle	t_{ORD}	0		0		0		ns	24
WE\ set-up time before RAS\ low	t_{WRP}	10		10		10		ns	9,10,11
WE\ hold time after RAS\ low CAS\ before RAS\ refresh	t_{WRH}	10		10		10		ns	9,10,11



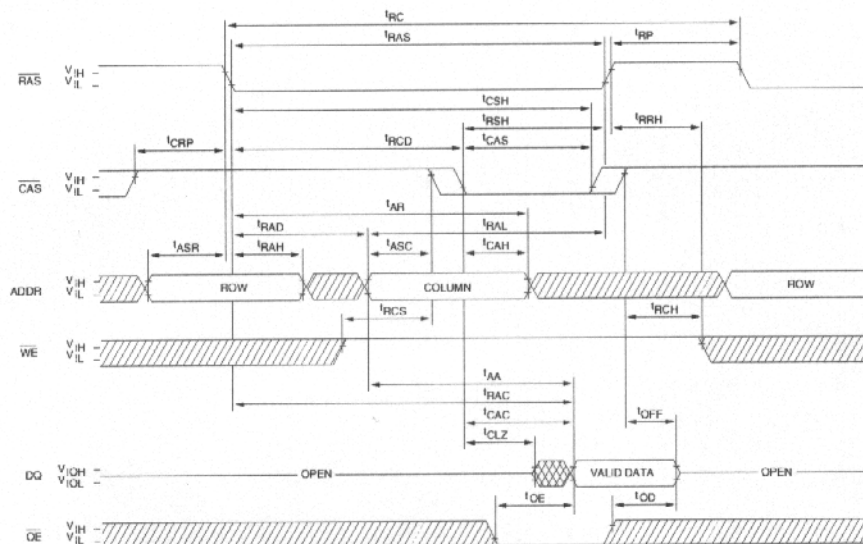


NOTES

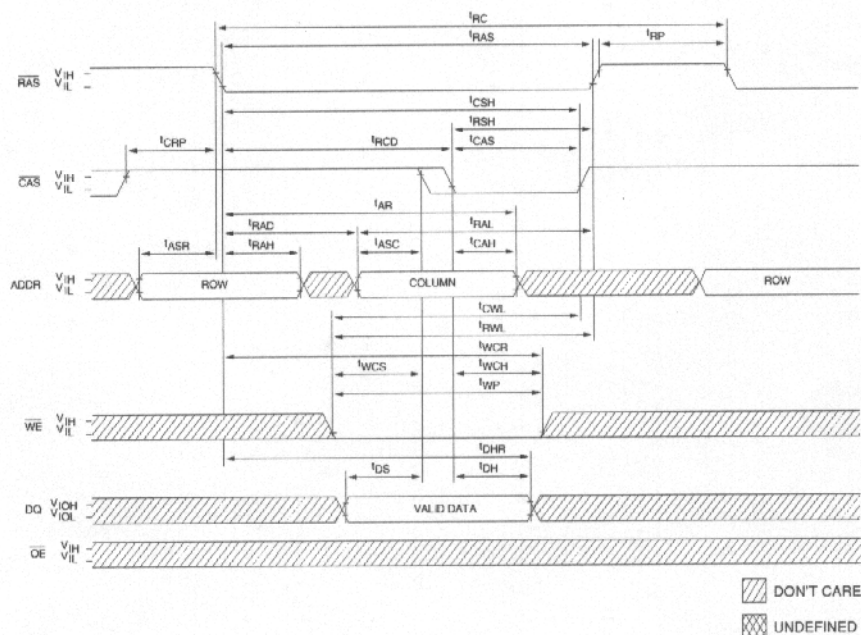
1. All voltages referenced to V_{SS}.
2. This parameter is sampled. V_{CC} = 5V ± 10%, f = 1 MHz.
3. I_{CC} is dependent on cycle rates.
4. I_{CC} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
5. Enables on-chip refresh and address counters.
6. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (-55°C ≤ T_C ≤ +125°C) is assured.
7. An initial pause of 100μs is required after power-up followed by any eight $\overline{\text{RAS}}$ only refresh cycles or CBR refresh cycle ($\overline{\text{WE}}$ held high) before proper device operation is assured.
8. AC characteristics assume t_T = 5ns. This parameter is not measured.
9. V_{IH} (MIN) and V_{IL} (MAX) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
10. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
11. If $\overline{\text{CAS}} = \text{V}_{IH}$, data outputs (DQs) are High-Z.
12. If $\overline{\text{CAS}} = \text{V}_{IL}$, data outputs (DQs) may contain data from the last valid READ cycle.
13. Measured with a load equivalent to 2 TTL gates and 100pF.
14. Assumes that t_{RCD} < t_{RCD} (MAX). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.
15. Assumes that t_{RCD} ≥ t_{RCD} (MAX).
16. If $\overline{\text{CAS}}$ is LOW at the falling edge of $\overline{\text{RAS}}$, DQs will be maintained from the previous cycle. To initiate a new cycle and clear the data out buffer, $\overline{\text{CAS}}$ must be pulsed HIGH for t_{CPN}.
17. Operation within the t_{RCD} (MAX) limit ensures that t_{RAC} (MAX) can be met. t_{RCD} (MAX) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (MAX) limit, then access time is controlled exclusively by t_{CAC}.
18. Operation within the t_{RAD} (MAX) limit ensures that t_{RAC} (MIN) and t_{CAC} (MIN) can be met. t_{RAD} (MAX) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (MAX) limit, then access time is controlled exclusively by t_{AA}.
19. Either t_{RCH} or t_{RRH} must be satisfied for a READ cycle.
20. t_{OFF} (MAX) defines the time at which the output achieves the open circuit condition, and is not referenced to V_{OH} or V_{OL}.
21. t_{WCS}, t_{RWD}, t_{AWD} and t_{CWD} are not restrictive operating parameters. t_{WCS} applies to EARLY-WRITE cycles. t_{RWD}, t_{AWD} and t_{CWD} apply to READ-MODIFY-WRITE cycles. If t_{WCS} ≥ t_{WCS} (MIN), the cycle is an EARLY-WRITE cycle and the data output will remain an open circuit throughout the entire cycle. If t_{RWD} ≥ t_{RWD} (MIN), t_{AWD} ≥ t_{AWD} (MIN) and t_{CWD} ≥ t_{CWD} (MIN), the cycle is a READ-MODIFY-WRITE and the data output will contain data read from the selected cell. If neither of the above conditions is met, the state of data out is indeterminate. $\overline{\text{OE}}$ held HIGH and $\overline{\text{WE}}$ taken LOW after $\overline{\text{CAS}}$ goes LOW results in a LATE-WRITE ($\overline{\text{OE}}$ controlled) cycle. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not applicable in a LATE-WRITE cycle.
22. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in EARLY-WRITE cycles and $\overline{\text{WE}}$ leading edge in LATE-WRITE or READ-MODIFY-WRITE cycles.
23. If $\overline{\text{OE}}$ is tied permanently LOW, LATE-WRITE or READ-MODIFY-WRITE operations are not possible.
24. A HIDDEN REFRESH may also be performed after a WRITE cycle. In this case, $\overline{\text{WE}} = \text{LOW}$ and $\overline{\text{OE}} = \text{HIGH}$.
25. LATE-WRITE and READ-MODIFY-WRITE cycles must have both t_{OD} and t_{OE} met ($\overline{\text{OE}}$ HIGH during WRITE cycle) in order to ensure that the output buffers will be open during the WRITE cycle. The DQs will provide the previously read data if $\overline{\text{CAS}}$ remains LOW and $\overline{\text{OE}}$ is taken back LOW after t_{OE} is met. If $\overline{\text{CAS}}$ goes HIGH prior to $\overline{\text{OE}}$ going back LOW, the DQs will remain open.
26. The DQs open during READ cycles once t_{OD} or t_{OFF} occur. If $\overline{\text{CAS}}$ goes HIGH first, $\overline{\text{OE}}$ becomes a "don't care." If $\overline{\text{OE}}$ goes HIGH and $\overline{\text{CAS}}$ stays LOW, $\overline{\text{OE}}$ is not a "don't care;" and the DQs will provide the previously read data if $\overline{\text{OE}}$ is taken back LOW (while $\overline{\text{CAS}}$ remains LOW).



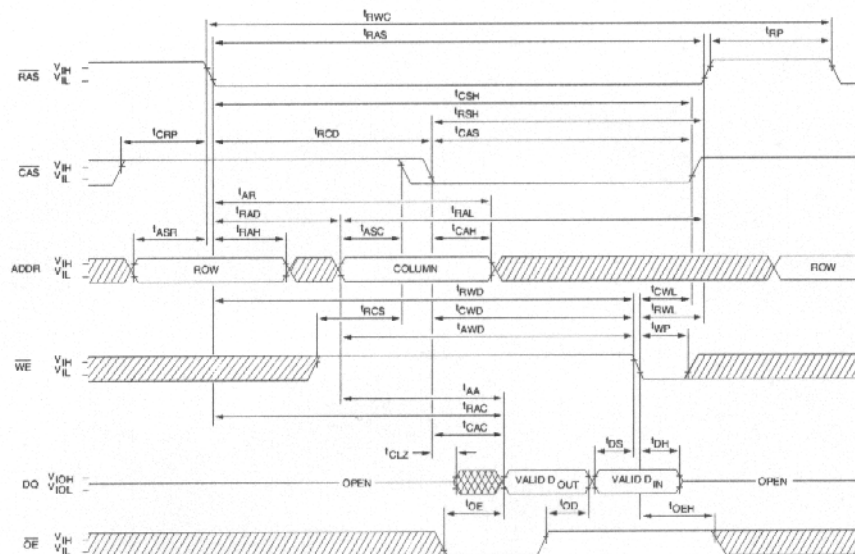
READ CYCLE



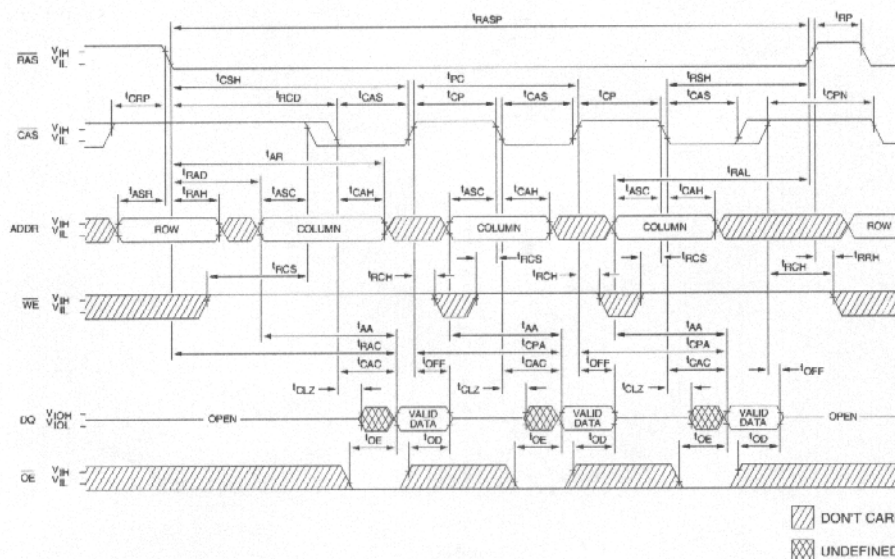
EARLY-WRITE CYCLE



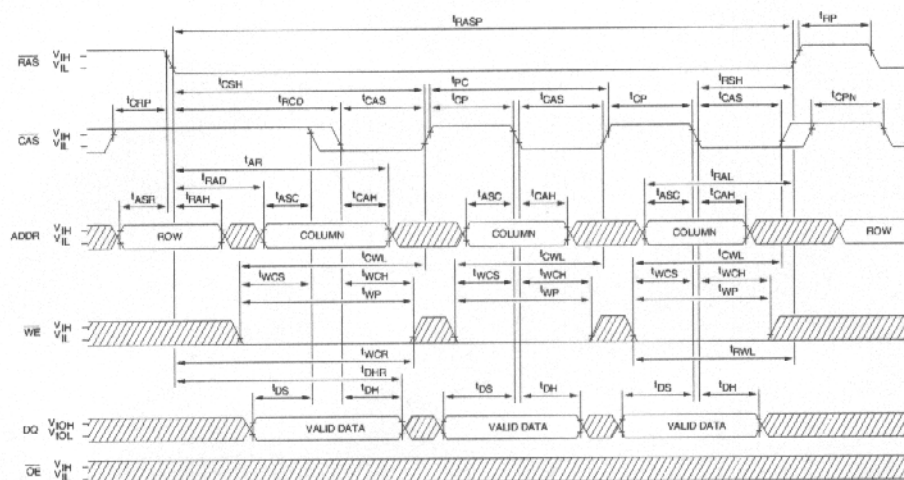
READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



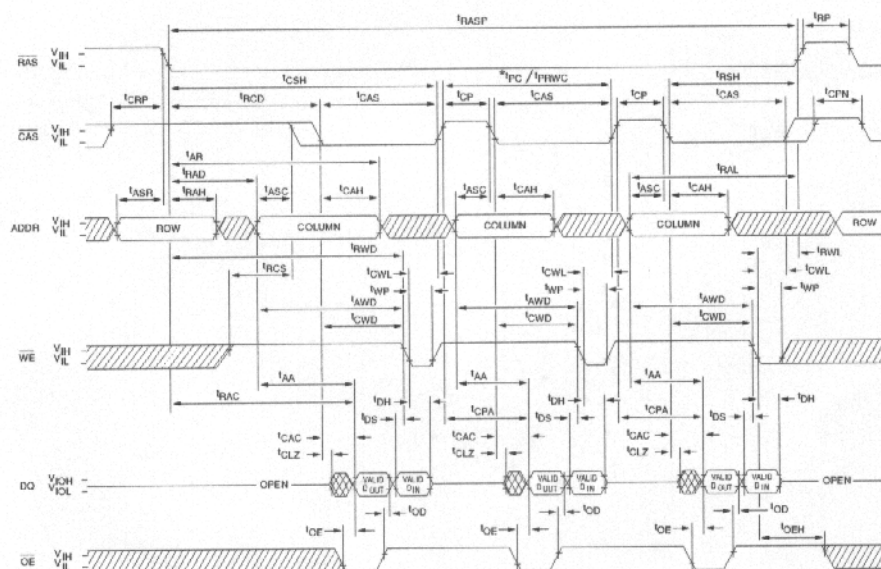
FAST-PAGE-MODE READ CYCLE



FAST-PAGE-MODE EARLY-WRITE CYCLE



FAST-PAGE-MODE READ-WRITE CYCLE
(LATE-WRITE and READ-MODIFY-WRITE CYCLES)



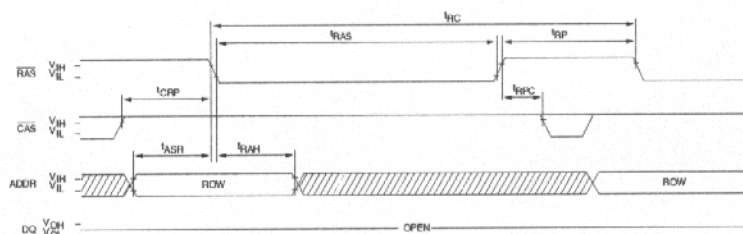
*t_{PC} = LATE-WRITE cycle

¹PRWC = FAST READ-MODIFY-WRITE cycle

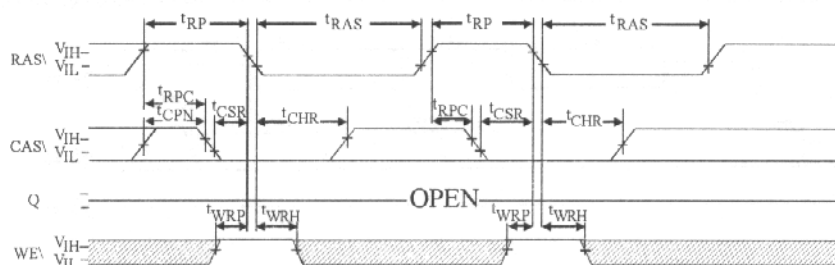
 DON'T CARE

 UNDEFINED

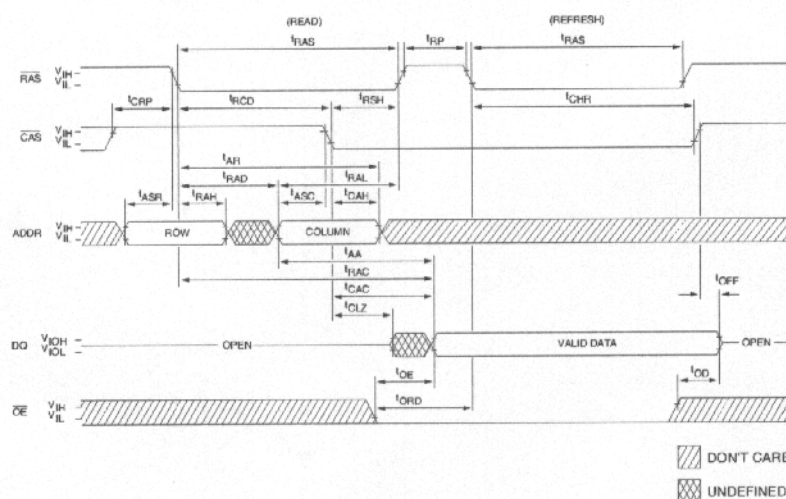
RAS-ONLY REFRESH CYCLE
(ADDR = A0-A8; $\overline{\text{WE}}$ = DON'T CARE)



CAS-BEFORE-RAS REFRESH CYCLE
(A0-A8, $\overline{WE}$ and $\overline{OE}$ = DON'T CARE)



HIDDEN REFRESH CYCLE ²⁴
($\overline{\text{WE}}$ = HIGH, $\overline{\text{OE}}$ = LOW)



**ELECTRICAL TEST REQUIREMENTS**

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (per Method 5005, Table I)
INTERIM ELECTRICAL (PRE-BURN-IN) TEST PARAMETERS (Method 5004)	2, 8A, 10
FINAL ELECTRICAL TEST PARAMETERS (Method 5004)	1*, 2, 3, 7*, 8, 9, 10, 11
GROUP A TEST REQUIREMENTS (Method 5005)	1, 2, 3, 4**, 7, 8, 9, 10, 11
GROUP C AND D END-POINT ELECTRICAL PARAMETERS (Method 5005)	1, 2, 3, 7, 8, 9, 10, 11

* PDA applies to subgroups 1 and 7.

** Subgroup 4 shall be measured only for initial qualification and after process or design changes, which may affect input or output capacitance.