ANALOG DEVICES

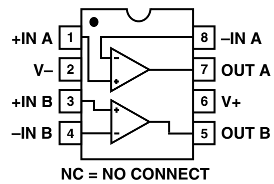
Dual Low Power Operational Amplifier, Single or Dual Supply

OP221

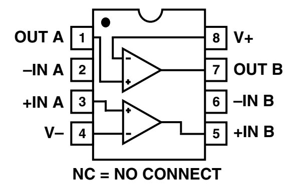
FEATURES
- Excellent TCVos Match, 2 µV/°C Max
- Low Input Offset Voltage, 150 µV Max
- Low Supply Current, 550 µA Max
- Single Supply Operation, 5 V to 30 V
- Low Input Offset Voltage Drift, 0.75 µV/°C
- High Open-Loop Gain, 1500 V/mV Min
- High PSRR, 3 µV/V
- Wide Common-Mode Voltage Range, V– to within 1.5 V of V+
- Pin Compatible with 1458, LM158, LM2904
- Available in Die Form

PIN CONNECTIONS

8-Lead SO (S-Suffix)



8-Lead HERMETIC DIP (Z-Suffix)



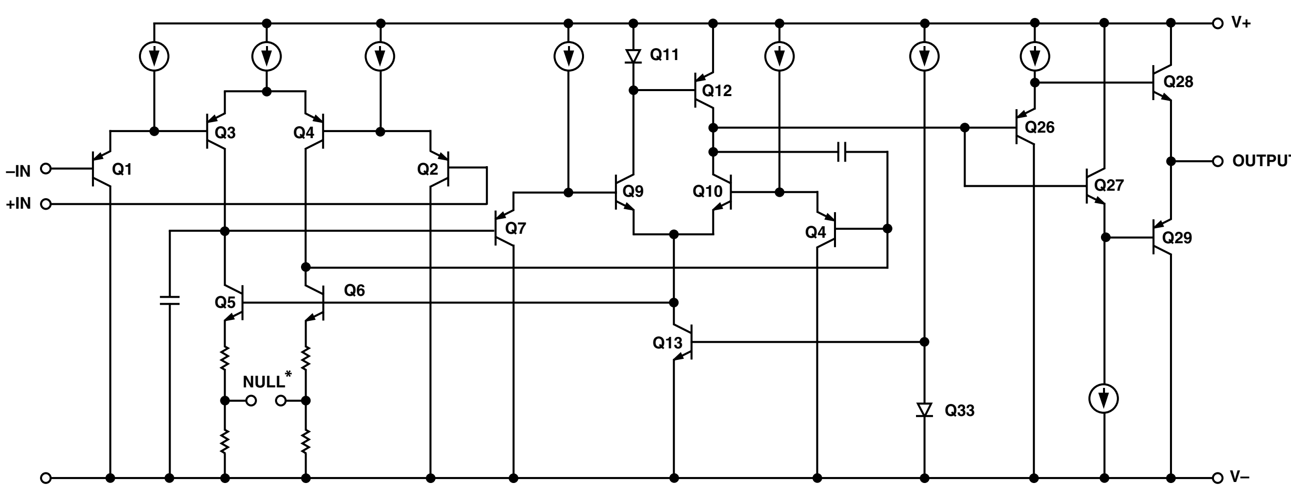
GENERAL DESCRIPTION

The OP221 is a monolithic dual operational amplifier that can be used either in single or dual supply operation. The wide supply voltage range, wide input voltage range, and low supply current drain of the OP221 make it well-suited for operation from batteries or unregulated power supplies.

The excellent specifications of the individual amplifiers combined with the tight matching and temperature tracking between channels provide high performance in instrumentation amplifier designs. The individual amplifiers feature very low input offset voltage, low offset voltage drift, low noise voltage, and low bias current. They are fully compensated and protected.

Matching between channels is provided on all critical parameters including input offset voltage, tracking of offset voltage vs. temperature, non-inverting bias currents, and common-mode rejection.

SIMPLIFIED SCHEMATIC



*ACCESSIBLE IN CHIP FORM ONLY

REV. A

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OP221–SPECIFICATIONS (Electrical Characteristics at V_S = ±2.5 V to ±15 V, T_A = 25°C, unless otherwise noted.)

			OP221A/E			OP221G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage	V_{OS}			75	150		250	500	µV
Input Offset Current	Ios	V_{CM} = 0		0.5	3		1.5	7	nA
Input Bias Current	I_B	V_{CM} = 0		55	100		70	120	nA
Input Voltage Range	IVR	V+ = 5 V, V– = 0 V (Note 2) V_S = ±15 V	0/3.5 –15/13.5			0/3.5 –15/13.5			V
Common-Mode Rejection Ratio	CMRR	V+ = –5 V, V– = 0 V 0 V ≤ V_{CM} ≤ 3.5 V V_S = ±15 V –15 V ≤ V_{CM} ≤ 13.5 V	 90 95	 100 100		 75 80	 85 90		dB
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ± 15 V V– = 0 V, V+ = 5 V to 30 V		3 6	10 18		32 57	100 180	µV/V
Large-Signal Voltage Gain	Avo	V_S = ±15 V, R_L = 10 kΩ V_O = ±10 V	1500			800			V/mV
Output Voltage Swing	V_O	V+ = 5 V, V– = 0 V R_L = 10 kΩ V_S = 15 V, R_L = 10 kΩ	0.7/4.1 ±13.8			0.8/4 ±13.5			V
Slew Rate	SR	R_L = 10 kΩ (Note 1)	0.2	0 3		0.2	0.3		V/µS
Bandwidth	BW			600			600		kHz
Supply Current (Both Amplifiers)	I_{SY}	V_S = ±2.5 V, No Load V_S = ±15 V, No Load		450 600	550 800		550 850	650 900	µA

NOTES
[1]Sample tested.
[2]Guaranteed by CMRR test limits.

SPECIFICATIONS

(Electrical Characteristics at V_S = ±2.5 V to ±15 V, –55°C ≤ T_A +125°C for OP221A, –25°C ≤ T_A ≤ +85°C for OP221E, –40°C ≤ T_A ≤ +85°C for OP221G, unless otherwise noted.)

			OP221A/E			OP221G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Average Input Offset Voltage	TCV_{OS}			0.75	1.5		2	3	µV/°C
Input Offset Voltage	V_{OS}			150	300		400	700	µV
Input Offset Current	I_{OS}	V_{CM} = 0		1	5		2	10	nA
Input Bias Current	I_B	V_{CM} = 0		55	100		80	140	nA
Input Voltage Range	IVR	V+ = 5 V, V– = 0 V (Note 2) V_S = ±15 V	0/3.2 –15/13.2			0/3.2 –15/13.2			V
Common-Mode Rejection Ratio	CMRR	V+ = –5 V, V– = 0 V 0 V ≤ V_{CM} ≤ 3.5 V V_S = ±15 V –15 V ≤ V_{CM} ≤ 13.5 V	 85 90	 90 95		 70 75	 80 85		dB
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ± 15 V V– = 0 V, V+ = 5 V to 30 V		6 10	18 32		57 100	180 320	µV/V
Large-Signal Voltage Gain	A_{VO}	V_S = ±15 V, R_L = 10 kΩ V_O = ±10 V	 1000			 600			V/mV
Output Voltage Swing	V_O	V+ = 5 V, V– = 0 V R_L = 10 kΩ V_S = 15 V, R_L = 10 kΩ	0.8/3.8 ±13.5			0.9/3.7 13.2			V
Supply Current (Both Amplifiers)	I_{SY}	V_S = ±2.5 V, No Load V_S = ±15 V, No Load		500 700	650 900		600 950	750 1000	µA

NOTES
[1]Sample tested.
[2]Guaranteed by CMRR test limits.

Matching Characteristics at V_S = ±15 V, T_A = 25°C, unless otherwise noted.

			OP221A/E			OP221G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage Match	ΔV_{OS}			50	200		250	600	µV
Average Noninverting Bias Current	I_B+				80			120	nA
Noninverting Input Offset Current	I_{OS}+			2	5		4	10	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	V_{CM} = –15 V to 13.5 V	92			72			dB
Power Supply Rejection Ratio Match (Note 1)	ΔPSRR	V_S = ±2.5 V to ± 15 V			14			140	µV/V

OP221–SPECIFICATIONS (Matching Characteristics at V_S = ±15 V, –55°C ≤ T_A ≤ +125°C for OP221A, –25°C ≤ T_A ≤ +85°C for OP221E, –40°C ≤ T_A ≤ +85°C for OP221G, unless otherwise noted. Grades E and G are sample tested.)

			OP221A/E			OP221G			
Parameter	**Symbol**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
Input Offset Voltage Match	ΔV_{OS}			100	400		400	800	μV
Average Noninverting Bias Current	I_B+	V_{CM} = 0			100			140	nA
Input Offset Voltage Tracking	$IC\Delta V_{OS}$			1	2		3	5	μV°C
Noninverting Input Offset Current	I_{OS}+	V_{CM} = 0		3	7		6	12	nA
Common-Mode Rejection Ratio Match (Note 1)	ΔCMRR	V_{CM} = –15 V to 13.2 V	87	90		72	80		dB
Power Supply Rejection Ratio Match (Note 1)	ΔPSRR				26		140	μV/V	

NOTES
[1]ΔCMRR is 20 $\log_{10}$ V_{CM}/ΔCME, where V_{CM} is the voltage applied to both noninverting inputs and ΔCME is the difference in common-mode input-referred error.
[2]ΔPSRR is: $\dfrac{\text{Input-Referred Differential Error}}{\Delta V_S}$

Wafer Test Limits at V_S = ±2.5 V to ±15 V, T_A = 25°C, unless otherwise noted.

Parameter	**Symbol**	**Conditions**	**OP221N Limit**	**Unit**
Input Offset Voltage	V_{OS}		200	μV Max
Input Offset Current	I_{OS}	V_{CM} = 0	3.5	nA Max
Input Bias Current	I_B	V_{CM} = 0	85	nA Max
Input Voltage Range	IVR	V+ = 5 V, V– = 0 V V_S= ±15 V	0/3.5 –15/13.5	V Min/Max V Min
Common-Mode Rejection Ratio	CMRR	V– = 0 V, V+ = 5 V, 0 V ≤ V_{CM} ≤ 3.5 V V_S = ±15 V –15 V ≤ V_{CM} ≤ 13.5 V	88 93	dB Min
Power Supply Rejection Ratio	PSRR	V_S = ±2.5 V to ± 15 V V– = 0 V, V+ = 5 V to 30 V	12.5 22.5	V/mV Min
Large-Signal Voltage Gain	Avo	V_S = ±15 V R_L = 10 kΩ	1500	V/mV Max
Output Voltage Swing	V_O	V+ = 5 V, V– = 0 V, R_L= 10 kΩ V_S = 15 V, R_L = 10 kΩ	0.7/4.1 ±13.8	V Min/Max V Min
Supply Current (Both Amplifiers)	I_{SY}	V_S = ±2.5 V, No Load V_S = ±15 V, No Load	560 810	μA Max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage . . . . ±18 V
Differential Input Voltage . . . . 30 V or Supply Voltage
Input Voltage . . . . Supply Voltage
Output Short-Circuit Duration . . . . Indefinite
Storage Temperature Range . . . . –65°C to +150°C
Operating Temperature Range
OP221A . . . . –55°C to +125°C
OP221E . . . . –25°C to +85°C
OP221G . . . . –40°C to +85°C
Lead Temperature (Soldering 60 sec) . . . . 300°C
Junction Temperature (T_J) . . . . –65°C to +150°C

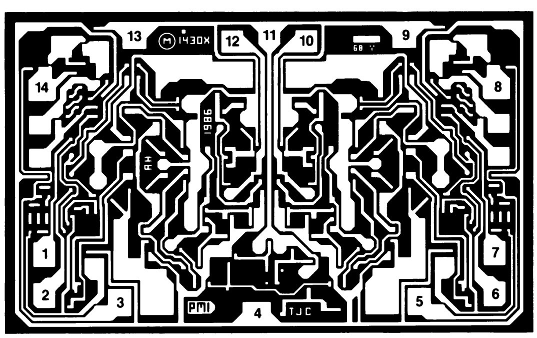
Package Type	θ_{JA} (Note 2)	θ_{JC}	Unit
8-Lead Hermetic DIP (Z)	148	16	°C/W
8-Lead Plastic DIP (P)	103	43	°C/W
8-Lead SO (S)	158	43	°C/W

NOTES
[1]Absolute maximum ratings apply to both DICE and packaged parts, unless otherwise noted.
[2]θ_{JA} is specified for worst case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, Cerdip, and PDIP packages; eIA is specified for device soldered to printed circuit board for SO package.

ORDERING INFORMATION[1,2]

T_A = +25°C V_{OS} MAX (µV)	Packages Cerdip 8-Lead	Plastic 8-Lead	Operating Temperature Range	Package Options
150	OP221AZ[3]		MIL	Q-8
150	OP221 EZ[3]		IND	
300				
500				
500		OP221GP[3]	XIND	R-8
500		OP221GS	XIND	

[1]Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.
[2]For devices processed in total compliance to MIL-STD-883, add/883 after part number. Consult factory for 883 data sheet.
[3]Not for new design, obsolete April 2002.



1. INVERTING INPUT (A)
2. NONINVERTING INPUT (A)
3. BALANCE (A)
4. V–
5. BALANCE (B)
6. INVERTING INPUT (B)
7. NONINVERTING INPUT (B)
8. BALANCE (B)
9. V+
10. OUT (B)
11. V+
12. OUT (A)
13. V+
14. BALANCE (A)

DIE SIZE 0.097 X 0.063 INCH, 6111 SQ. MILS
(2.464 X 1.600 MM, 3.94 SQ. MM)

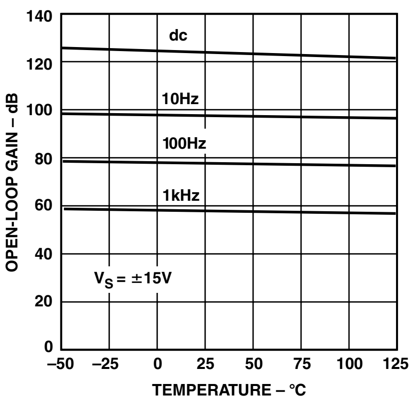
NOTE: ALL V+ PADS ARE INTERNALLY CONNECTED.

Figure 1. Dice Characteristics

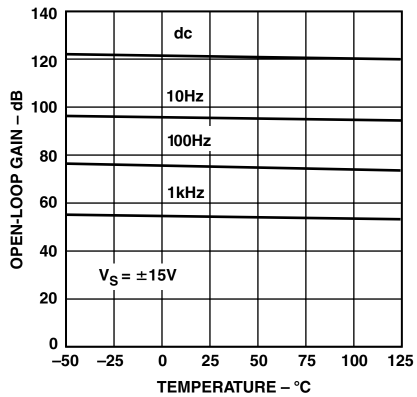
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP221 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

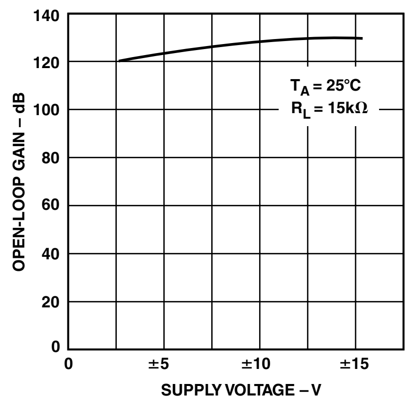
Typical Perfomance Characteristics – OP221



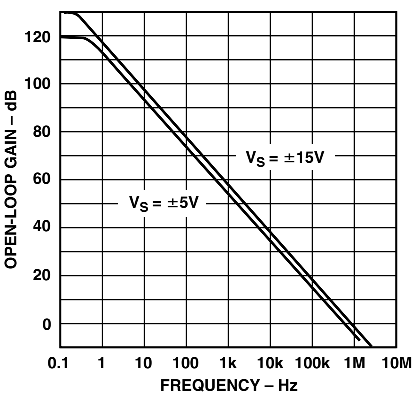
TPC 1. Open-Loop Gain at ±15 V vs. Temperature



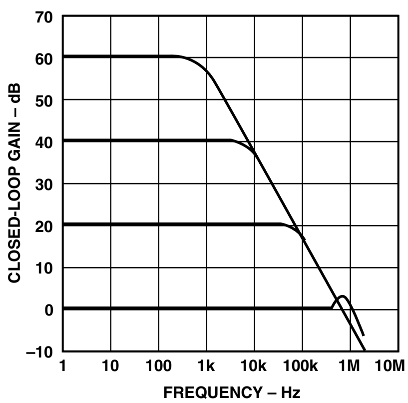
TPC 2. Open-Loop Gain at ± 5 V vs. Temperature



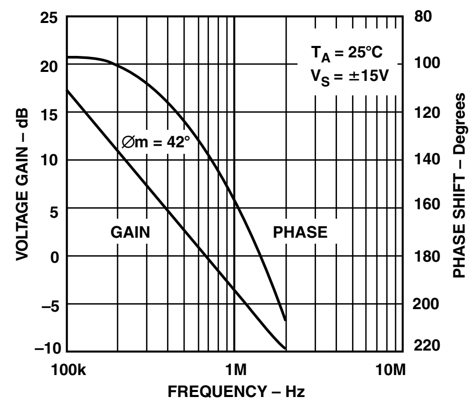
TPC 3. Open-Loop Gain at vs. Supply Voltage



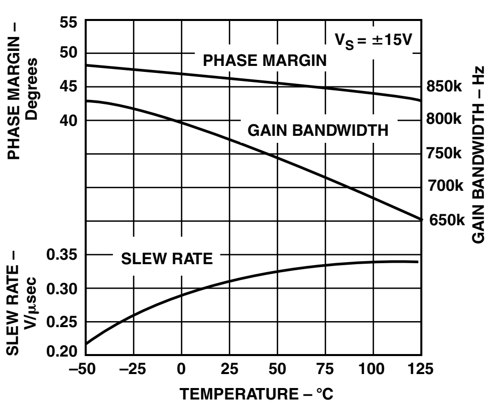
TPC 4. Open-Loop Gain at ±15 V vs. Frequency



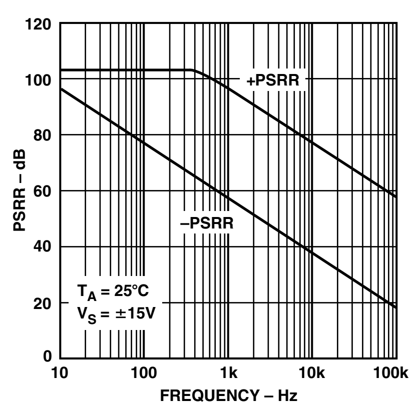
TPC 5. Closed-Loop Gain vs. Frequency



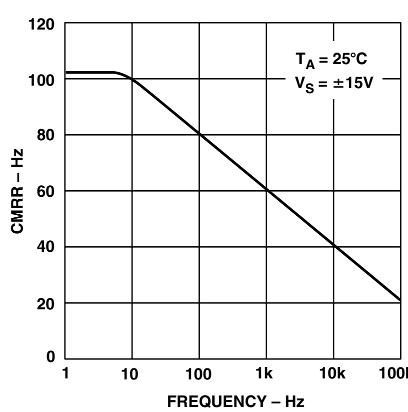
TPC 6. Gain and Phase Shift vs. Frequency



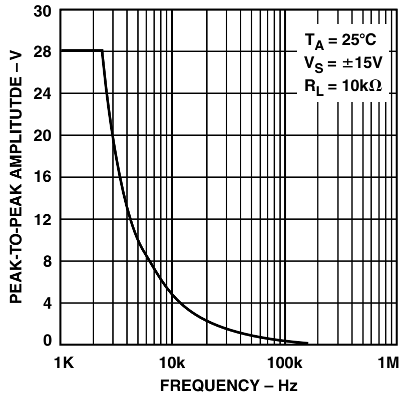
TPC 7. Phase Margin, Gain Bandwidth, and Slew Rate vs. Temperature



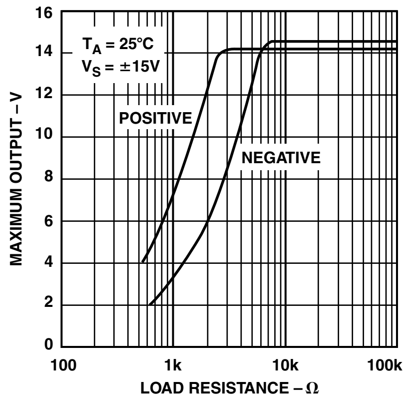
TPC 8. PSRR vs. Frequency



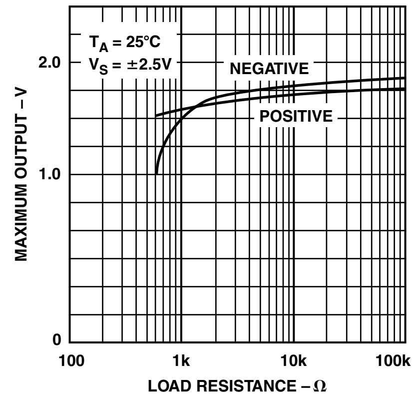
TPC 9. CMRR vs. Frequency



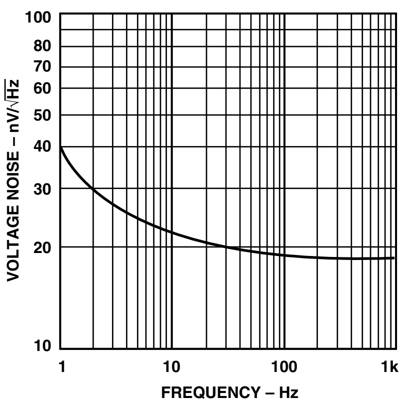
TPC 10. *Maximum Output Swing vs. Frequency*



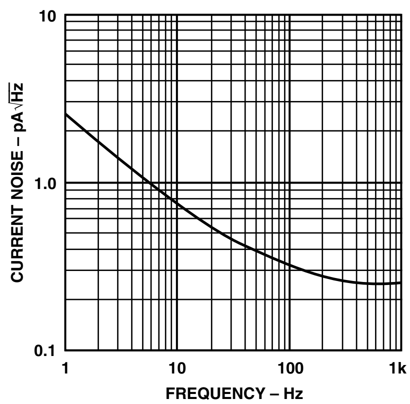
TPC 11. *Maximum Output Voltage vs. Load Resistance*



TPC 12. *Maximum Output Voltage vs. Load Resistance*



TPC 13. *Voltage Noise Density vs. Frequency*



TPC 13. *Current Noise Density vs. Frequency*

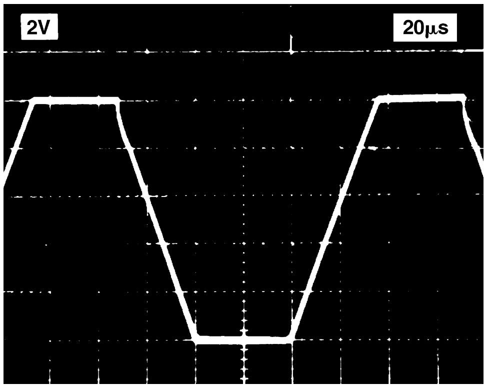


Figure 2a. Noninverting Step Response

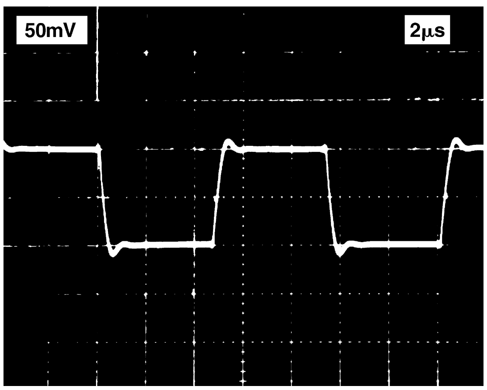


Figure 2b. Noninverting Step Response

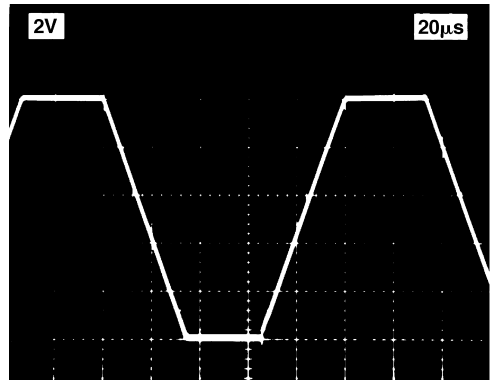


Figure 3a. Inverting Step Response

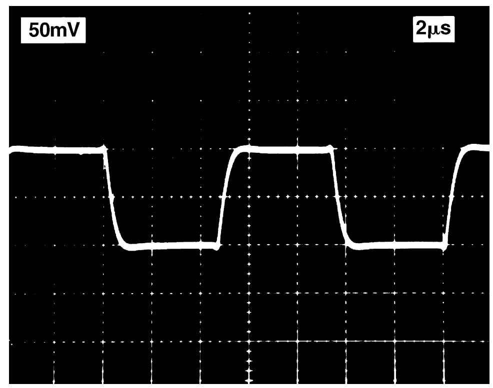


Figure 3b. Inverting Step Response

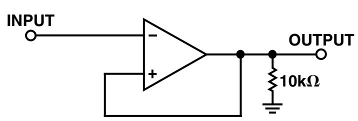


Figure 4. TBD.

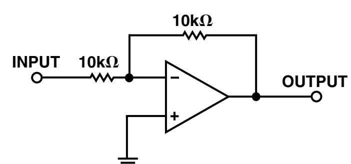


Figure 5. TBD.

SPECIAL NOTES ON THE APPLICATION OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Advantages of Dual Monolithic Operational Amplifiers

Dual matched operational amplifiers provide the engineer with a powerful tool for designing instrumentation amplifiers and many other differential-input circuits. These designs are based on the principle that careful matching between two operational amplifiers can minimize the effect of dc errors in the individual amplifiers.

Reference to the circuit shown in Figure 6, a differential-in, differential-out amplifier, shows how the reductions in error can be accomplished. Assuming the resistors used are ideally matched, the gain of each side will be identical. If the offset voltages of each amplifier are perfectly matched, then the net differential voltage at the amplifier's output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the difference (degree of matching) between the amplifiers' offset voltages. This error-cancellation principle holds for a considerable number of input referred error parameters—offset voltage, offset voltage drift, inverting and noninverting bias currents, common mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are high and tightly matched, an important feature not practical with single operation amplifier circuits.

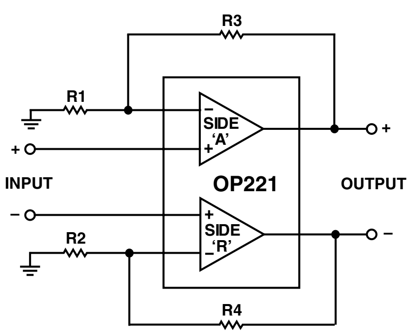


Figure 6. Differential-In, Differential-Out Amplifier

INSTRUMENTATION AMPLIFIER APPLICATIONS

Two-Op Amp Configuration

The two-op amp circuit (Figure 7) is recommended where the common-mode input voltage range is relatively limited; the common-mode and differential voltage both appear at V1. The high open-loop gain of the OP221 is very important in achieving good CMRR in this configuration. Finite open-loop gain of A1 (Ao1) causes undesired feedthrough of the common-mode input. For Ad/Ao, << 1, the common-mode error (CME) at the output due to this effect is approximately (2 Ad/Ao1) x VCM. This circuit features independent adjustment of CMRR and differential gain.

Three-Op Amp Configuration

The three-op amp circuit (Figure 8) has increased common-mode voltage range because the common-mode voltage is not amplified as it is in Figure 7. The CMR of this amplifier is directly proportional to the match of the CMR of the input op amps. CMRR can be raised even further by trimming the output stage resistors.

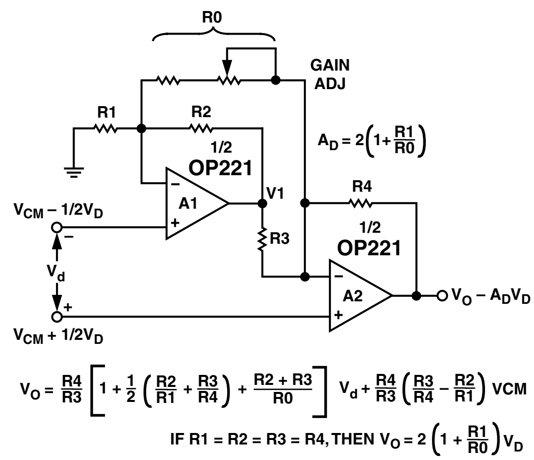


Figure 7. Two-Op Amp Circuit

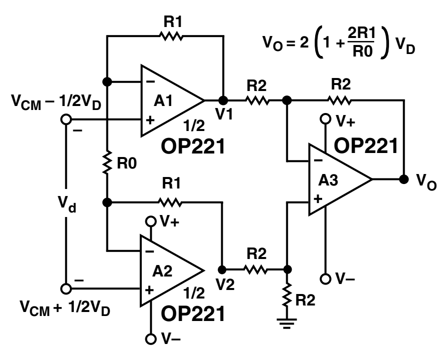


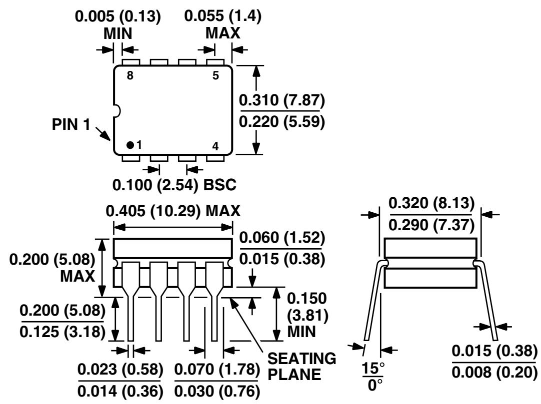
Figure 8. Three-Op Amp Circuit

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

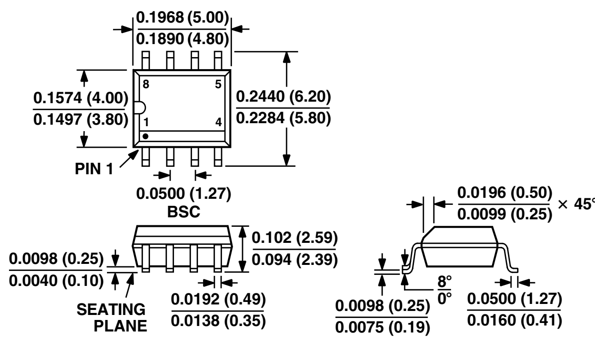
8-Lead CERDIP Package

(Q-8)



8-Lead SOIC Package

(R-8)



Revision History

C00324–0–1/02(A)

PRINTED IN U.S.A.