

FEATURES

Low offset voltage

B grade: 0.4 mV maximum

A grade: 1 mV maximum

Low offset voltage drift

B grade: 4 $\mu\text{V}/^\circ\text{C}$ maximum

A grade: 8 $\mu\text{V}/^\circ\text{C}$ maximum

Low input bias current: 5 pA typical at $V_{\text{SY}} = \pm 15\text{ V}$

Dual-supply operation: $\pm 4.5\text{ V}$ to $\pm 15\text{ V}$

Low noise

7.3 nV/ $\sqrt{\text{Hz}}$ typical at $f = 1\text{ kHz}$

0.45 $\mu\text{V p-p}$ at 0.1 Hz to 10 Hz

Low distortion: 0.00006%

No phase reversal

Rail-to-rail output

Unity gain stable

APPLICATIONS

Instrumentation

Medical instruments

Multipole filters

Precision current measurement

Photodiode amplifiers

Sensors

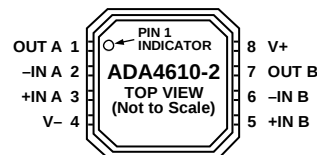
Audio

GENERAL DESCRIPTION

The [ADA4610-2](#) is a dual channel, precision JFET amplifier that features low input voltage and current noise, offset voltage, input bias current, and rail-to-rail output.

The combination of low offset, noise, and very low input bias current makes these amplifiers especially suitable for high impedance sensor amplification and precise current measurements using shunts. With excellent dc precision, low noise, and fast settling time, the [ADA4610-2](#) provides superior accuracy in medical instruments, electronic measurement, and automated test equipment. Unlike many competitive amplifiers, the [ADA4610-2](#) maintains fast settling performance with substantial capacitive loads. Unlike many older JFET amplifiers, the [ADA4610-2](#) does not suffer from output phase reversal when input voltages exceed the maximum common-mode voltage range.

PIN CONFIGURATIONS



NOTES

1. THE EXPOSED PAD MUST BE CONNECTED TO V_{-} .

Figure 1. 8-Lead LFCSP (CP Suffix)

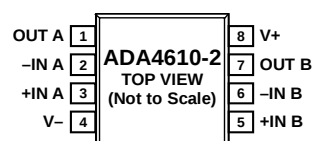


Figure 2. 8-Lead SOIC_N (R Suffix) and 8-Lead MSOP (RM Suffix)

The fast slew rate and great stability with capacitive loads make the [ADA4610-2a](#) perfect fit for high performance filters. Low input bias currents, low offset, and low noise result in a wide dynamic range for photodiode amplifier circuits. Low noise and distortion, high output current, and excellent speed make the [ADA4610-2](#) a great choice for audio applications.

The [ADA4610-2](#) is specified over the -40°C to $+125^\circ\text{C}$ extended industrial temperature range.

The [ADA4610-2](#) is available in the 8-lead narrow SOIC, 8-lead MSOP, and 8-lead LFCSP packages.

Rev. A

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REVISION HISTORY

5/12—Rev. 0 to Rev. A

Changes to Data Sheet Title and General Description Section..	1
Changed Input Impedance, Differential to Input Capacitance, Differential in Table 1.....	3
Added Input Resistance in Table 1	3
Changed Input Impedance, Differential to Input Capacitance, Differential in Table 2.....	4
Added Input Resistance in Table 2	4
Added Figure 9, Figure 10, and Figure 14	8
Added Figure 15.....	9
Updated Outline Dimensions	16
Changes to Ordering Guide	17

12/11—Revision 0: Initial Version

SPECIFICATIONS

$V_{SY} = \pm 5\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade) ¹	V_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	0.4	mV
Offset Voltage (A Grade) ¹	V_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.4	0.8	mV
Offset Voltage Drift (B Grade) ²	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	1.8	$\mu\text{V}/^\circ\text{C}$
Offset Voltage Drift (A Grade) ²	$\Delta V_{OS}/\Delta T$			1	8	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B			5	25	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$			1.5	nA
		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	20	pA
Input Voltage Range			-2.5		0.25	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -2.5\text{ V to }+2.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	94	110	+2.5	V
			86			dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_{OUT} = -3.5\text{ V to }+3.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	98	100		dB
			86			dB
Input Capacitance, Differential		$V_{CM} = 0\text{ V}$		3.1		pF
Input Capacitance, Common-Mode		$V_{CM} = 0\text{ V}$		4.8		pF
Input Resistance		$V_{CM} = 0\text{ V}$		$>1 \times 10^{13}$		Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2\text{ k}\Omega$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.85	4.90		V
			4.6			V
		$R_L = 600\text{ }\Omega$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	4.6	4.89		V
			4.05			V
Output Voltage Low	V_{OL}	$R_L = 2\text{ k}\Omega$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		-4.95	-4.9	V
					-4.75	V
		$R_L = 600\text{ }\Omega$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		-4.9	-4.8	V
					-4.4	V
Short-Circuit Current	I_{SC}			± 63		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 4.5\text{ V to } \pm 18\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	106	125		dB
			103			dB
Supply Current/Amplifier	I_S	$I_{OUT} = 0\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1.5	1.7	mA
					1.85	mA
DYNAMIC PERFORMANCE						
Gain Bandwidth Product	GBP	$V_{IN} = 5\text{ mV p-p}$, $R_L = 2\text{ k}\Omega$, $A_V = 100$		15.4		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 5\text{ mV p-p}$, $R_L = 2\text{ k}\Omega$, $A_V = -10$		9.3		MHz
Phase Margin	ϕ_M			61		Degrees
-3 dB Closed-Loop Bandwidth	-3 dB	$A_V = 1$, $V_{IN} = 5\text{ mV p-p}$		10.6		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_n\text{ p-p}$	0.1 Hz to 10 Hz		0.45		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 10\text{ Hz}$		14		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100\text{ Hz}$		8.2		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1\text{ kHz}$		7.3		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10\text{ kHz}$		7.3		$\text{nV}/\sqrt{\text{Hz}}$

¹ Offset voltage does not include solder heat resistance.

² Guaranteed by design and characterization.

ELECTRICAL CHARACTERISTICS

$V_{SY} = \pm 15\text{ V}$, $V_{CM} = 0\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage (B Grade) ¹	V_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.2	0.4	mV
Offset Voltage (A Grade) ¹	V_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.4	0.8	mV
Offset Voltage Drift (B Grade) ²	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		0.5	1	$\mu\text{V}/^\circ\text{C}$
Offset Voltage Drift (A Grade) ²	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		1	1.8	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	I_B	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		5	25	pA
Input Offset Current	I_{OS}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		2	1.5	nA
Input Voltage Range		$-40^\circ\text{C} < T_A < +125^\circ\text{C}$	-12.5		0.25	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -12.5\text{ V to } +12.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	100	115	+12.5	dB
Large Signal Voltage Gain	A_{VO}	$R_L = 2\text{ k}\Omega$, $V_{OUT} = \pm 13.5\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	96	107		dB
Input Capacitance, Differential		$V_{CM} = 0\text{ V}$		3.1		pF
Input Capacitance, Common-Mode		$V_{CM} = 0\text{ V}$		4.8		pF
Input Resistance		$V_{CM} = 0\text{ V}$		$> 1 \times 10^{13}$		Ω
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 2\text{ k}\Omega$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	14.8	14.9		V
		$R_L = 600\text{ }\Omega$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	14.65	14.47		V
Output Voltage Low	V_{OL}	$R_L = 2\text{ k}\Omega$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	14.25	-14.9	-14.85	V
		$R_L = 600\text{ }\Omega$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	13.35	-14.68	-14.75	V
Short-Circuit Current	I_{SC}	$-40^\circ\text{C} < T_A < +125^\circ\text{C}$		± 79	-14.6	V
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_{SY} = \pm 4.5\text{ V to } \pm 18\text{ V}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	106	125		dB
Supply Current/Amplifier	I_{SY}	$I_{OUT} = 0\text{ mA}$ $-40^\circ\text{C} < T_A < +125^\circ\text{C}$	103	1.6	1.85	mA
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 2\text{ k}\Omega$	$\pm 17^2$	+25/-61		V/ μs
Gain Bandwidth Product	GBP	$V_{IN} = 5\text{ mV p-p}$, $R_L = 2\text{ k}\Omega$, $A_V = 100$		16.3		MHz
Unity-Gain Crossover	UGC	$V_{IN} = 5\text{ mV p-p}$, $R_L = 2\text{ k}\Omega$, $A_V = -10$		9.3		MHz
Phase Margin	ϕ_M			66		Degrees
-3 dB Closed-Loop Bandwidth	-3 dB	$A_V = 1$, $V_{IN} = 5\text{ mV p-p}$		9.50		MHz
Total Harmonic Distortion (THD) + Noise	THD + N	1 kHz, $G = +1$, $R_L = 2\text{ k}\Omega$, $V_{IN} = 6\text{ V rms}$		0.00006		%

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
NOISE PERFORMANCE						
Peak-to-Peak Voltage Noise	e_n p-p	0.1 Hz to 10 Hz bandwidth		0.45		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 10 \text{ Hz}$		14		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 100 \text{ Hz}$		8.5		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 1 \text{ kHz}$		7.3		$\text{nV}/\sqrt{\text{Hz}}$
		$f = 10 \text{ kHz}$		7.3		$\text{nV}/\sqrt{\text{Hz}}$

¹ Offset voltage does not include solder heat resistance.

² Guaranteed by design and characterization.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	$\pm 18\text{ V}$
Input Voltage	$\pm V_S$
Output Short-Circuit Duration to GND	Observe derating curves
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	-40°C to $+125^{\circ}\text{C}$
Junction Temperature Range	-65°C to $+150^{\circ}\text{C}$
Lead Temperature (Soldering, 10 sec)	300°C
Electrostatic Discharge (Human Body Model)	2500 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4. Thermal Resistance

Package Type	θ_{JA}^1	θ_{JC}	Unit
8-Lead MSOP (RM-8)	142	45	$^{\circ}\text{C}/\text{W}$
8-Lead SOIC_N (R-8)	120	43	$^{\circ}\text{C}/\text{W}$
8-Lead LFCSP_VD (CP-8-9)	57	12	$^{\circ}\text{C}/\text{W}$

¹ θ_{JA} is specified for worst-case conditions, that is, θ_{JA} is specified for device soldered in circuit board for surface-mount packages.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

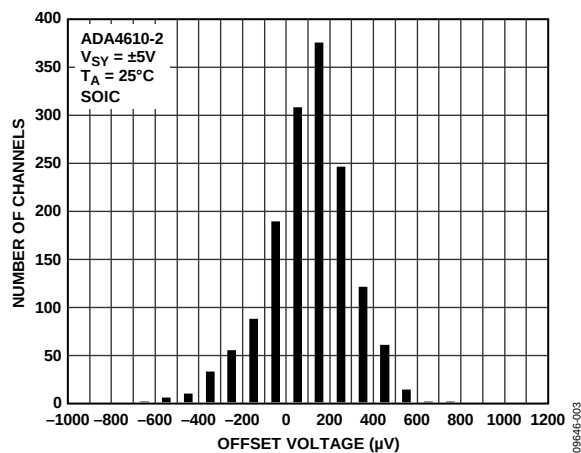


Figure 3. Input Offset Voltage Distribution

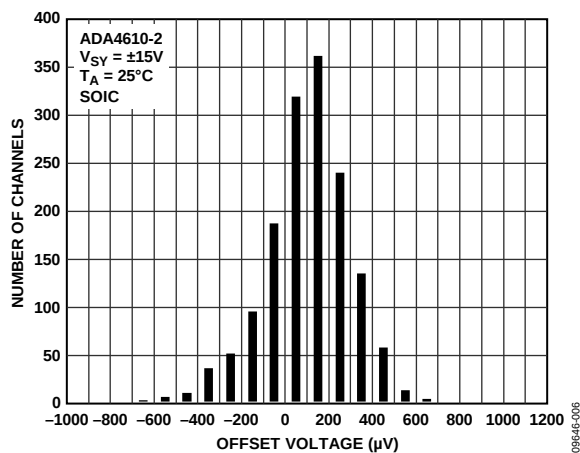


Figure 6. Input Offset Voltage Distribution

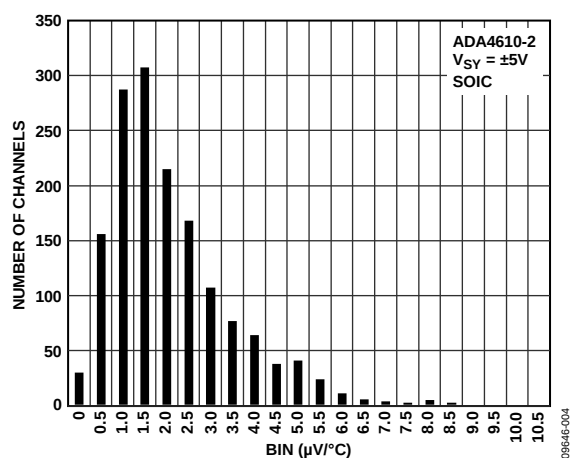


Figure 4. $T_C V_{OS}$ Distribution

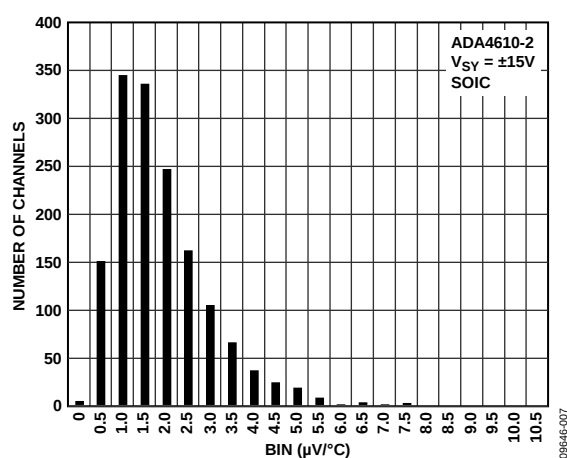


Figure 7. $T_C V_{OS}$ Distribution

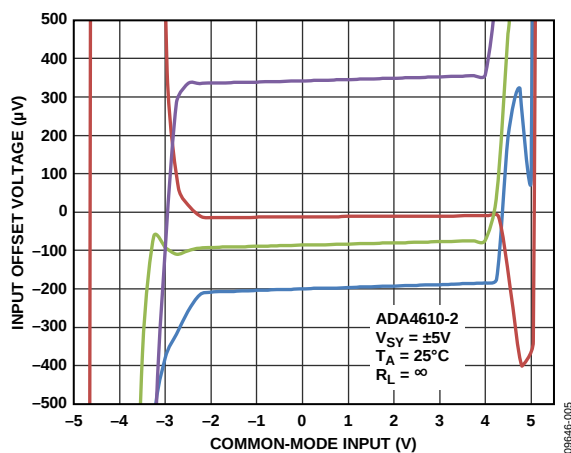


Figure 5. Input Offset Voltage vs. Common-Mode Input Voltage

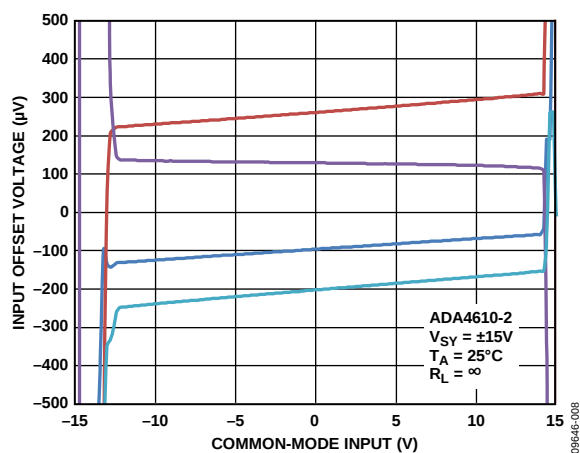


Figure 8. Input Offset Voltage vs. Common-Mode Input Voltage

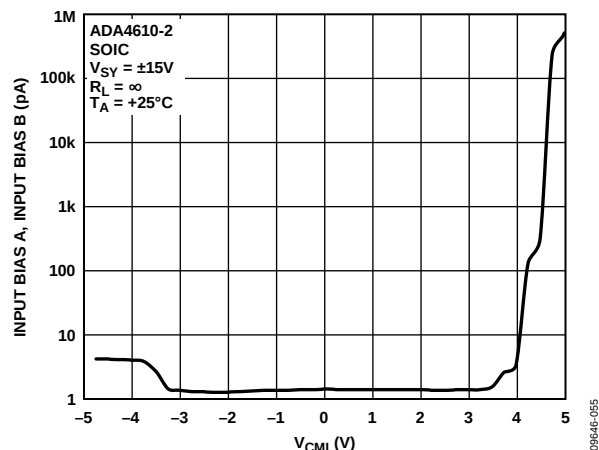


Figure 9. Input Bias Current vs. Common Mode Voltage

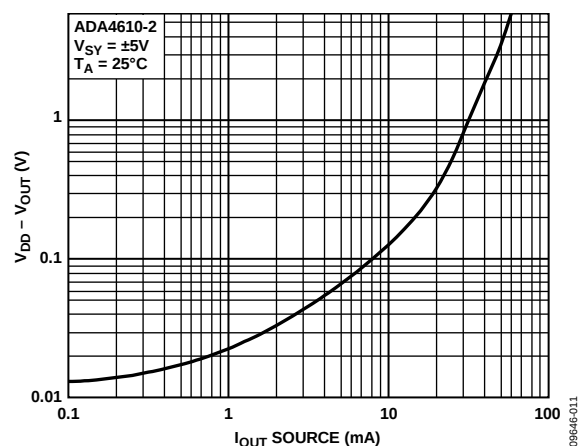


Figure 12. Dropout Voltage vs. Source Current

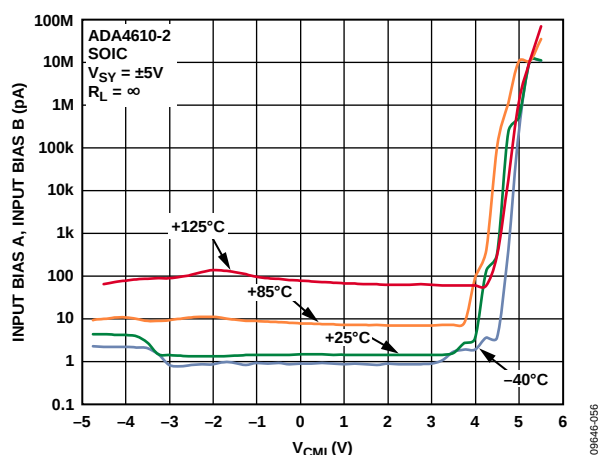


Figure 10. Input Bias Current vs. Common Mode Voltage and Temperature

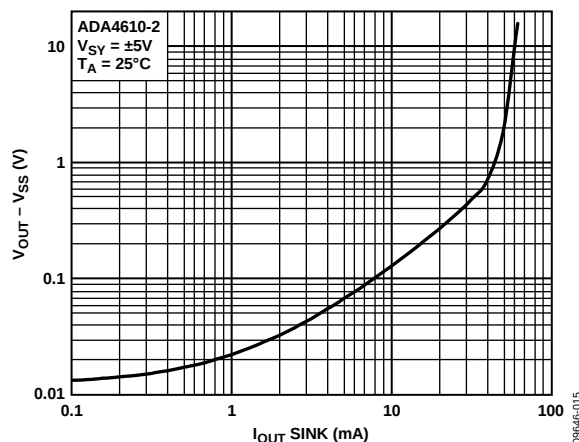


Figure 13. Dropout Voltage vs. Sink Current

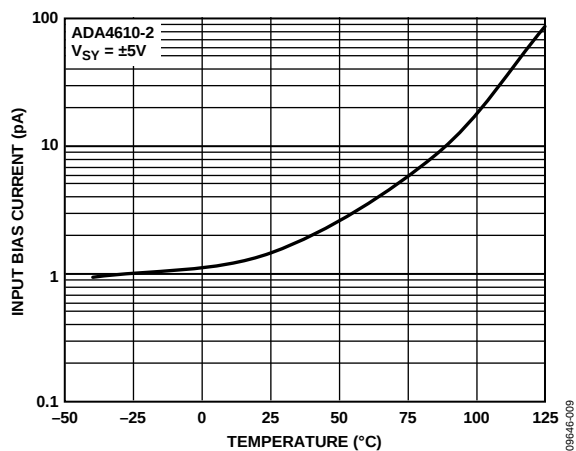


Figure 11. Input Bias Current vs. Temperature

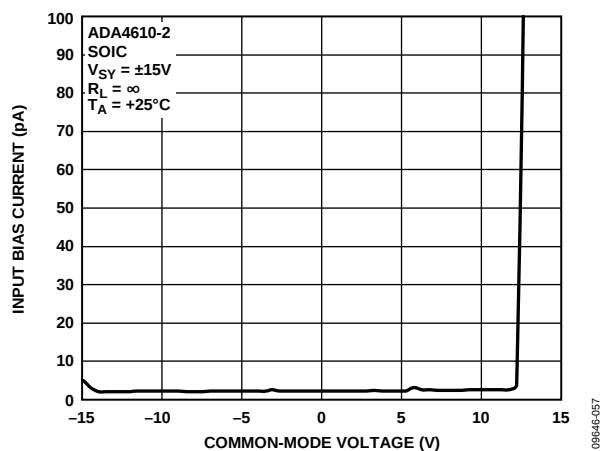


Figure 14. Input Bias Current vs. Common-Mode Voltage

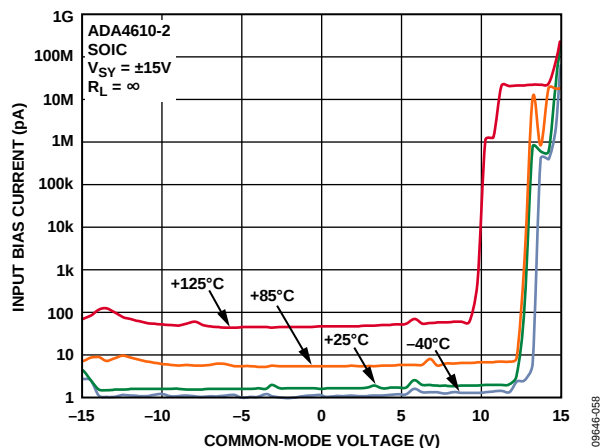


Figure 15. Input Bias Current vs. Common-Mode Voltage and Temperature

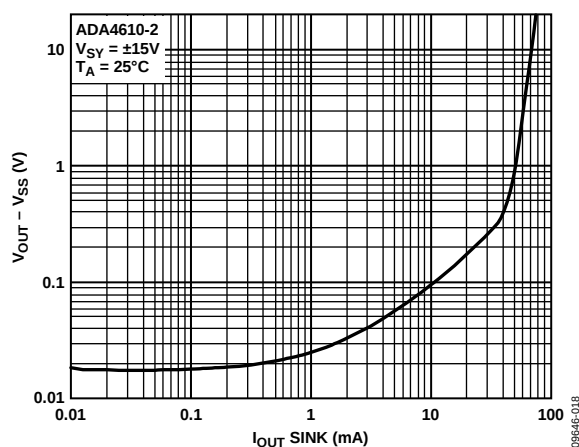


Figure 18. Dropout Voltage vs. Sink Current

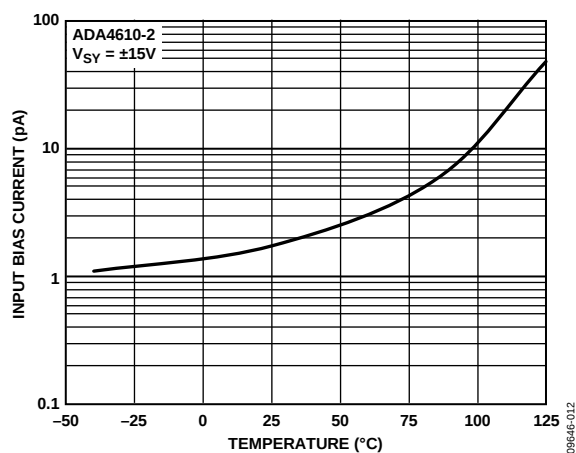


Figure 16. Input Bias Current vs. Temperature

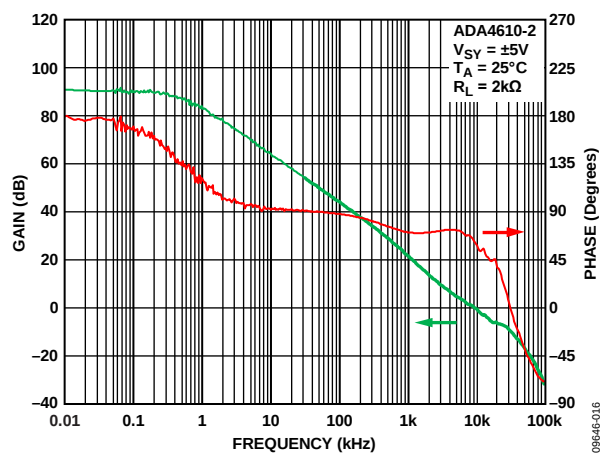


Figure 19. Open-Loop Gain and Phase vs. Frequency

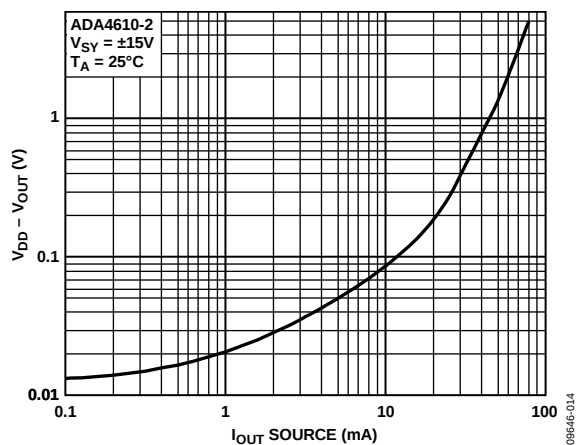


Figure 17. Dropout Voltage vs. Source Current

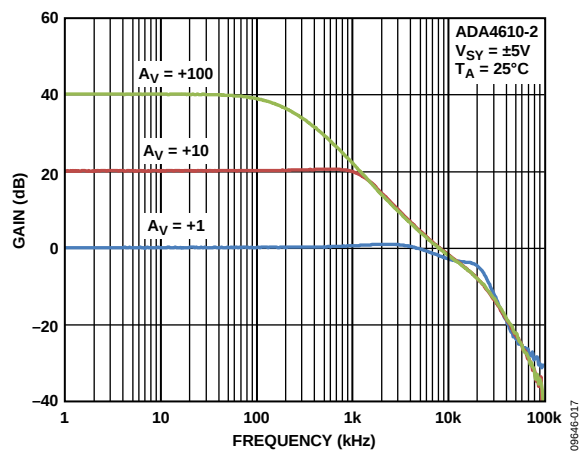


Figure 20. Closed-Loop Gain vs. Frequency

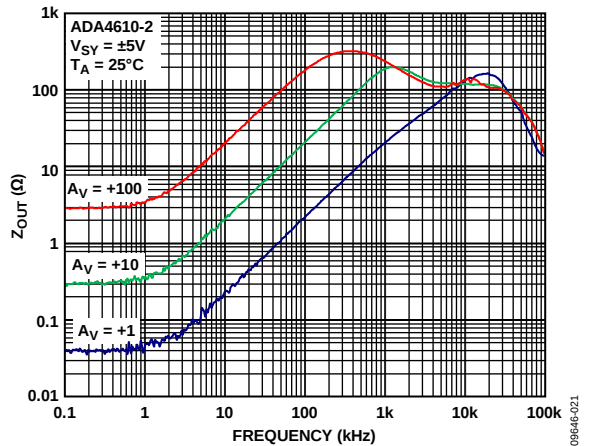


Figure 21. Closed-Loop Output Impedance vs. Frequency

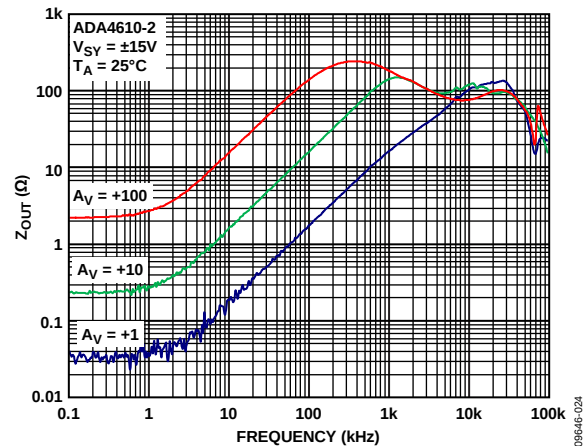


Figure 24. Closed-Loop Output Impedance vs. Frequency

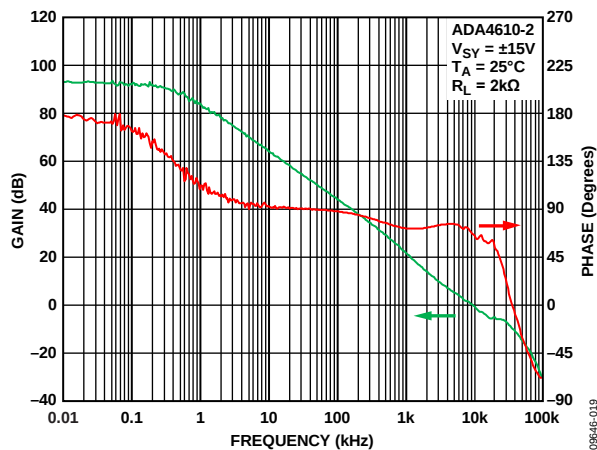


Figure 22. Open-Loop Gain and Phase vs. Frequency

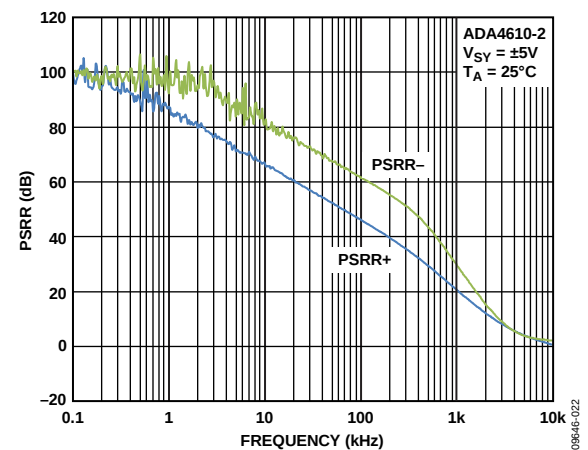


Figure 25. PSRR vs. Frequency

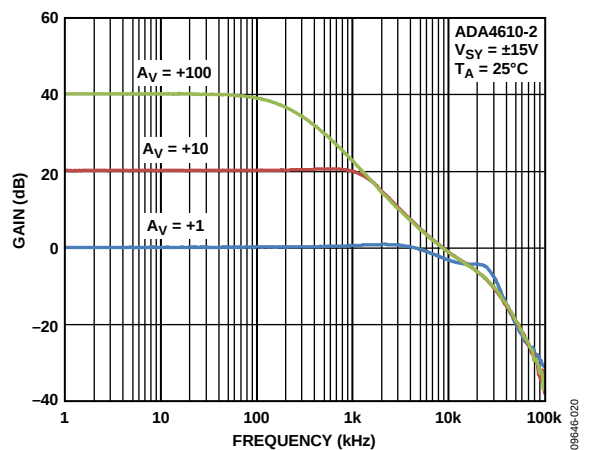


Figure 23. Closed-Loop Gain vs. Frequency

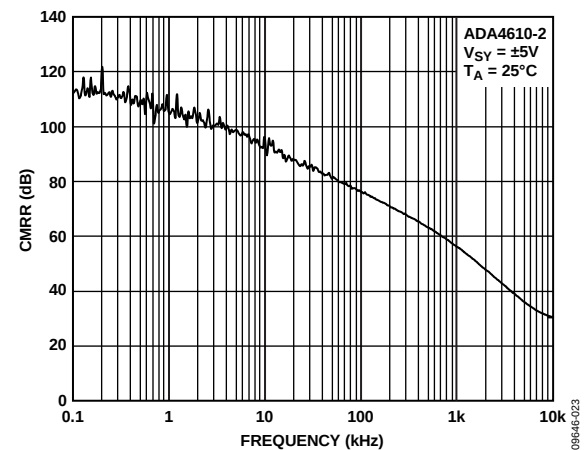


Figure 26. CMRR vs. Frequency

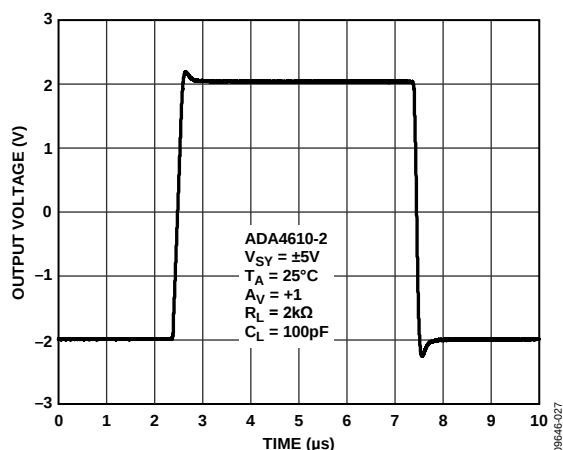


Figure 27. Large Signal Transient Response

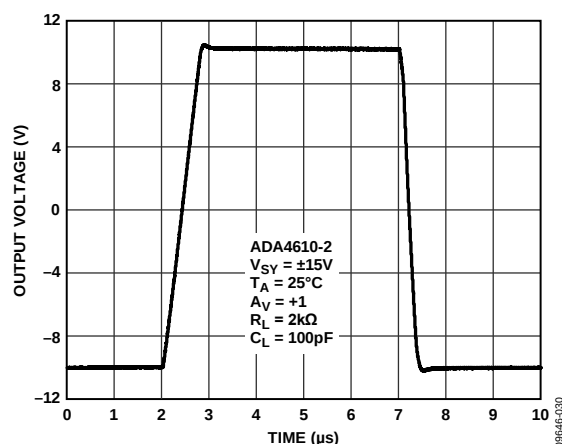


Figure 30. Large Signal Transient Response

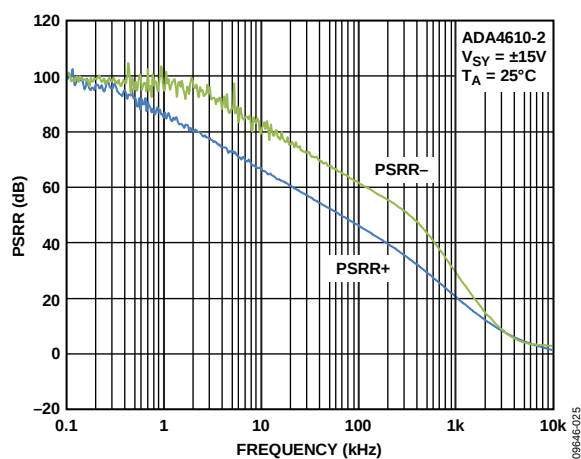


Figure 28. PSRR vs. Frequency

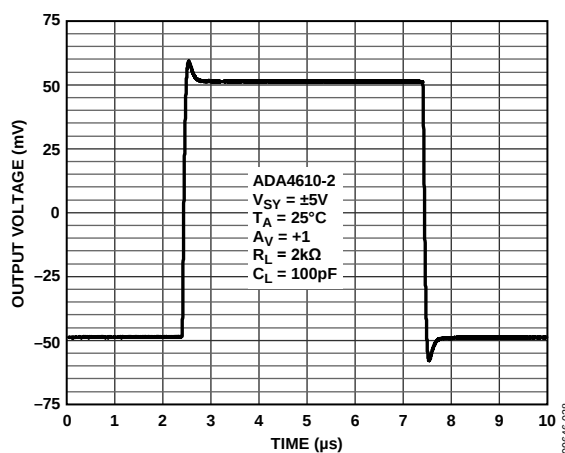


Figure 31. Small Signal Transient Response

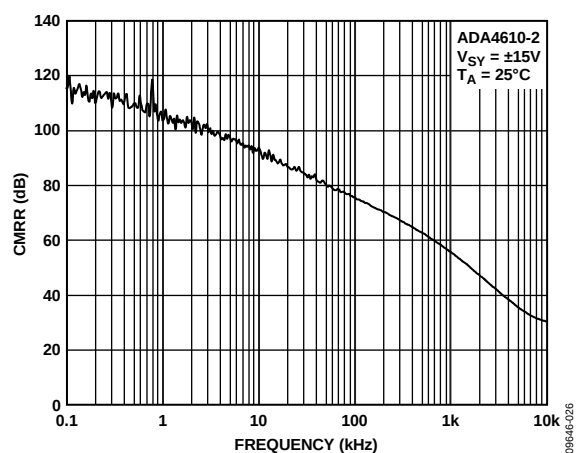


Figure 29. CMRR vs. Frequency

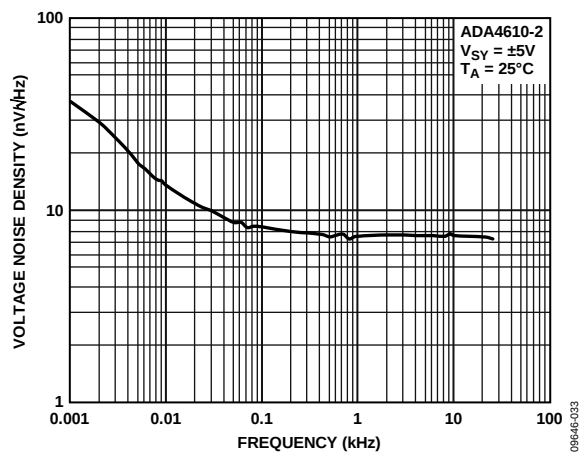


Figure 32. Voltage Noise Density

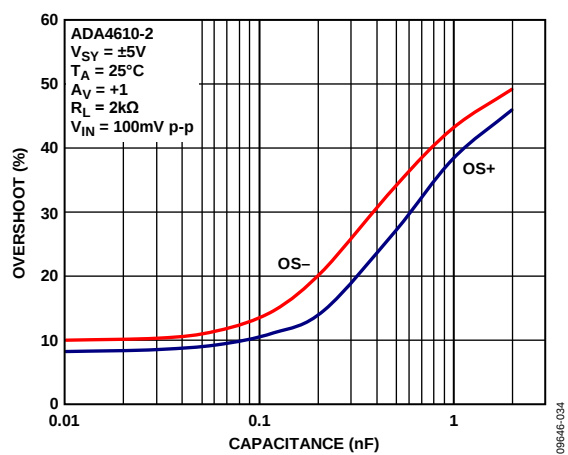


Figure 33. Overshoot vs. Load Capacitance

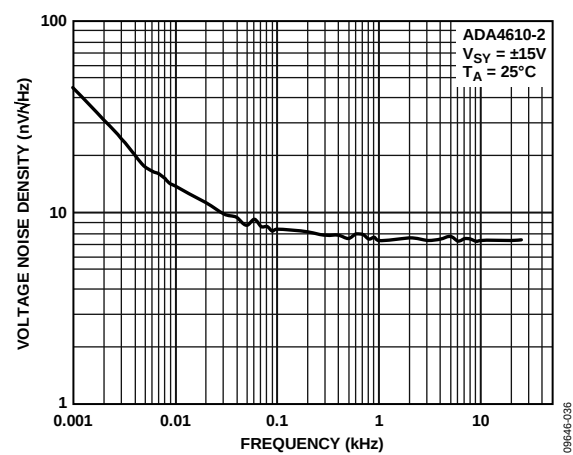


Figure 35. Voltage Noise Density

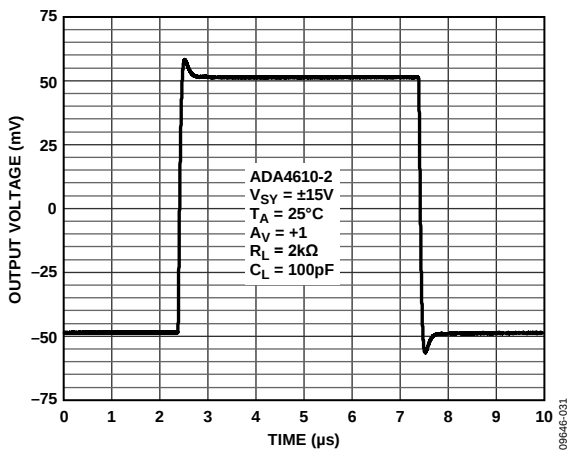


Figure 34. Small Signal Transient Response

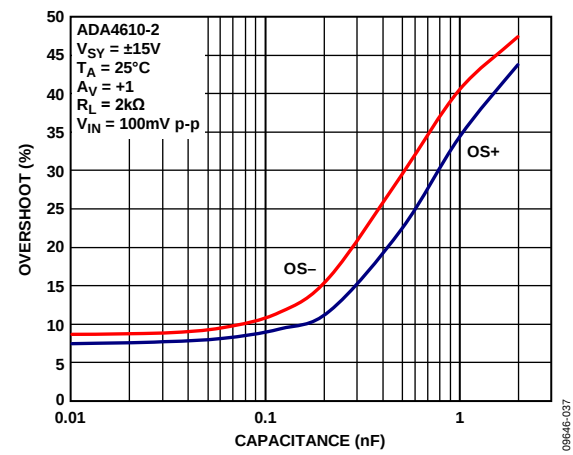


Figure 36. Overshoot vs. Load Capacitance

COMPARATIVE VOLTAGE AND VARIABLE VOLTAGE GRAPHS

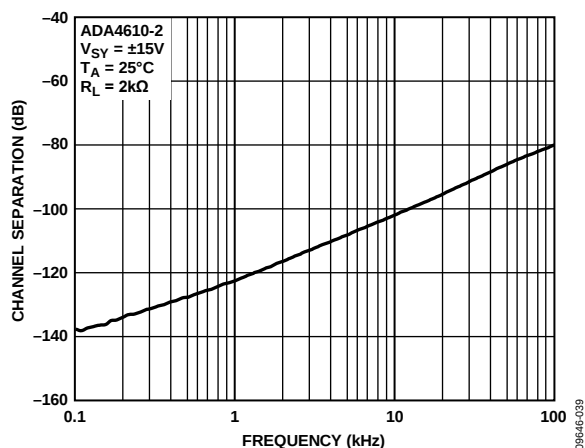


Figure 37. Channel Separation

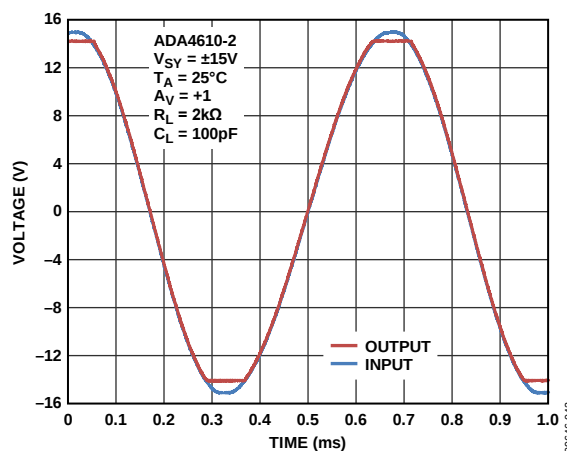


Figure 40. No Phase Reversal

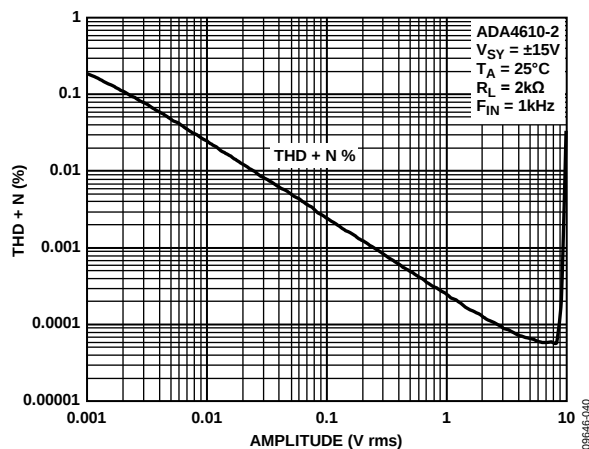


Figure 38. THD + N vs. Amplitude

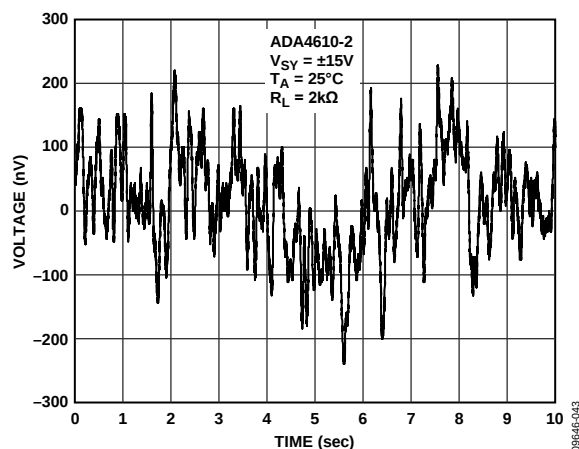


Figure 41. Voltage Noise, 0.1 Hz to 10 Hz

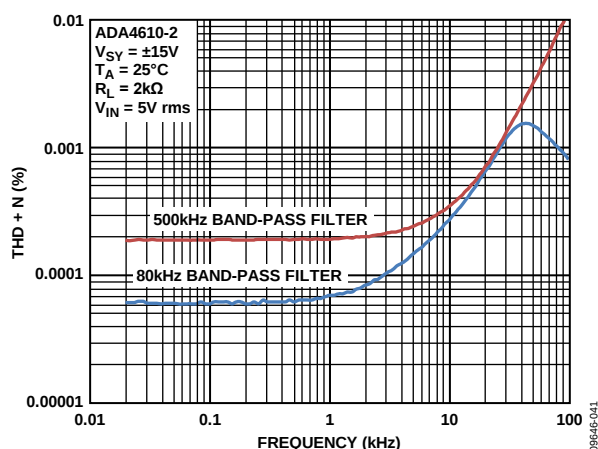


Figure 39. THD + N vs. Frequency

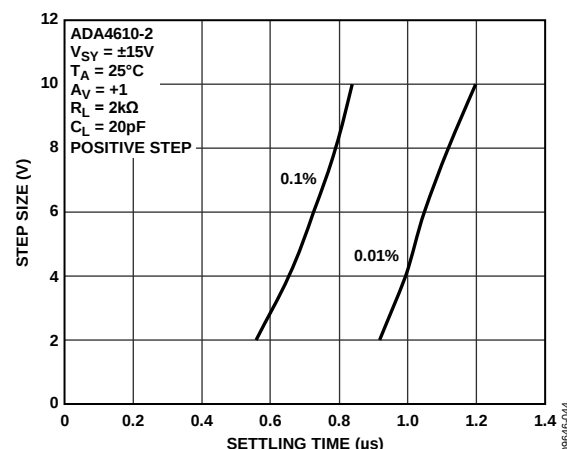


Figure 42. Positive Step Settling Time

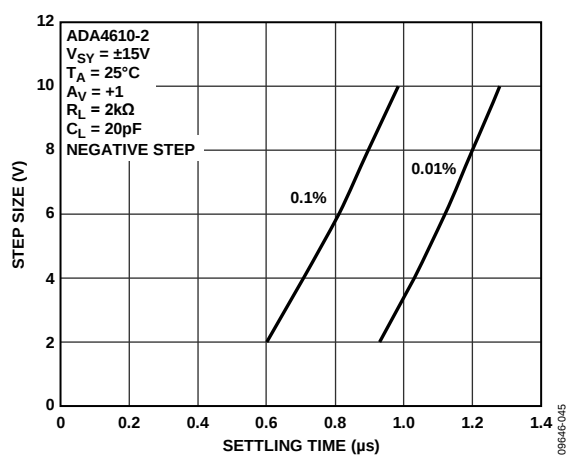


Figure 43 Negative Step Settling Time

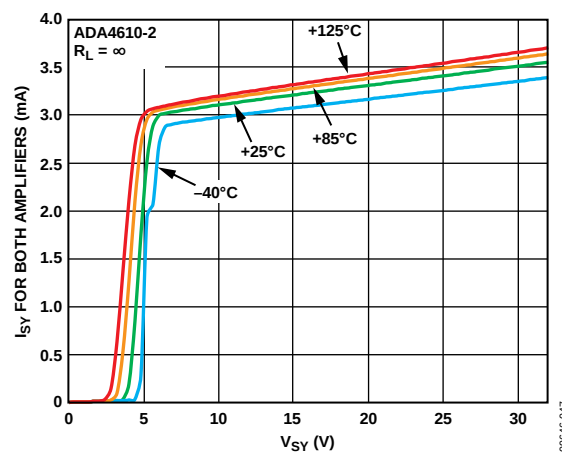


Figure 44. Supply Current vs. Supply Voltage and Temperature

APPLICATIONS INFORMATION

COMPARATOR OPERATION

Although op amps are quite different from comparators, occasionally an unused section of a dual or a quad op amp may be used as a comparator; however, this is not recommended for any rail-to-rail output op amp. For rail-to-rail output op amps, the output stage is generally a ratioed current mirror with bipolar or MOSFET transistors. With the part operating open loop, the second stage increases the current drive to the ratioed mirror to close the loop. However, the second stage cannot close the loop, which results in an increase in supply current. With the op amp configured as a comparator, the supply current can be significantly higher (see Figure 45). Configuring an unused section as a voltage follower with the noninverting input connected to a voltage within the input voltage range is recommended. The ADA4610-2 has a unique output stage design that reduces the excess supply current, but does not entirely eliminate this effect when the op amp is operating open loop.

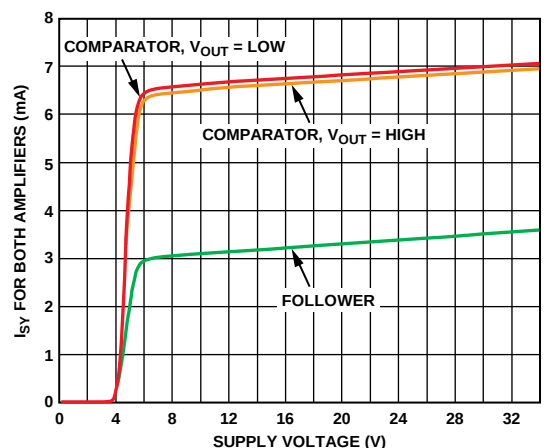


Figure 45. Supply Current vs. Supply Voltage

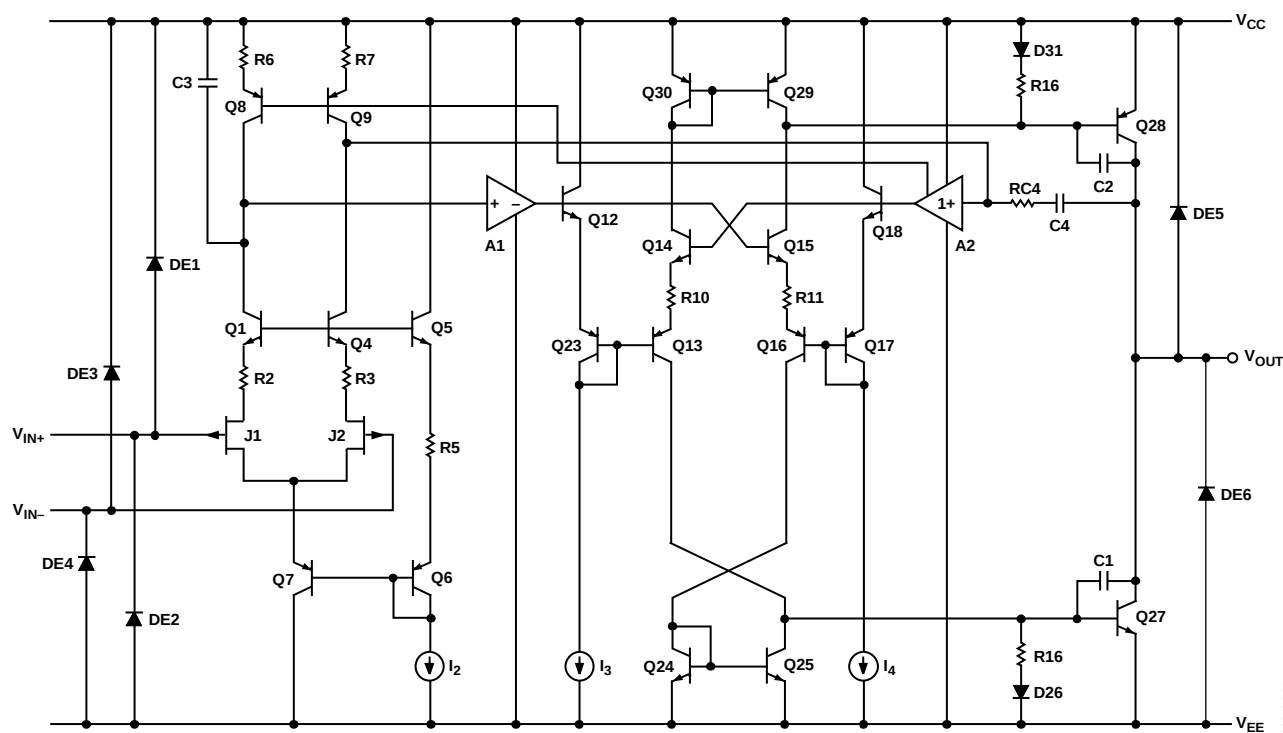
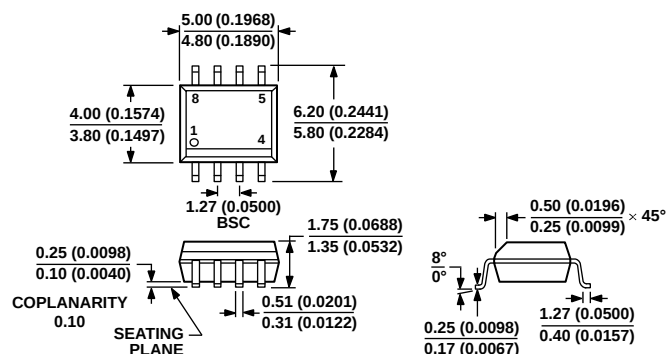


Figure 46. Simplified Schematic

OUTLINE DIMENSIONS

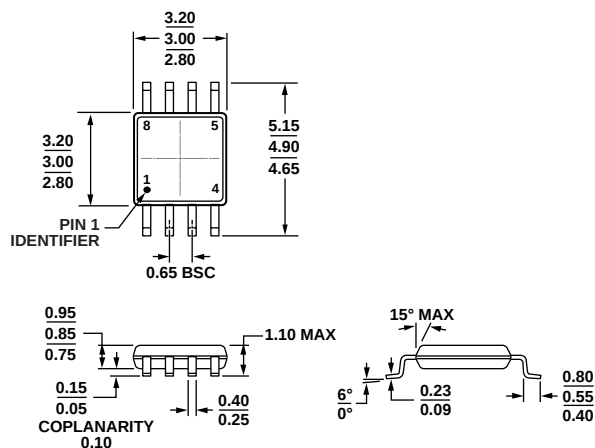


COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 47. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

022407-A



COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 48. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)

Dimensions shown in millimeters

10-07-2009-B

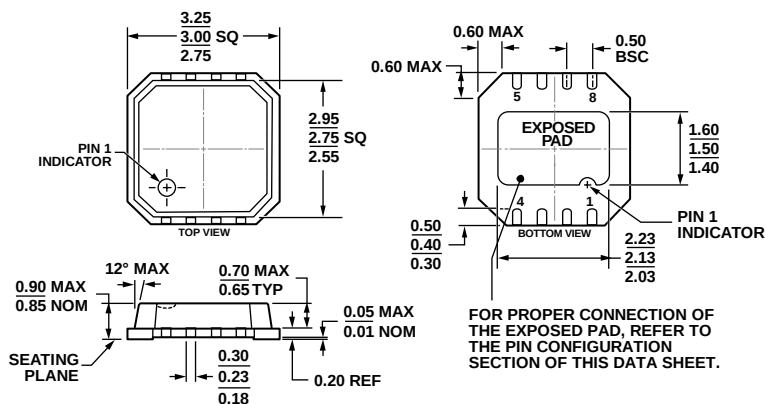


Figure 49. 8-Lead Lead Frame Chip Scale Package [LFCSP_VD]
 3 mm × 3 mm Body, Very Thin, Dual Lead
 (CP-8-9)
 Dimensions shown in millimeters

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option	Branding
ADA4610-2ACPZ-R7	−40°C to +125°C	8-Lead LFCSP_VD	CP-8-9	A2U
ADA4610-2ACPZ-RL	−40°C to +125°C	8-Lead LFCSP_VD	CP-8-9	A2U
ADA4610-2ARMZ	−40°C to +125°C	8-Lead MSOP	RM-8	A2U
ADA4610-2ARMZ-R7	−40°C to +125°C	8-Lead MSOP	RM-8	A2U
ADA4610-2ARMZ-RL	−40°C to +125°C	8-Lead MSOP	RM-8	A2U
ADA4610-2ARZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4610-2ARZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4610-2ARZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4610-2BRZ	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4610-2BRZ-R7	−40°C to +125°C	8-Lead SOIC_N	R-8	
ADA4610-2BRZ-RL	−40°C to +125°C	8-Lead SOIC_N	R-8	

¹ Z = RoHS Compliant Part.

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