ANALOG DEVICES

LC²MOS High-Speed 12-Bit ADC

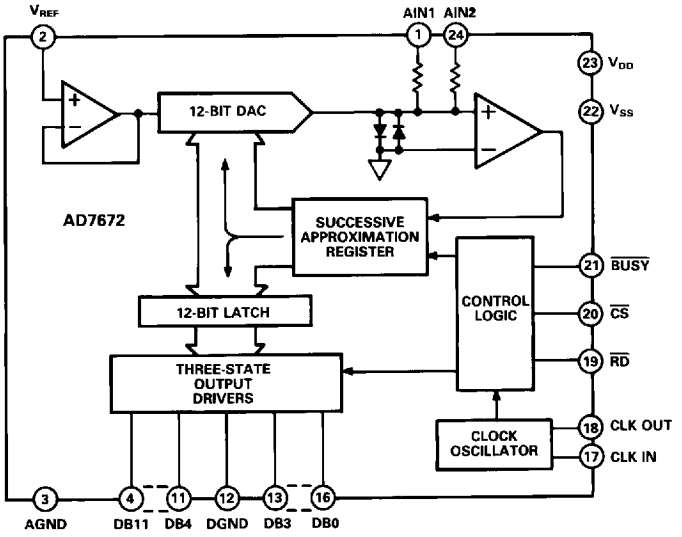
AD7672

FEATURES

12-Bit Resolution and Accuracy
Fast Conversion Time
- **AD7672XX03 – 3μs**
- **AD7672XX05 – 5μs**
- **AD7672XX10 – 10μs**

Unipolar or Bipolar Input Ranges
Low Power: 110mW
Fast Bus Access Times: 90ns
Small, 0.3", 24-Pin Package and 28-Terminal Surface Mount Packages

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7672 is a high-speed 12-bit ADC, fabricated in an advanced, mixed technology, Linear-Compatible CMOS (LC²MOS) process, which combines precision bipolar components with low-power, high-speed CMOS logic. The AD7672 uses an accurate high-speed DAC and comparator in an otherwise conventional successive-approximation loop to achieve conversion times as low as 3μs while dissipating only 110mW of power.

To allow maximum flexibility the AD7672 is designed for use with an external reference voltage. This allows the user to choose a reference whose performance suits the application or to drive many AD7672s from a single system reference, since the reference input of the AD7672 is buffered and draws little current. For digital signal processing applications where absolute accuracy and temperature coefficients may be unimportant, a low-cost reference can be used. For maximum precision, the AD7672 can be used with a high-accuracy reference, such as the AD588, when absolute 12-bit accuracy can be obtained over a wide temperature range.

An on-chip clock-circuit is provided which may be used with a crystal for accurate definition of conversion time. Alternatively, the clock input may be driven from an external source such as a microprocessor clock.

The AD7672 also offers flexibility in its analog input ranges, with a choice of 0 to +5V, 0 to +10V and ±5V.

The AD7672 is also designed to operate from nominal supply voltages of +5V and −12V. This makes it an ideal choice for data acquisition cards in personal computers where the negative supply is generally −12V.

The AD7672 has a high-speed digital interface with three-state data outputs and standard microprocessor control inputs (Chip Select and Read). Bus access time of only 90ns allows the AD7672 to be interfaced to most modern microprocessors.

The AD7672 is available in a variety of space-saving packages; plastic and hermetic 24-pin "skinny" DIP and 28-pin ceramic and plastic chip carrier.

PRODUCT HIGHLIGHTS

1. Fast, 3μs, 5μs and 10μs conversion speeds make the AD7672 ideal for a wide range of applications in telecommunications, sonar and radar signal processing or any high-speed data acquisition system.
2. LC²MOS circuitry gives high precision with low power drain (110mW typ).
3. Choice of 0 to +5V, 0 to +10V or ±5V input ranges, accomplished by pin-strapping.
4. Fast, simple, digital interface has a bus access time of 90ns allowing easy connection to most microprocessors.
5. Available in space-saving 24-pin, 0.3" DIP or surface mount package.

REV. A

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AD7672—SPECIFICATIONS

(V_{DD} = 5V ± 5%, V_{SS} = −12V ± 10%, V_{REF} = −5V unless otherwise noted. f_{CLK}: 4MHz for AD7672XX03, 2.5MHz for AD7672XX05, 1.25MHz for AD7672XX10. All Specifications T_{min} to T_{max} unless otherwise noted. Specifications apply to Slow Memory Mode.)

Parameter	K Version[1]	L Version[1]	B Version[1]	C Version[1]	Units	Test Conditions/Comments
ACCURACY[2]						
Resolution	12	12	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	±1	±1/2	LSB max	Tested Range ±5V
T_{min} to T_{max}	±1	±1/2	±1	±1/2	LSB max	
Differential Nonlinearity	±0.9	±0.9	±0.9	±0.9	LSB max	No Missing Codes Guaranteed
Unipolar Offset Error @ +25°C	±5	±3	±5	±3	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±6	±4	±6	±4	LSB max	Typical TC is 2ppm/°C
Unipolar Gain Error @ +25°C	±5	±4	±5	±4	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±7	±6	±7	±6	LSB max	Typical TC is 2ppm/°C
Bipolar Zero Error @ +25°C	±5	±3	±5	±3	LSB max	Input Range: ±5V
T_{min} to T_{max}	±6	±4	±6	±4	LSB max	Typical TC is 2ppm/°C
Bipolar Gain Error @ +25°C	±5	±4	±5	±4	LSB max	Input Range: ±5V
T_{min} to T_{max}	±7	±6	±7	±6	LSB max	Typical TC is 2ppm/°C
ANALOG INPUT						
Unipolar Input Current	3.5	3.5	3.5	3.5	mA max	Input Ranges: 0 to 5V or 0 to 10V
Bipolar Input Current	±1.75	±1.75	±1.75	±1.75	mA max	Input Range: ±5V
REFERENCE INPUT						
V_{REF} (For Specified Performance)	−5	−5	−5	−5	Volts	±1%
Input Reference Current	−3	−3	−3	−3	μA max	
POWER SUPPLY REJECTION						
V_{DD} Only, (FS Change)	±1	±1	±1	±1	LSB typ	V_{SS} = −12V, V_{DD} = +4.75V to +5.25V
V_{SS} Only, (FS Change)	±1	±1	±1	±1	LSB typ	V_{DD} = +5V, V_{SS} = −10.8V to −13.2V
LOGIC INPUTS						
$\overline{CS}$, $\overline{RD}$, CLK IN						
V_{INL}, Input Low Voltage	+0.8	+0.8	+0.8	+0.8	V max	V_{DD} = 5V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	+2.4	+2.4	V min	
C_{IN},[3] Input Capacitance	10	10	10	10	pF max	
$\overline{CS}$, $\overline{RD}$						
I_{IN}, Input Current	±10	±10	±10	±10	μA max	V_{IN} = 0 to V_{DD}
CLK IN						
I_{IN}, Input Current	±20	±20	±20	±20	μA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS						
DB11–DB0, $\overline{BUSY}$, CLK OUT						
V_{OL}, Output Low Voltage	+0.4	+0.4	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	+4.0	+4.0	+4.0	+4.0	V min	I_{SOURCE} = 200μA
Floating-State Leakage Current						
DB11–DB0	±10	±10	±10	±10	μA max	
Floating-State Output Capacitance[3]	15	15	15	15	pF max	
CONVERSION TIME						
AD7672XX03						Applies to K and B Grades Only
Synchronous Clock	3.125	–	3.125	–	μs max	f_{CLK} = 4MHz. See Under
Asynchronous Clock	3/3.25	–	3/3.25	–	μs min/max	Control Inputs Synchronization
AD7672XX05						
Synchronous Clock	5	5	5	5	μs max	f_{CLK} = 2.5MHz
Asynchronous Clock	4.8/5.2	4.8/5.2	4.8/5.2	4.8/5.2	μs min/max	
AD7672XX10						
Synchronous Clock	10	10	10	10	μs max	f_{CLK} = 1.25MHz
Asynchronous Clock	9.6/10.4	9.6/10.4	9.6/10.4	9.6/10.4	μs min/max	
POWER REQUIREMENTS						
V_{DD}	+5	+5	+5	+5	VNOM	±5% for Specified Performance
V_{SS}	−12	−12	−12	−12	VNOM	±10% for Specified Performance
I_{DD}[4]	7	7	7	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
I_{SS}[4]	−12	−12	−12	−12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
Power Dissipation	110	110	110	110	mW typ	
	179	179	179	179	mW max	

NOTES

[1]Temperature range as follows: K, L Versions; 0 to +70°C.
B, C Versions; −25°C to +85°C.

[2]V_{DD} = 5V, V_{SS} = −12V, 1LSB = FS/4096

[3]Sample tested to ensure compliance.

[4]Power supply current is measured when AD7672 is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.

Specifications subject to change without notice.

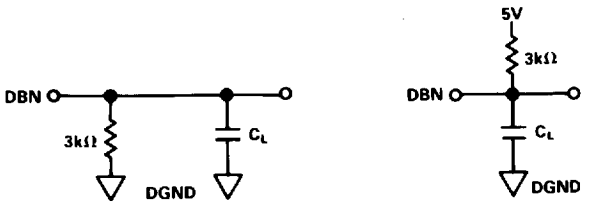
Parameter	T Version[1]	U Version[1]	Units	Test Conditions/Comments
ACCURACY[2]				
Resolution	12	12	Bits	
Integral Nonlinearity @ +25°C	±1	±1/2	LSB max	Tested Range ±5V
T_{min} to T_{max}	±1	±3/4	LSB max	
Differential Nonlinearity	±0.9	±0.9	LSB max	No Missing Codes Guaranteed
Unipolar Offset Error @ +25°C	±5	±3	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±6	±4	LSB max	Typical TC is 2ppm/°C
Unipolar Gain Error @ +25°C	±5	±4	LSB max	Input Range: 0 to 5V or 0 to 10V
T_{min} to T_{max}	±7	±6	LSB max	Typical TC is 2ppm/°C
Bipolar Zero Error @ +25°C	±5	±3	LSB max	Input Range: ±5V
T_{min} to T_{max}	±6	±4	LSB max	Typical TC is 2ppm/°C
Bipolar Gain Error @ +25°C	±5	±4	LSB max	Input Range: ±5V
T_{min} to T_{max}	±7	±6	LSB max	Typical TC is 2ppm/°C
ANALOG INPUT				
Unipolar Input Current	3.5	3.5	mA max	Input Ranges: 0 to 5V or 0 to 10V
Bipolar Input Current	±1.75	±1.75	mA max	Input Range: ±5V
REFERENCE INPUT				
V_{REF} (For Specified Performance)	−5	−5	Volts	±1%
Input Reference Current	−3	−3	μA max	
POWER SUPPLY REJECTION				
V_{DD} Only, (FS Change)	±1	±1	LSB typ	V_{SS} = −12V, V_{DD} = +4.75V to +5.25V
V_{SS} Only, (FS Change)	±1	±1	LSB typ	V_{DD} = +5V, V_{SS} = −10.8V to −13.2V
LOGIC INPUTS				
$\overline{CS}$, $\overline{RD}$, CLK IN				
V_{INL}, Input Low Voltage	+0.8	+0.8	V max	V_{DD} = 5V ±5%
V_{INH}, Input High Voltage	+2.4	+2.4	V min	
C_{IN},[3] Input Capacitance	10	10	pF max	
$\overline{CS}$, $\overline{RD}$				
I_{IN}, Input Current	±10	±10	μA max	V_{IN} = 0 to V_{DD}
CLK IN				
I_{IN}, Input Current	±20	±20	μA max	V_{IN} = 0 to V_{DD}
LOGIC OUTPUTS				
DB11–DB0, $\overline{BUSY}$, CLK OUT				
V_{OL}, Output Low Voltage	+0.4	+0.4	V max	I_{SINK} = 1.6mA
V_{OH}, Output High Voltage	+4.0	+4.0	V min	I_{SOURCE} = 200μA
Floating-State Leakage Current				
DB11–DB0	±10	±10	μA max	
Floating-State Output Capacitance[3]	15	15	pF max	
CONVERSION TIME				
AD7672XX05				
Synchronous Clock	5	5	μs max	f_{CLK} = 2.5MHz. See Under
Asynchronous Clock	4.8/5.2	4.8/5.2	μs min/max	Control Inputs Synchronization
AD7672XX10				
Synchronous Clock	10	10	μs max	f_{CLK} = 1.25MHz
Asynchronous Clock	9.6/10.4	9.6/10.4	μs min/max	
POWER REQUIREMENTS				
V_{DD}	+5	+5	VNOM	±5% for Specified Performance
V_{SS}	−12	−12	VNOM	±10% for Specified Performance
I_{DD}[4]	7	7	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
I_{SS}[4]	−12	−12	mA max	$\overline{CS}$ = $\overline{RD}$ = V_{DD}, AIN1 = AIN2 = 5V
Power Dissipation	110	110	mW typ	
	179	179	mW max	

NOTES
[1]Temperature range as follows: T, U Versions; −55°C to +125°C.
[2]V_{DD} = 5V, V_{SS} = −12V, 1LSB = FS/4096
[3]Sample tested to ensure compliance.
[4]Power supply current is measured when AD7672 is inactive, i.e., $\overline{CS}$ = $\overline{RD}$ = $\overline{BUSY}$ = HIGH.
Specifications subject to change without notice.

TIMING CHARACTERISTICS[1] (V_{DD} = 5V, V_{SS} = −12V)

Parameter	Limit at +25°C (All Grades)	Limit at T_{min}, T_{max} (K, L, B, C Grades)	Limit at T_{min}, T_{max} (T, U Grades)	Units	Conditions/Comments
t_1	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Setup Time
t_2	190	230	270	ns max	$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay
t_3[2]	90	110	120	ns max	Data Access Time after $\overline{RD}$, C_L = 20pF
	125	150	170	ns max	Data Access Time after $\overline{RD}$, C_L = 100pF
t_4	t_3	t_3	t_3	ns min	$\overline{RD}$ Pulse Width
t_5	0	0	0	ns min	$\overline{CS}$ to $\overline{RD}$ Hold Time
t_6[2]	70	90	100	ns max	Data Setup Time after $\overline{BUSY}$
t_7[3]	20	20	20	ns min	Bus Relinquish Time
	75	85	90	ns max	
t_8	200	200	200	ns min	Delay Between Successive Read Operations

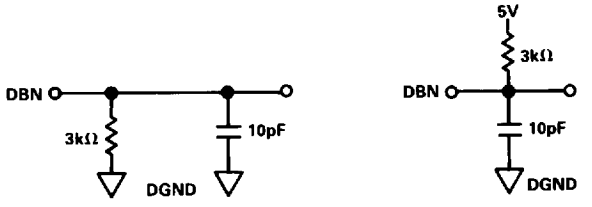
NOTES
[1]Timing Specifications are sample tested at +25°C to ensure compliance. All input control signals are specified with tr = tf = 5ns (10% to 90% of +5V) and timed from a voltage level of 1.6V.
[2]t_3 and t_6 are measured with the load circuits of Figure 1 and defined as the time required for an output to cross 0.8V or 2.4V.
[3]t_7 is defined as the time required for the data lines to change 0.5V when loaded with the circuits of Figure 2.
Specifications subject to change without notice.



a. High-Z to V_{OH} (t_3) and V_{OL} to V_{OH} (t_6)

b. High-Z to V_{OL} (t_3) and V_{OH} to V_{OL} (t_6)

Figure 1. Load Circuits for Access Time



a. V_{OH} to High-Z

b. V_{OL} to High-Z

Figure 2. Load Circuits for Output Float Delay

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

V_{DD} to DGND	−0.3V to +7V
V_{SS} to DGND	+0.3V to −17V
AGND to DGND	−0.3V to V_{DD} +0.3V
AIN1, AIN2 to AGND	−15V to +15V
V_{REF} to AGND	V_{SS} −0.3V to V_{DD} +0.3V
Digital Input Voltage to DGND (CLK IN, $\overline{CS}$, $\overline{RD}$)	−0.3V to V_{DD} +0.3V
Digital Output Voltage to DGND (DB11-DB0, $\overline{BUSY}$, CLK OUT)	−0.3V to V_{DD} +0.3V
Operating Temperature Range	
K, L	0 to +70°C
B, C	−25°C to +85°C
T, U	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C
Power Dissipation (Any Package) to +75°C	1,000mW
Derates above +75°C by	10mW/°C

*Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

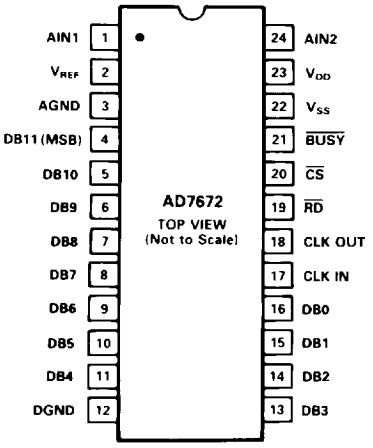
CAUTION
ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

DIP PIN FUNCTION DESCRIPTION

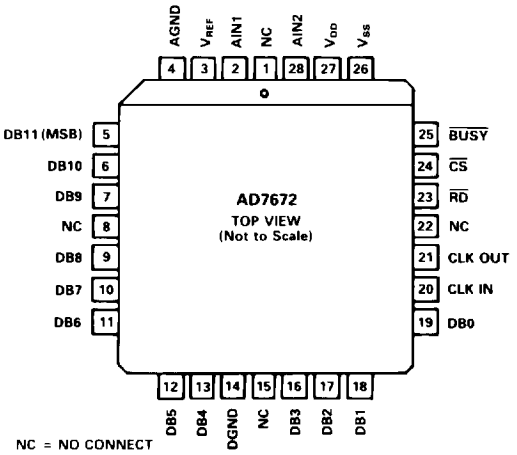
DIP Pin No.	Mnemonic	Description
1	AIN1	Analog Input.
2	V_{REF}	Voltage Reference Input. The AD7672 is specified with $V_{REF} = -5V$.
3	AGND	Analog Ground.
4 . . . 11	DB11 . . .DB4	Three-state data outputs. They become active when $\overline{CS}$ and $\overline{RD}$ are brought low. DB11 is the most significant bit (MSB).
13 . . . 16	DB3 . . . DB0	
12	DGND	Digital Ground.
17	CLK IN	Clock Input pin. An external TTL compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output Pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description.
19	$\overline{RD}$	READ input. This active LOW signal, in conjunction with $\overline{CS}$ is used to enable the output data three-state drivers and initiate a conversion.
20	$\overline{CS}$	CHIP SELECT Input. This active LOW signal, in conjunction with $\overline{RD}$ is used to enable the output data three-state drivers and initiate a conversion.
21	$\overline{BUSY}$	$\overline{BUSY}$ output indicates converter status. $\overline{BUSY}$ is LOW during conversion.
22	V_{SS}	Negative Supply, $-12V$.
23	V_{DD}	Positive Supply, $+5V$.
24	AIN2	Analog Input.

PIN CONFIGURATIONS

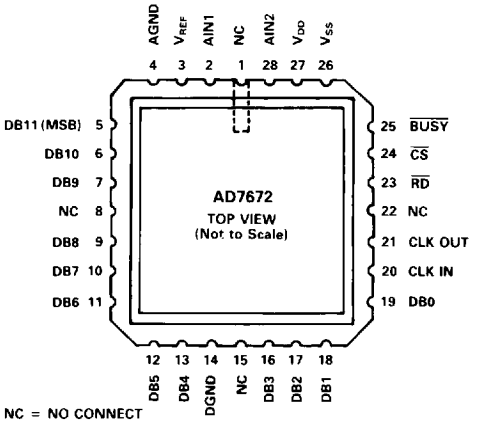
DIP



PLCC



LCCC



TERMINOLOGY

UNIPOLAR OFFSET ERROR
The ideal first code transition should occur when the analog input is 1/2LSB above AGND. The deviation of the actual transition from that point is termed the offset error.

BIPOLAR ZERO ERROR
The ideal midscale transition (i.e., 0111 1111 1111 to 1000 0000 0000) for the ±5V range should occur when the analog input is 1/2LSB below AGND. Bipolar zero error is the deviation of the actual transition from that point.

GAIN ERROR
The ideal difference between the first code transition and last code transition is FS −2LSBs. The Gain error is defined as the deviation between this ideal difference and the measured difference. Ideal FS corresponds to 5V for the unipolar 0 to 5V range and 10V for both the unipolar 0 to 10V and bipolar ±5V ranges.

ORDERING GUIDE

Model[1,2]	Conversion Time	Temperature Range	Accuracy Grade	Package Option[3]
AD7672KN03	3µs	0°C to +70°C	±1LSB	N-24
AD7672BQ03	3µs	−25°C to +85°C	±1LSB	Q-24
AD7672KP03	3µs	0°C to +70°C	±1LSB	P-28A
AD7672BE03	3µs	−25°C to +85°C	±1LSB	E-28A
AD7672KN05	5µs	0°C to +70°C	±1LSB	N-24
AD7672BQ05	5µs	−25°C to +85°C	±1LSB	Q-24
AD7672TQ05	5µs	−55°C to +125°C	±1LSB	Q-24
AD7672LN05	5µs	0°C to +70°C	±1/2LSB	N-24
AD7672CQ05	5µs	−25°C to +85°C	±1/2LSB	Q-24
AD7672UQ05	5µs	−55°C to +125°C	±1/2LSB	Q-24
AD7672KP05	5µs	0°C to +70°C	±1LSB	P-28A
AD7672TE05	5µs	−55°C to +125°C	±1LSB	E-28A
AD7672LP05	5µs	0°C to +70°C	±1/2LSB	P-28A
AD7672UE05	5µs	−55°C to +125°C	±1/2LSB	E-28A
AD7672KN10	10µs	0°C to +70°C	±1LSB	N-24
AD7672BQ10	10µs	−25°C to +85°C	±1LSB	Q-24
AD7672TQ10	10µs	−55°C to +125°C	±1LSB	Q-24
AD7672LN10	10µs	0°C to +70°C	±1/2LSB	N-24
AD7672CQ10	10µs	−25°C to +85°C	±1/2LSB	Q-24
AD7672UQ10	10µs	−55°C to +125°C	±1/2LSB	Q-24
AD7672KP10	10µs	0°C to +70°C	±1LSB	P-28A
AD7672TE10	10µs	−55°C to +125°C	±1LSB	E-28A
AD7672LP10	10µs	0°C to +70°C	±1/2LSB	P-28A
AD7672UE10	10µs	−55°C to +125°C	±1/2LSB	E-28A

NOTES
[1]Analog Devices reserves the right to ship either ceramic (D-24A) or cerdip (Q-24) hermetic packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact local sales office for military data sheet.
[3]D = Ceramic DIP; E = Leadless Ceramic Chip Carrier (LCCC); N = Plastic DIP; P = Plastic Leaded Chip Carrier (PLCC); Q = Cerdip.

OPERATING FROM A NEGATIVE SUPPLY GREATER THAN −12V

The AD7672 is designed to operate with a V_{SS} input of −12V ± 10%. In applications where the negative supply is greater than −12V, then a Zener diode in series with V_{SS} can be used to reduce the supply. The Zener diode should have a dynamic impedance of not greater than 40Ω. An example is given in Figure 3. The diode has a Zener voltage of 3V, which makes it suitable for a negative supply of −15V ± 7%.

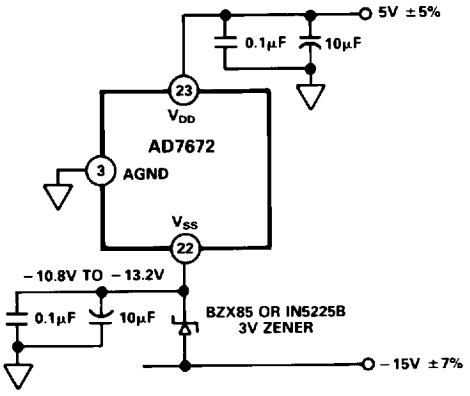


Figure 3. Operation from Nominal Power Supplies of 5V and −15V

CONVERTER DETAILS

Conversion start is controlled by the $\overline{CS}$ and $\overline{RD}$ inputs. At the start of conversion the successive approximation register (SAR) is reset and the three-state data outputs are enabled. Once a conversion cycle has begun it cannot be restarted.

During conversion, the internal 12-bit DAC is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB). Referring to Figure 4, the analog inputs (AIN1 & AIN2) connect to the comparator input via 5kΩ resistors. The DAC which has 2.5kΩ output impedence connects to the same comparator input. Bit decisions are made by the comparator (zero crossing detector) which checks the addition of each successive weighted bit from the DAC output against the analog inputs. The MSB decision is made 80ns (typically) after the second falling edge of CLK IN following a conversion start (see Figure 5). Similarly, the succeeding bit decisions are made approximately 80ns after a CLK IN falling edge until conversion

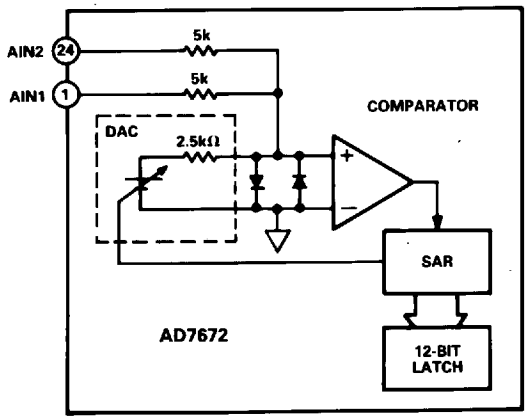


Figure 4. AD7672 AIN Input

is finished. At the end of conversion, the DAC output current balances the current from the analog inputs. The SAR contents (12-bit data word) which represent the analog input signal are loaded into a 12-bit latch.

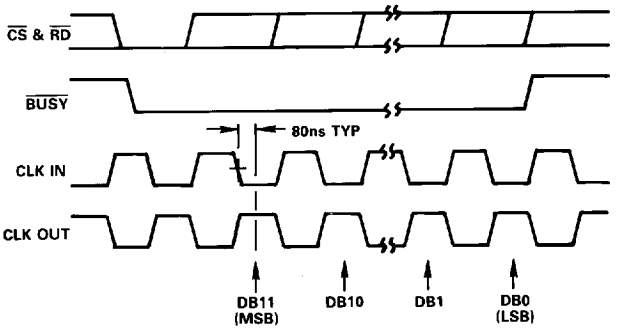


Figure 5. Operating Waveforms Using an External Clock Source for CLK IN

CONTROL INPUTS SYNCHRONIZATION

In applications where the $\overline{RD}$ control input is not synchronized with the ADC clock then conversion time can vary from 12 to 13 CLK IN periods. This is because the ADC waits for the first falling CLK IN edge after conversion start before the conversion procedure begins. Without synchronization, this delay can vary from zero to an entire clock period. If a constant conversion time is required, then the following approach may be used: when initiating a conversion, $\overline{RD}$ must go low on either the rising edge of CLK IN or the falling edge of CLK OUT. This ensures a fixed conversion time that is 12.5 times the CLK IN period.

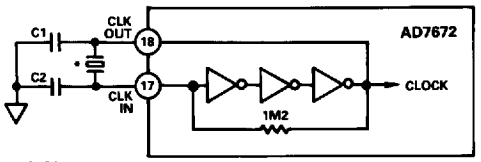
DRIVING THE ANALOG INPUTS

During conversion current from the analog inputs is modulated by the DAC output current at a rate equal to the CLK IN frequency (i.e., 4MHz when CLK IN = 4MHz). This causes voltage spikes (glitches) to appear at the analog inputs. The magnitude and settling time of these glitches depends on the open-loop output impedance and small signal bandwidth of the amplifier or sample and hold driving these inputs. These devices must have sufficient drive to ensure that the glitches have settled within one clock period. An example of a suitable op amp is the AD OP-27. The magnitude of the largest glitch when using this device to drive one of the analog inputs is typically 11mV with a 200ns settling time.

Suitable devices capable of driving the AD7672 analog inputs are the AD OP-27 and AD711 op amps and the AD585 sample-and-hold.

INTERNAL CLOCK OPERATION

Figure 6 shows the AD7672 internal clock circuit. A crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18) to provide a clock oscillator for the ADC timing. Alternatively the crystal/ceramic resonator may be omitted and an external clock source may be connected to CLK IN. For an external clock the mark/space ratio must be 50/50. An inverted CLK IN will appear at the CLK OUT pin as shown in the operating waveforms of Figure 5.



NOTES
AD7672XX03 – 4MHz CRYSTAL/CERAMIC RESONATOR.
AD7672XX05 – 2.5MHz CRYSTAL/CERAMIC RESONATOR.
AD7672XX10 – 1.25MHz CRYSTAL/CERAMIC RESONATOR.
C1 AND C2 CAPACITANCE VALUES DEPEND ON CRYSTAL/CERAMIC RESONATOR MANUFACTURER. TYPICAL VALUES ARE FROM 30pF TO 100pF.

Figure 6. AD7672 Internal Clock Circuit

ANALOG INPUT RANGES

The AD7672 provides three user selectable analog input ranges; 0 to +5V, 0 to +10V and ±5V. Figure 7 shows how to configure the two analog inputs (AIN1 and AIN2) for these ranges.

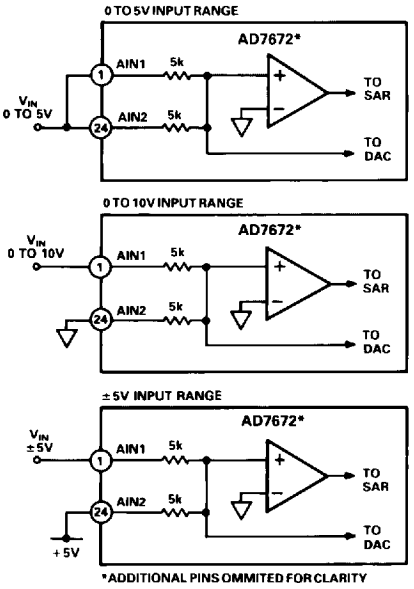


Figure 7. Analog Input Range Configurations

UNIPOLAR OPERATION

Figure 8 shows how to configure an AD584 to produce a reference voltage of −5V for unipolar operation.

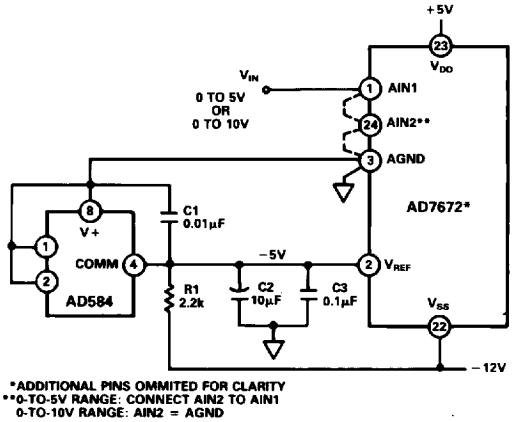


Figure 8. Unipolar Operation Using the AD584 as a Reference

The ideal input/output characteristic is shown in Figure 9. The designed code transitions occur midway between successive integer LSB values (i.e., 1/2LSB, 3/2LSBs . . . FS −3/2 LSBs). The output code is natural binary with 1LSB = FS/4096. FS is either +5V or +10V depending on the analog inputs configuration.

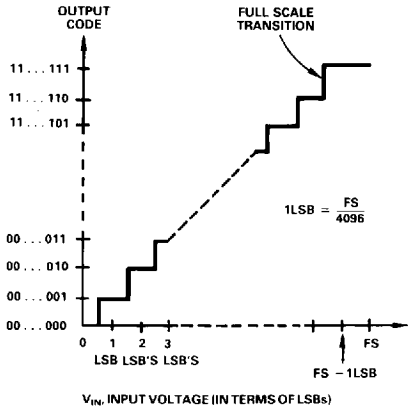


Figure 9. AD7672 Ideal Input/Output Transfer Characteristic for Unipolar Operation.

OFFSET AND FULL-SCALE ERROR

In most Digital Signal Processing (DSP) applications, offset and full-scale error have little or no effect on system performance. A typical example is a digital filter, where an analog input signal is quantized, digitally processed and recreated using a DAC. In these type of applications the offset error can be eliminated by ac coupling the recreated signal. Full-scale error effect is linear and does not cause problems as long as the input signal is within the full dynamic range of the ADC. An important consideration in DSP applications is Differential Nonlinearity and this is not affected by either offset or full-scale error.

UNIPOLAR OFFSET AND FULL-SCALE ERROR ADJUSTMENT

If absolute accuracy is an application requirement then offset and full-scale error can be adjusted to zero. Offset error must be adjusted before full-scale error. Figure 10 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the offset of the op amp driving the analog input (i.e., A1 in Figure 10.). For zero offset error apply a voltage equal to 1/2LSB at V_{IN} and adjust the op amp offset voltage until the ADC output code flickers between 0000 0000 0000 and 0000 0000 0001.

0 to +5V Range: 1/2LSB = 0.61mV
0 to +10V Range: 1/2LSB = 1.22mV

For zero full-scale error apply an analog input voltage equal to FS-3/2LSBs (last code transition) at V_{IN} and adjust R1 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.

0 to +5V Range: FS-3/2LSBs = 4.99817
0 to +10V Range: FS-3/2LSBs = 9.99634

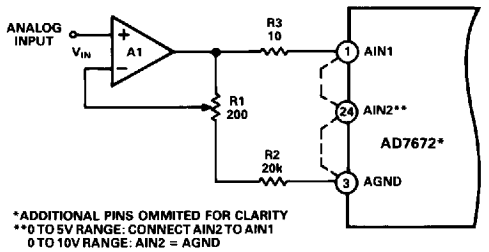
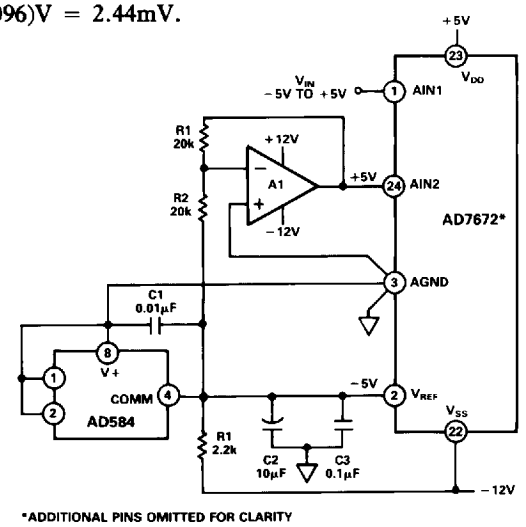


Figure 10. Unipolar Operation with Gain Error Adjust

BIPOLAR OPERATION

Bipolar operation is achieved by providing a +10V span at the AIN1 input which is offset to ±5V by applying +5V at the AIN2 input. This requires two reference voltages; −5V for the V_{REF} input and +5V for the AIN2 input. Figure 11 demonstrates how to produce these voltages from an AD584 and an inverting amplifier configuration. Alternatively, a convenient solution is to use the AD588 voltage reference as in Figure 12. This device generates the required ±5V with a minimum of additional components. It also offers excellent temperature stability with voltage drifts as low as 1.5ppm/°C.

The ideal input/output transfer characteristic after offset and gain adjustment is shown in Figure 13. The LSB size is (10/4096)V = 2.44mV.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 11. Bipolar Operation Using an AD584 and an AD711 Op Amp

BIPOLAR OFFSET AND GAIN ADJUSTMENT

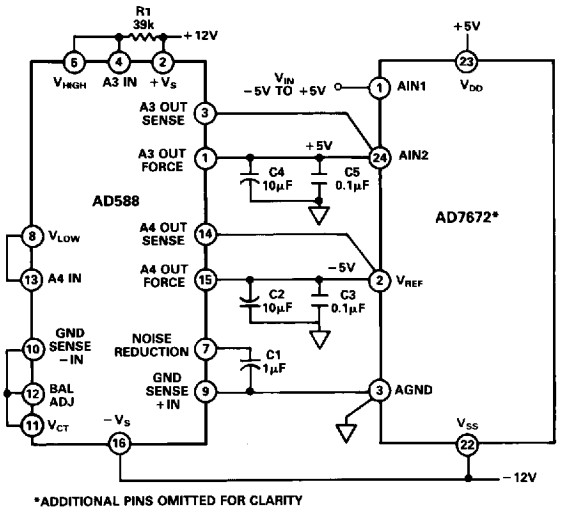
In applications where absolute accuracy is important then offset and gain error can be adjusted to zero. Offset is adjusted by trimming the voltage at the AIN1 or the AIN2 input when the analog input is at −FS/2 +1/2LSB. This can be achieved by adjusting the offset of an external amplifier used to drive either of these analog inputs. Alternatively the AD588 voltage reference contains a balance control input which can be used to trim the offset to zero. An additional potentiometer (R2 in Figure 14) is required. The trim procedure is as follows:

Apply −4.99878V (−FS/2 + 1/2LSB) at V_{IN} and adjust R2 until the ADC ouput code flickers between 0000 0000 0000 and 0000 0000 0001.

Gain error can be adjusted at either the last positive code transition or the mid-scale transition (bipolar zero error adjust). Adjusting the positive end of the transfer function is in keeping with more conventional ADC calibration techniques where the user fixes the two end points as in the unipolar case. Bipolar zero adjustment is required in some applications (e.g., motor control) where the user must be guaranteed that the 0111 1111 1111 to 1000 0000 0000 transition occurs exactly when the analog input is 1/2LSB below AGND. The trim procedures for both cases are as follows. (See Figure 14.)

Last Code Transition Adjust

Apply a voltage of 4.99634 volts (FS/2 − 3/2LSBs) at V_{IN}. Adjust R5 until the ADC output code flickers between 1111 1111 1110 and 1111 1111 1111.



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 12. Bipolar Operation Using an AD588 Voltage Reference

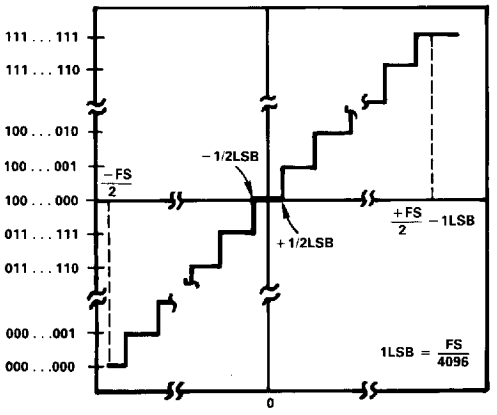
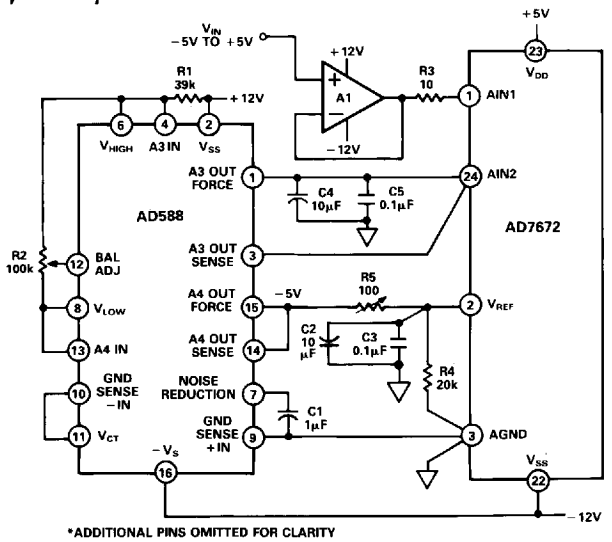


Figure 13. Ideal Input/Output Transfer Characteristic for Bipolar Operation



*ADDITIONAL PINS OMITTED FOR CLARITY

Figure 14. Bipolar Operation with Offset and Gain Error Adjust

Bipolar Zero Error Adjust

Apply a voltage of −1.22mV at V_{IN} and adjust R5 until the ADC output code flickers between 0111 1111 1111 and 1000 0000 0000.

TIMING AND CONTROL

Conversion start and data read operations are controlled by two of the AD7672 digital inputs; $\overline{CS}$ and $\overline{RD}$. Figure 15 shows the equivalent logic circuit of these inputs. A high-to-low logic transition on $\overline{CS}$ and $\overline{RD}$ initiates a conversion. Once initiated it cannot be restarted until conversion is complete. Converter status is indicated by the $\overline{BUSY}$ output, and this is low while conversion is in progress.

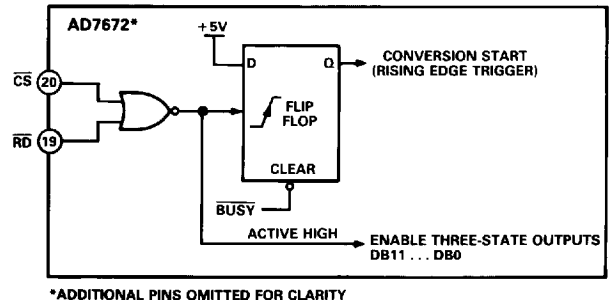


Figure 15. Internal Logic for Control Inputs $\overline{CS}$ and $\overline{RD}$

There are two modes of operation as outlined by the timing diagrams of Figures 16 and 17. Slow Memory Mode is designed for microprocessors that can be driven into a WAIT state, a READ operation brings $\overline{CS}$ and $\overline{RD}$ low, which initiates a conversion and data is read when conversion is complete. The second is the ROM Mode, which does not require microprocessor WAIT states. A READ operation brings $\overline{CS}$ and $\overline{RD}$ low which initiates a conversion and reads the previous conversion result. The data format for both modes is designed for parallel interfacing.

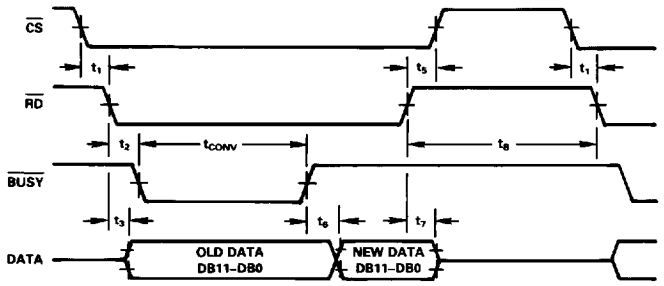


Figure 16. Slow Memory Mode Timing Diagram

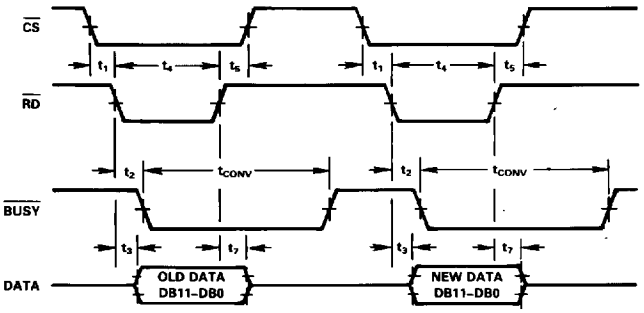


Figure 17. ROM Mode Timing Diagram

SLOW MEMORY MODE

Figure 16 shows the timing diagram for Slow Memory Mode. $\overline{CS}$ and $\overline{RD}$ going low triggers a conversion and the AD7672 acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{BUSY}$ returns high at the end of conversion when the output latches have been updated and the conversion result is placed on the output data bus.

ROM MODE

The ROM Mode avoids placing a microprocessor into a wait state. A conversion is started with a READ operation and the 12-bits of data from the previous conversion are available on the data outputs while $\overline{CS}$ and $\overline{RD}$ are low. This data may be disregarded if not required. A second READ operation reads the new data and starts another conversion. A delay at least as long as the AD7672 conversion time must be allowed between READ operations.

MICROPROCESSOR INTERFACING

The AD7672 is designed to interface to microprocessors as a memory mapped device. The $\overline{CS}$ and $\overline{RD}$ inputs are common control inputs to all peripheral memory interfacing.

MC68000 MICROPROCESSOR

Figure 18 shows a typical interface for the MC68000. The AD7672 is operating in the Slow Memory Mode. Assuming the AD7672 is located at address C000 then the following single 16-bit MOVE instruction both starts a conversion and reads the conversion result.

Move.W $C000,D0

At the beginning of the instruction cycle when the ADC address is selected, $\overline{BUSY}$ and $\overline{CS}$ assert $\overline{DTACK}$, so that the 68000 is forced into a WAIT state. At the end of conversion $\overline{BUSY}$ returns high and the conversion result is placed in the D0 register of the UP.

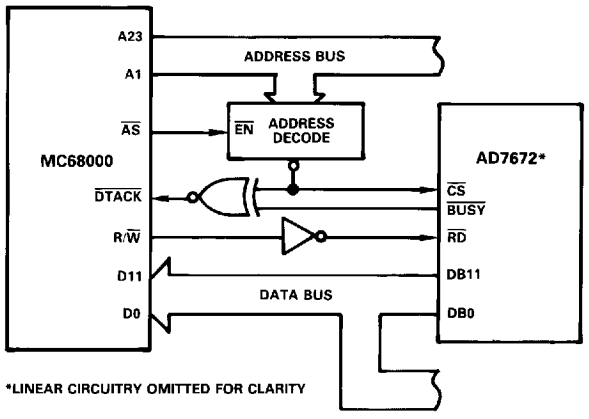


Figure 18. AD7672 –MC68000 Interface

8085A, Z-80 MICROPROCESSORS

Figure 19 shows an AD7672 interface for the Z-80 and 8085A. The AD7672 is operating in the Slow Memory Mode and a two byte read is required. Not shown in the Figure is the 8-bit latch required to demultiplex the 8085A common address/data bus. The following LOAD instruction starts a conversion and reads the conversion result into the HL register pair.

For the 8085A LHLD (B000)
For the Z-80 LDHL (B000)

This is a two byte read instruction. During the first read operation, $\overline{BUSY}$ forces the microprocessor to wait for the AD7672 conversion. At the end of conversion the low byte (DB7-DB0) is loaded into the HL register pair and the high byte (DB11-DB8) is latched into a 74HC374. No WAIT states are inserted during the second read operation when the microprocessor is reading the high data byte.

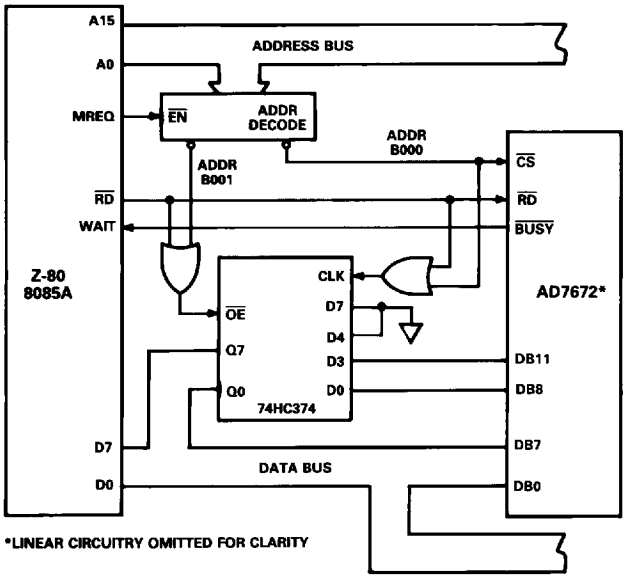


Figure 19. AD7672 – 8085A/Z80 Interface

IBM PC* COMPUTER

The −12V power supply operation of the AD7672 makes it an ideal choice for the IBM PC. A typical interface is shown in Figure 20. The AD7672 is configured in the ROM mode. Two addresses are required to read the 12-bit ADC data over the 8-bit data bus. An I/O read instruction to the ADC address (B000) starts a conversion and reads the low data byte (DB7-DB0). This data is from the previous conversion. The high byte (DB11-DB8) may be read with a similar I/O instruction to the 74HC374 latch (address B001). Alternatively the up-to-date data may be read at the end of conversion. The AD7672 $\overline{BUSY}$ may be used to interrupt the IBM PC as shown in Figure 20. The data is then read with two I/O instructions as before. Note a read instruction to the ADC should not be attempted while conversion is in progress.

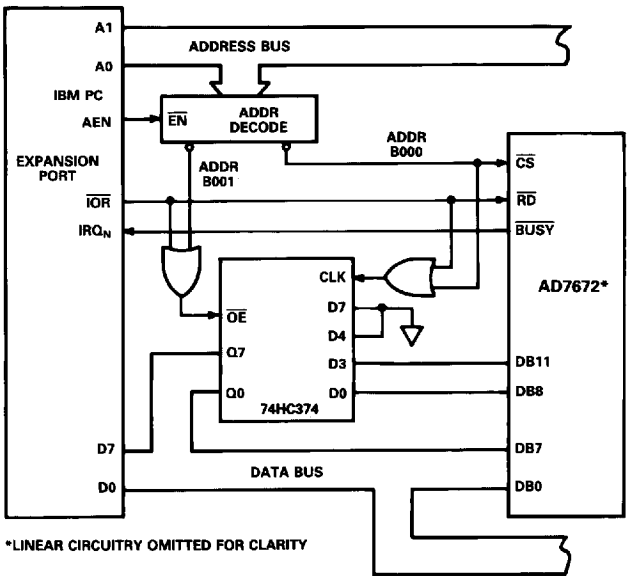


Figure 20. AD7672 – IBM PC Interface

ADSP-2100 DIGITAL SIGNAL PROCESSOR

The ADSP-2100 like other digital signal processors requires very fast data access times beyond the capabilities of the AD7672. This problem is easily overcome by inserting 74HC374 latches in the data bus as in Figure 21. Again for this interface a single instruction is sufficient to read the AD7672 conversion result.

MRO = DM (ADC ADDRESS)

This instruction initiates a conversion and reads the previous conversion result into the MRO register. $\overline{CS}$ and $\overline{RD}$ are gated so that they remain low for the duration of the conversion. Note that no WAIT states are inserted even though the AD7672 is configured for a Slow Memory mode. At the end of conversion, $\overline{BUSY}$ going high latches the new result into the 74HC374 latches. An RC delay is inserted to compensate for the data setup time after $\overline{BUSY}$ (t_6).

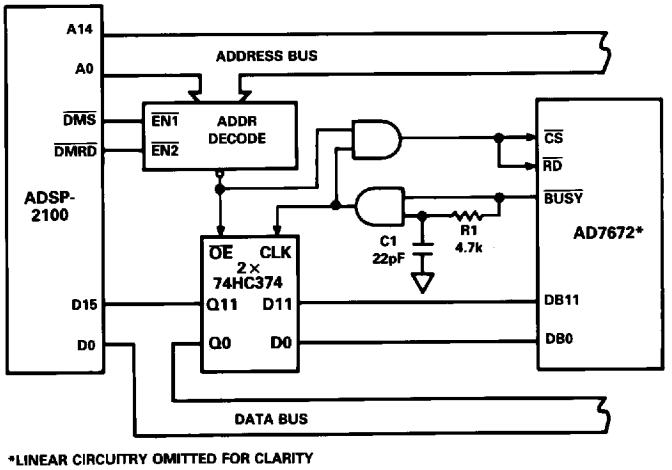


Figure 21. AD7672 – ADSP-2100 Interface

*IBM PC is a trademark of International Business Machines Corp.

TMS32010 MICROCOMPUTER

Figure 22 shows an AD7672-TMS32010 interface. The AD7672 is operating in the ROM mode. The interface is designed for a maximum TMS32010 clock frequency of 18MHz but will typically work over the full TMS32010 clock frequency range.

The AD7672 is mapped at a port address. The following I/O instruction starts a conversion and reads the previous conversion result into data memory.

IN A,PA (PA = PORT ADDRESS)

When conversion is complete, a second I/O instruction reads the up-to-date data into the accumulator and starts another conversion. A delay at least as long as the ADC conversion time must be allowed between I/O instructions.

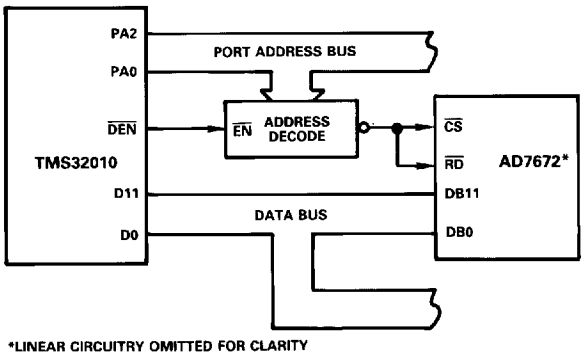


Figure 22. AD7672 – TMS32010 Interface

APPLICATION HINTS

Good printed circuit board (PCB) layout is as important as the circuit design itself in achieving high speed A/D performance. For 12-bit performance the AD7672's comparator is required to make bit decisions to an accuracy of 0.61mV. To achieve this, the designer has to be conscious of noise both in the ADC itself and the preceding analog circuitry. Switching mode power supplies are not recommended as the switching spikes will feed through to the comparator causing noisy code transitions. Other causes of concern are ground loops and digital feedthrough from microprocessors. These are factors which influence any ADC, and a proper PCB layout which minimizes these effects is essential for best performance.

LAYOUT HINTS

Ensure that the layout for the printed circuit board has the digital and analog signal lines separated as much as possible. Take care not to run any digital track alongside an analog signal track. Guard (screen) the analog input with AGND.

Establish a single point analog ground (star ground) separate from the logic system ground at Pin 3 (AGND) or as close as possible to the AD7672 as shown in Figure 23. Connect all other grounds and Pin 12 (AD7672 DGND) to this single analog ground point. Do not connect any other digital grounds to this analog ground point. Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC, so make the foil width for these tracks as wide as possible. The use of ground planes minimizes impedance paths, while guarding the analog circuitry from digital noise. The

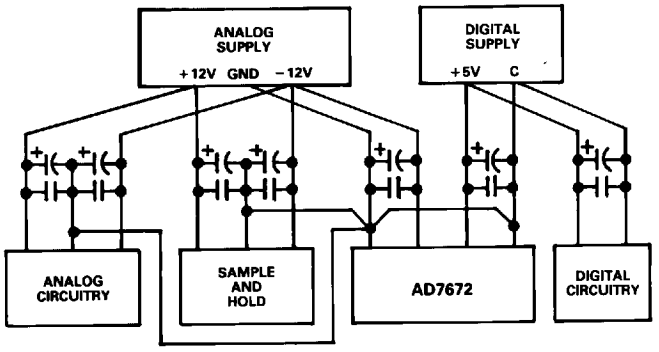


Figure 23. Power Supply Grounding Practice

circuit layout of Figures 29 and 30 have both analog and digital ground planes which are kept separated and only joined together at the AD7672 AGND pin.

NOISE: Keep the input signal leads to AIN and signal return leads from AGND (Pin3) as short as possible to minimize input noise coupling. In applications where this is not possible use a shielded cable between the source and the ADC. Reduce the ground circuit impedance as much as possible, since any potential difference in grounds between the signal source and the ADC appears as an error voltage in series with the input signal.

Microprocessor applications generate noisy environments, making 12-bit performance difficult to achieve, especially when the ADC is connected to a continously active bus. The problem can be eliminated by forcing the microprocessor into a WAIT state during conversion (see Slow Memory Mode interfacing), or by using three-state buffers to isolate the AD7672 data bus.

DATA ACQUISITION APPLICATION

Figure 24 shows a typical data acquisition circuit designed for a microprocessor environment. The corresponding PCB layout and silk screen are shown in Figures 28 to 30. The analog input is applied to a Sample-and-Hold Amplifier (SHA) which can either be an AD683, an AD681 or an AD585. (See Figures 25 and 26.) A voltage reference (AD588) provides the appropriate biasing for any of the three analog input ranges. The data bus outputs are buffered with 74HC374 latches. These provide data bus isolation and improve data access time. Data access time is reduced to under 30ns allowing interfacing to practically any microprocessor including the high-speed DSP processors. Data format can either be a complete parallel load for 16-bit microprocessors or a two byte load for 8-bit microprocesssors.

Bus activity on the AD7672 $\overline{CS}$ and $\overline{RD}$ inputs during conversion can feedthrough to the comparator and cause LSB errors. Ideally these signals should be inactive during conversion. One way of achieving this is to force them into an inactive state by gating them with $\overline{BUSY}$ as shown in Figure 24. R2 and C26 are included to provide a delay of approximately 100ns. This compensates for the data setup time after $\overline{BUSY}$ goes high ensuring valid data gets loaded into IC5 and IC6.

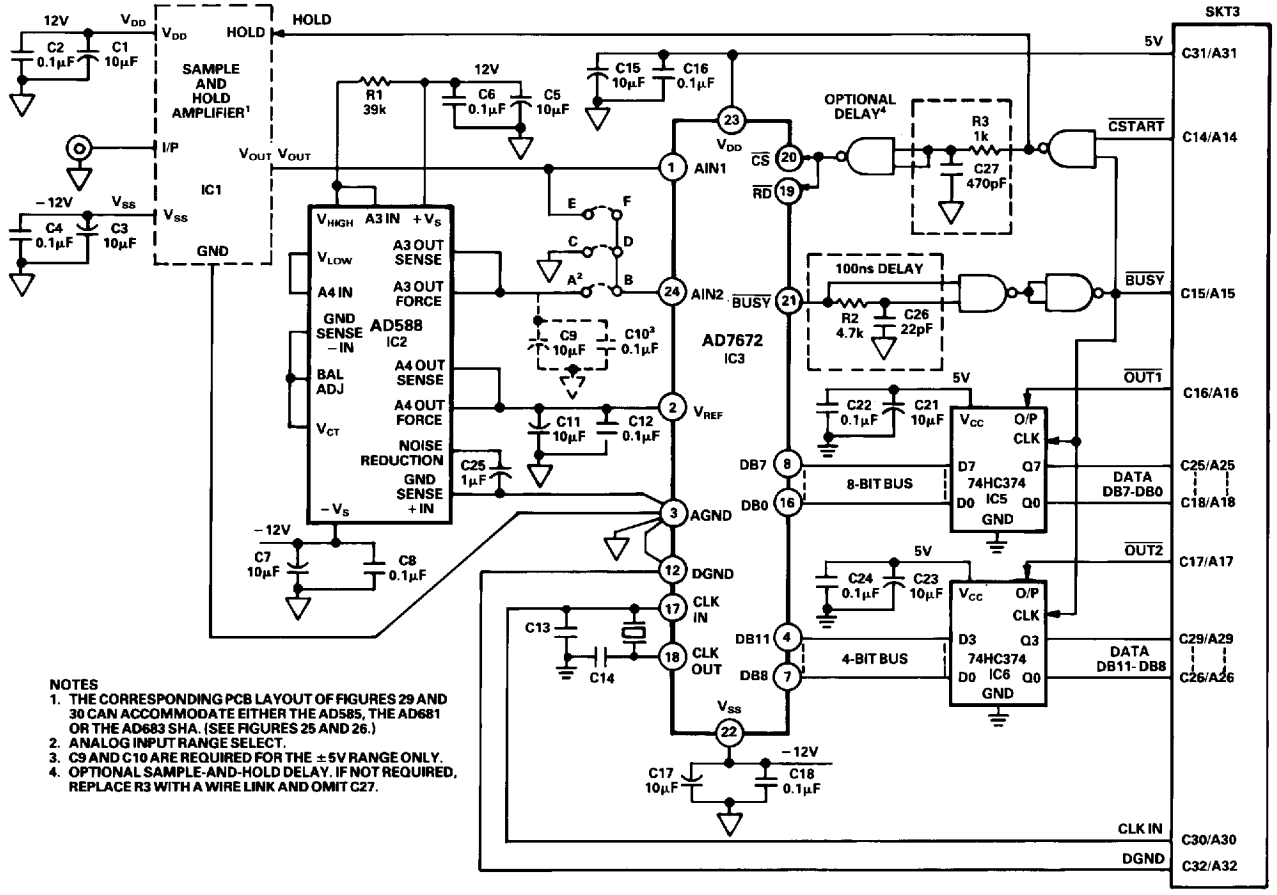


Figure 24. Data Acquisition Circuit Using the AD7672

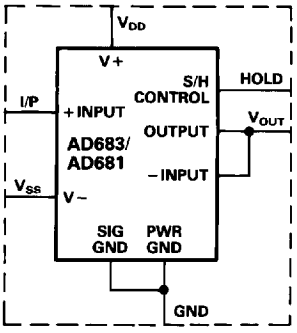


Figure 25. AD683/AD681 SHA Connection Diagram for Figure 24

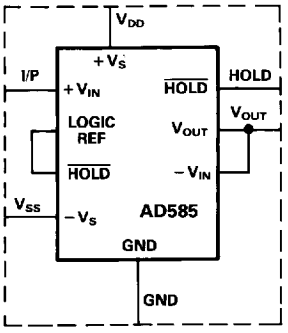


Figure 26. AD585 SHA Connection Diagram for Figure 24

SAMPLE-AND-HOLD OPERATION

The PCB layout of Figures 29 and 30 can accommodate either the AD683, the AD681 or the AD585 sample-and-hold amplifier. The choice of SHA depends mainly on the acquisition time required.

However, another important consideration with sample-and-hold interfacing is settling time. This is the time required by the sample and hold amplifier output to settle after receiving a HOLD command. To allow for this, there must be a delay which is at least as long as the SHA settling time between the HOLD command and the AD7672's first MSB decision. When initiating a conversion, if the SHA's HOLD input and the AD7672 $\overline{CS}$ and $\overline{RD}$ inputs are asserted together, then this delay can vary from one to two clock periods. This corresponds to a delay of 800ns to 1600ns for the AD7672XX10, 400ns to 800ns for the AD7672XX05 and 250ns to 500ns for the AD7672XX03. Under these conditions a settling time of less than 200ns is required by the SHA to satisfy all speed grades of the AD7672. This figure allows an additional 50ns for the AD7672XX03 internal comparator. Both the AD683 and AD681 meet this condition. However, since the AD585 is specified with a settling time of 500ns, the 10μs version of the AD7672 is the only one of the three-speed grades guaranteed to meet this timing requirement. This settling time requirement may be met with the higher speed grades by using either an additional circuit delay or by synchronizing the control inputs with the clock. Both of these methods are discussed below.

AD7672 – AD585 INTERFACE

The 500ns settling time requirement of the AD585 must be allowed for, at the start of conversion when interfacing to the 3μs and 5μs versions of the AD7672. It may be achieved for the 5μs version by using either one of two methods. The first is to synchronize the control inputs with the ADC clock as follows; when initiating a conversion $\overline{CS}$ and $\overline{RD}$ ($\overline{CSTART}$ in Figure 24) should go low on a falling CLK IN edge. This guarantees two clock periods between conversion start and the first MSB decision.

The second method will work for both the 3μs and 5μs parts. It compensates for settling time by inserting an external delay between the AD7672 $\overline{CS}$ and $\overline{RD}$ inputs and the AD585 HOLD input. The length of this delay should be equal to the sample-and-hold amplifier settling time. It is shown as an optional RC delay in Figure 24 which must be bypassed if not used. Note it is not required for the slower 10μs, AD7672XX10 or when either the AD683 or the AD681 is used with any speed grade of the AD7672.

INPUT RANGE SELECT OPTIONS

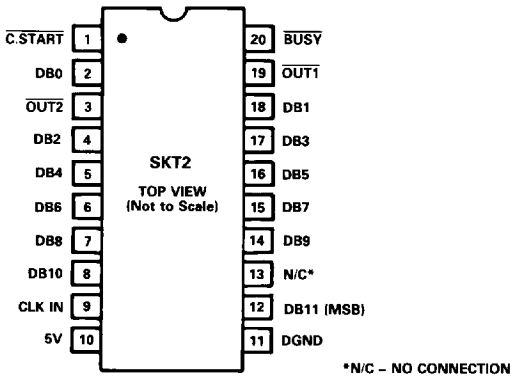
There are three analog input ranges which are user selectable by placing links on the PCB as shown in Table I below. These options are located between IC2 and IC3.

EXTERNAL CONNECTIONS

The PCB layout is designed so that all external connections except the V_{DD} and V_{SS} power supplies can be made by any of three ways:

1. 32 way single sided edge connector,
2. Euro card connector, SKT3
3. 20-pin DIP socket. (SKT2 on the silk screen).

The pinout for the 20-pin DIP socket is shown below and the other pinouts are shown in Figures 24 and 30. The V_{DD} and V_{SS} power supplies are connected at the top of the board (see Figure 28, Silk Screen).



PIN FUNCTION DESCRIPTION

$\overline{C.START}$	Conversion Start going low initiates a conversion.
$\overline{OUT1}$	Active Low, three-state control for DB7-DB0.
$\overline{OUT2}$	Active Low, three-state control for DB11-DB8.
$\overline{BUSY}$	AD7672 Status Output. $\overline{BUSY}$ is low during conversion.
CLK IN	AD7672 CLK IN input. Note the board has a facility for an on-board crystal oscillator or a ceramic resonator.
DB11-DB0	Three-State data outputs.
5V	5V power supply.
DGND	Digital Ground

Table I. Input Range Link Options

Range (Volts)	Links Required	
0 to 5	Connect E to F	: A–B, C–D = Open Circuit
0 to 10*	Connect C to D	: A–B, E–F = Open Circuit
−5 to +5	Connect A to B	: C–D, E–F = Open Circuit

*Due to headroom limitations at 12V power supplies, the AD585 sample-and-hold amplifier is not suitable for the 0-10V range.

COMPONENT LIST

IC1	Sample and hold, IC1 can occupy one of two positions depending on the sample-and-hold model. These positions are outlined in Figure 27. The plated-through holes denoted by "1" are configured for the AD683/AD681 and the plated-through holes denoted by "2" are configured for the AD585.

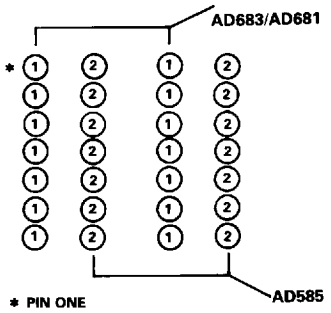


Figure 27. PCB Sample-and-Hold Amplifier Options

IC2	AD588 Voltage Reference.
IC3	AD7672 Analog-to-Digital Converter.
IC4	74HC00 Quad NAND Gate.
IC5, IC6	74HC374 Ocatal Latches with Three-State Outputs.
C1, C3, C5, C7, C11, C15, C17, C19, C21, C23	10μF Capacitors.
C2, C4, C6, C8, C12, C16, C18, C20, C22, C24	0.1μF Capacitors.
C25	1μF
C9	10μF Capacitor, Required for ±5V Range Only.
C10	0.1μF Capacitor, Required for ±5V Range Only.
C13, C14	Crystal/Ceramic Resonator Capacitors Values Depend on the Manufacturer. For example: 4MHz XTAL (HC – 18/U) from IQD; C13, C14 = 30pF; 2.5MHz (HC 18/U) and 1.2288MHz (HC 33/U) from Anderson; No Capacitors Required.
C26	22pF.
C27	470pF, Sample-and-Hold Delay (See Sample-and-Hold Operation) Omit C27 if this delay is not required.
R1	39k.
R2	4.7k.
R3	1k, Sample-and-Hold Delay (See Sample-and-Hold Operation) Replace with a wire link if this delay is not required.
SKT1	Subminiature Connector from Greenpar.

TEST POINTS

TP1 – Analog Input
TP2 – Analog Ground
TP3 – CLK IN
TP4 – AD7672 $\overline{BUSY}$ Output

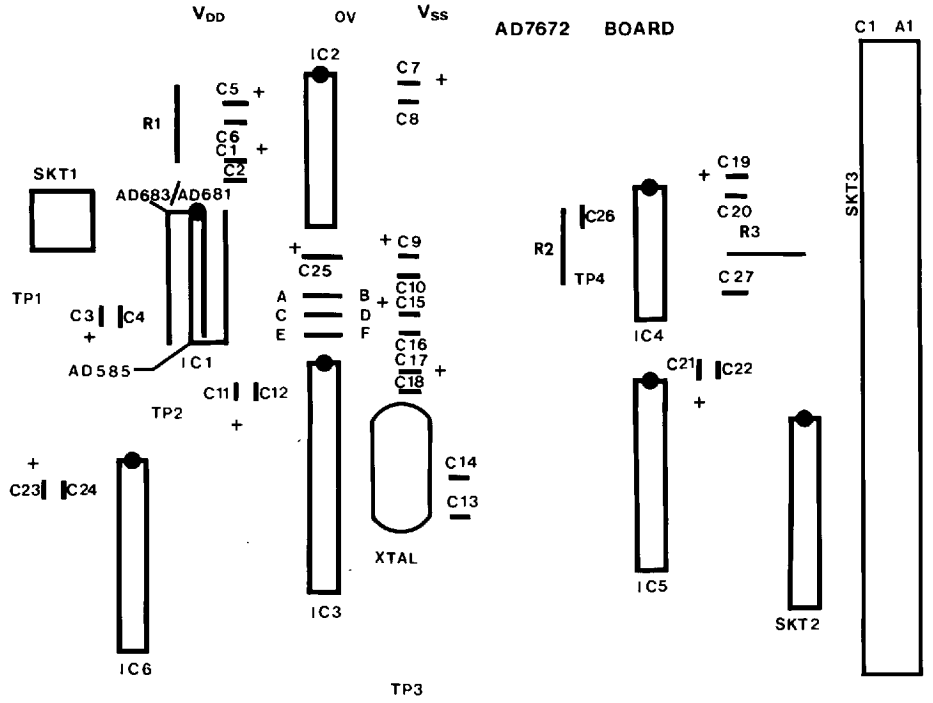


Figure 28. PCB Silk Screen for Figure 24

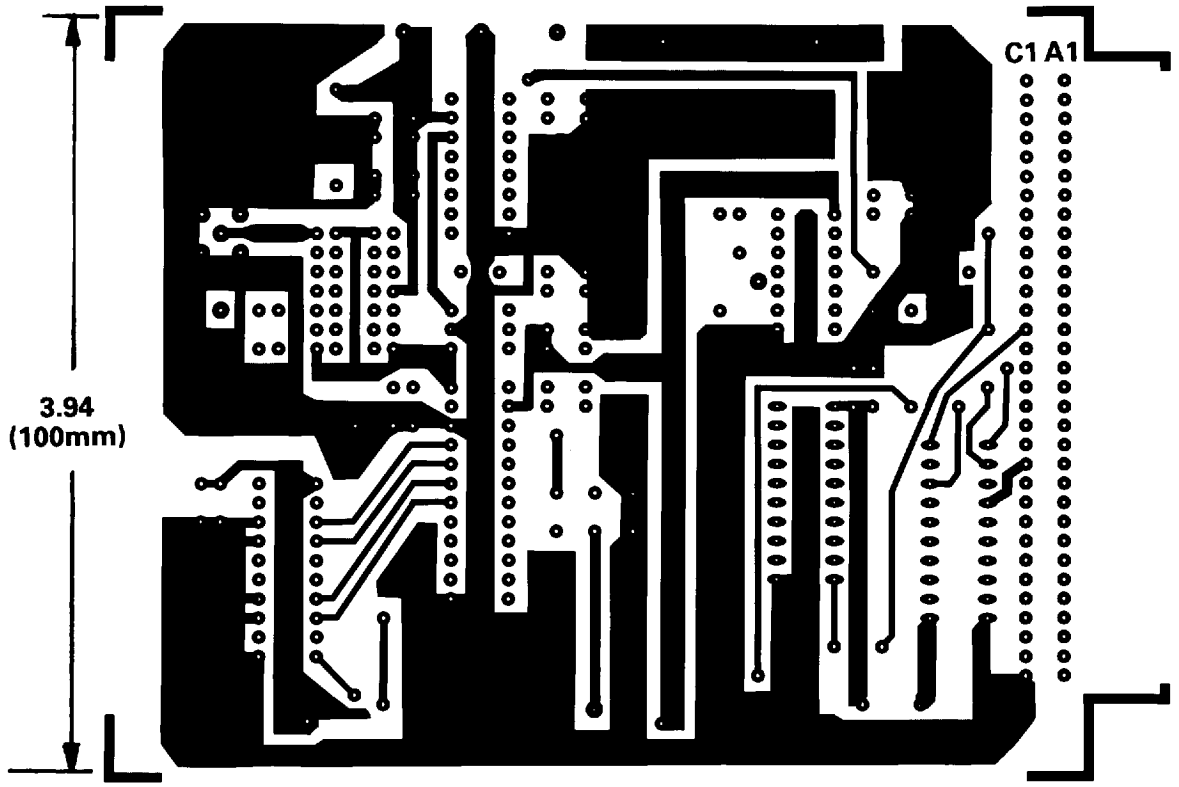


Figure 29. PCB Component Side Layout for Figure 24

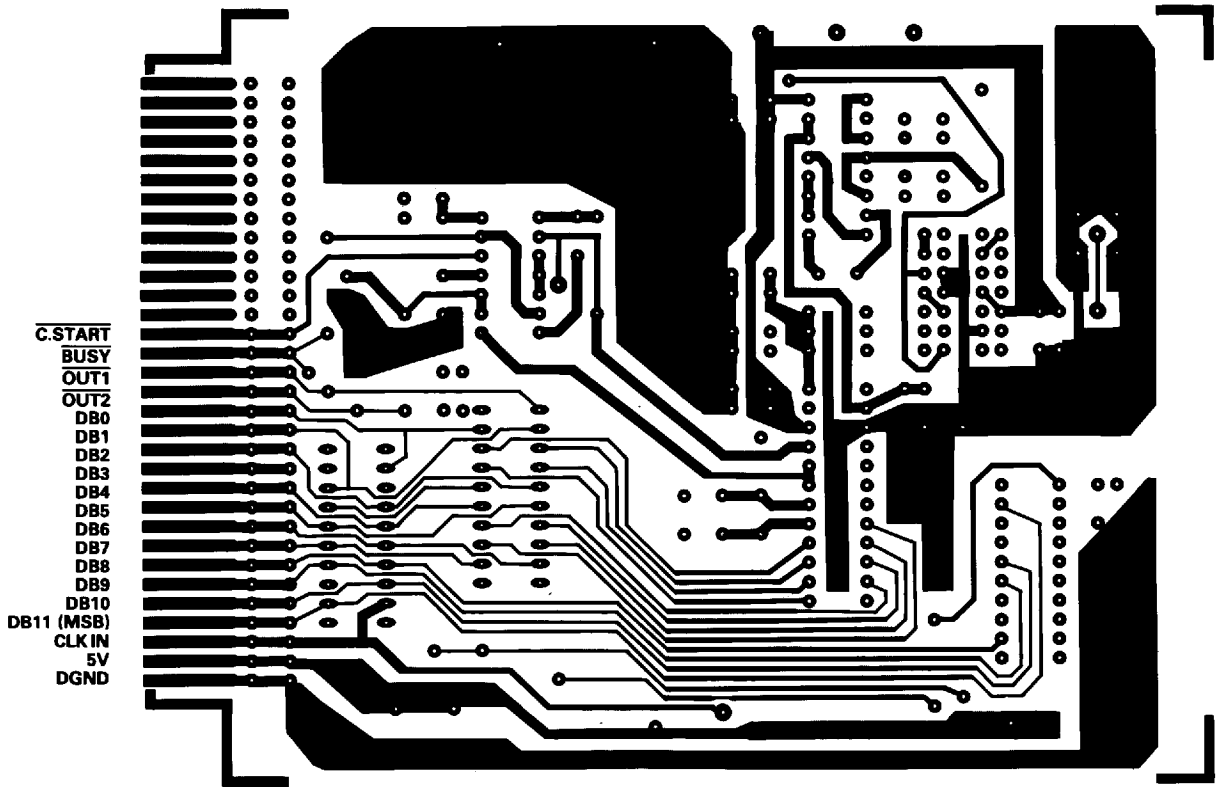
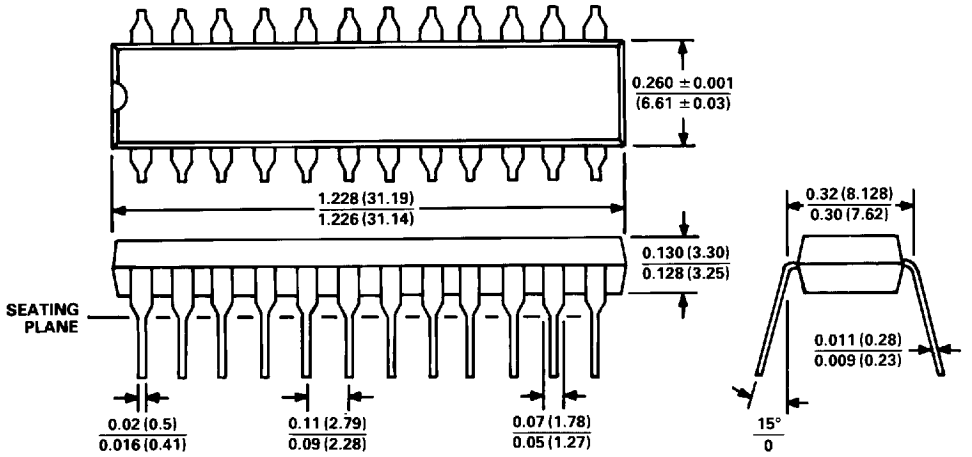


Figure 30. PCB Solder Side Layout for Figure 24

OUTLINE DIMENSIONS

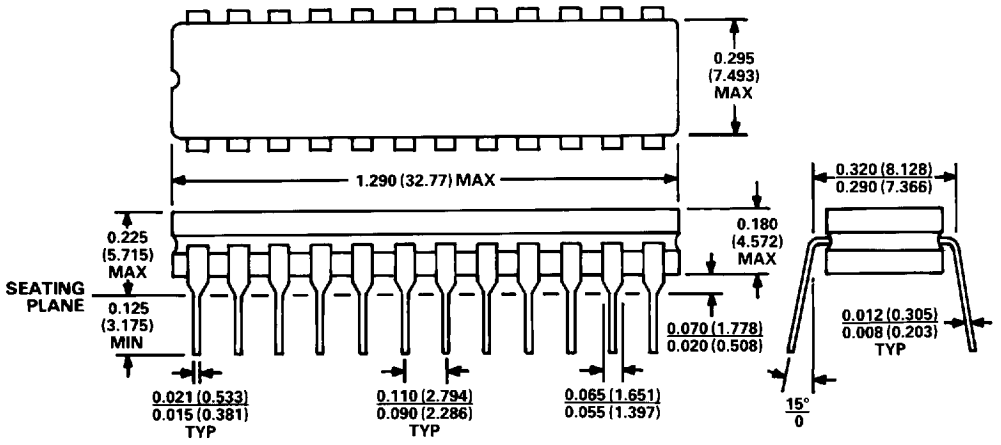
Dimensions shown in inches and (mm).

24-Pin Plastic DIP (N-24)



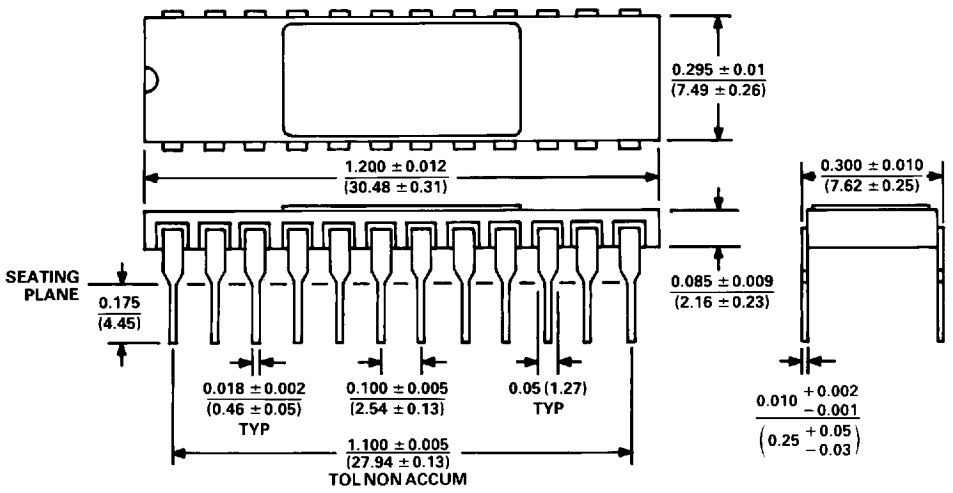
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. PLASTIC LEADS WILL BE EITHER SOLDER DIPPED OR TIN/LEAD PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Pin Cerdip (Q-24)



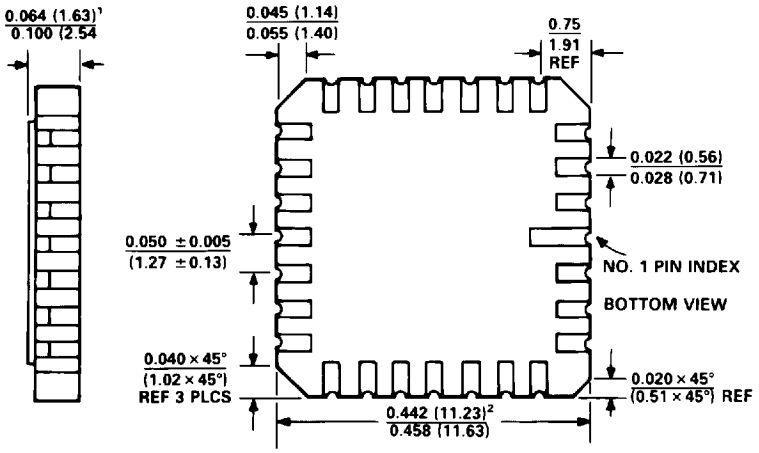
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERDIP LEADS WILL BE EITHER TIN PLATED OR SOLDER DIPPED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

24-Pin Ceramic DIP (D-24A)



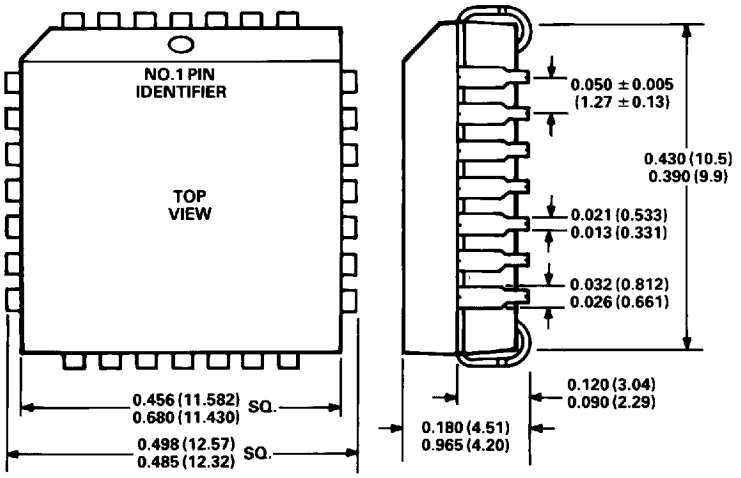
NOTES
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.
3. METAL LID IS CONNECTED TO DGND

28-Terminal Leadless Ceramic Chip Carrier (E-28A)



NOTES
1. THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2. APPLIES TO ALL FOUR SIDES.
3. ALL TERMINALS ARE GOLD PLATED.

28-Terminal Plastic Leaded Chip Carrier
(P-28A)



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