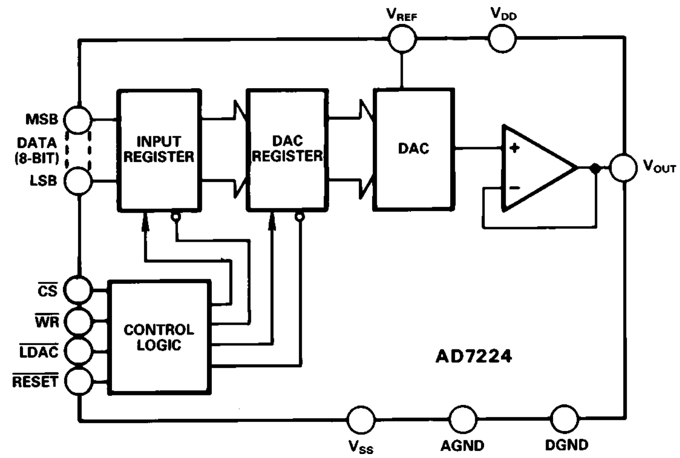
ANALOG DEVICES

LC²MOS 8-Bit DAC with Output Amplifiers

AD7224

FEATURES
8-Bit CMOS DAC with Output Amplifiers
Operates with Single or Dual Supplies
Low Total Unadjusted Error:
Less Than 1 LSB Over Temperature
Extended Temperature Range Operation
μP-Compatible with Double Buffered Inputs
Standard 18-Pin DIPs, and 20-Terminal Surface Mount Package and SOIC Package

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7224 is a precision 8-bit voltage-output, digital-to-analog converter, with output amplifier and double buffered interface logic on a monolithic CMOS chip. No external trims are required to achieve full specified performance for the part.

The double buffered interface logic consists of two 8-bit registers–an input register and a DAC register. Only the data held in the DAC registers determines the analog output of the converter. The double buffering allows simultaneous update in a system containing multiple AD7224s. Both registers may be made transparent under control of three external lines, $\overline{CS}$, $\overline{WR}$ and $\overline{LDAC}$. With both registers transparent, the $\overline{RESET}$ line functions like a zero override; a useful function for system calibration cycles. All logic inputs are TTL and CMOS (5 V) level compatible and the control logic is speed compatible with most 8-bit microprocessors.

Specified performance is guaranteed for input reference voltages from +2 V to +12.5 V when using dual supplies. The part is also specified for single supply operation using a reference of +10 V. The output amplifier is capable of developing +10 V across a 2 kΩ load.

The AD7224 is fabricated in an all ion-implanted high speed Linear Compatible CMOS (LC²MOS) process which has been specifically developed to allow high speed digital logic circuits and precision analog circuits to be integrated on the same chip.

PRODUCT HIGHLIGHTS

1. DAC and Amplifier on CMOS Chip
   The single-chip design of the 8-bit DAC and output amplifier is inherently more reliable than multi-chip designs. CMOS fabrication means low power consumption (35 mW typical with single supply).
2. Low Total Unadjusted Error
   The fabrication of the AD7224 on Analog Devices Linear Compatible CMOS (LC²MOS) process coupled with a novel DAC switch-pair arrangement, enables an excellent total unadjusted error of less than 1 LSB over the full operating temperature range.
3. Single or Dual Supply Operation
   The voltage-mode configuration of the AD7224 allows operation from a single power supply rail. The part can also be operated with dual supplies giving enhanced performance for some parameters.
4. Versatile Interface Logic
   The high speed logic allows direct interfacing to most microprocessors. Additionally, the double buffered interface enables simultaneous update of the AD7224 in multiple DAC systems. The part also features a zero override function.

REV. B

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AD7224–SPECIFICATIONS

DUAL SUPPLY

(V_{DD} = 11.4 V to 16.5 V, V_{SS} = –5 V ± 10%; AGND = DGND = 0 V; V_{REF} = +2 V to (V_{DD} – 4 V)[1] unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	**K, B, T Versions**[2]	**L, C, U Versions**[2]	**Units**	**Conditions/Comments**
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±1	LSB max	V_{DD} = +15 V ± 5%, V_{REF} = +10 V
Relative Accuracy	±1	±1/2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
Full-Scale Error	±3/2	±1	LSB max	
Full-Scale Temperature Coefficient	±20	±20	ppm/°C max	V_{DD} = 14 V to 16.5 V, V_{REF} = +10 V

SINGLE SUPPLY (V_{DD} = +15 V ± 5%; V_{SS} = AGND = DGND = 0 V; V_{REF} = +10 V[1] unless otherwise noted. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

Parameter	K, B, T Versions[2]	L, C, U Versions[2]	Units	Conditions/Comments
STATIC PERFORMANCE				
Resolution	8	8	Bits	
Total Unadjusted Error	±2	±2	LSB max	
Differential Nonlinearity	±1	±1	LSB max	Guaranteed Monotonic
REFERENCE INPUT				
Input Resistance	8	8	kΩ min	
Input Capacitance[3]	100	100	pF max	Occurs when DAC is loaded with all 1s.
DIGITAL INPUTS				
Input High Voltage, V_{INH}	2.4	2.4	V min	
Input Low Voltage, V_{INL}	0.8	0.8	V max	
Input Leakage Current	±1	±1	µA max	V_{IN} = 0 V or V_{DD}
Input Capacitance[3]	8	8	pF max	
Input Coding	Binary	Binary		
DYNAMIC PERFORMANCE				
Voltage Output Slew Rate[4]	2	2	V/µs min	
Voltage Output Settling Time[4]				
Positive Full-Scale Change	5	5	µs max	Settling Time to ±1/2 LSB
Negative Full-Scale Change	20	20	µs max	Settling Time to ±1/2 LSB
Digital Feedthrough[3]	50	50	nV secs typ	V_{REF} = 0 V
Minimum Load Resistance	2	2	kΩ min	V_{OUT} = +10 V
POWER SUPPLIES				
V_{DD} Range	14.25/15.75	14.25/15.75	V min/V max	For Specified Performance
I_{DD}				
@ 25°C	4	4	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
T_{MIN} to T_{MAX}	6	6	mA max	Outputs Unloaded; V_{IN} = V_{INL} or V_{INH}
SWITCHING CHARACTERISTICS[3, 4]				
t_1				
@ 25°C	90	90	ns min	Chip Select/Load DAC Pulse Width
T_{MIN} to T_{MAX}	90	90	ns min	
t_2				
@ 25°C	90	90	ns min	Write/Reset Pulse Width
T_{MIN} to T_{MAX}	90	90	ns min	
t_3				
@ 25°C	0	0	ns min	Chip Select/Load DAC to Write Setup Time
T_{MIN} to T_{MAX}	0	0	ns min	
t_4				
@ 25°C	0	0	ns min	Chip Select/Load DAC to Write Hold Time
T_{MIN} to T_{MAX}	0	0	ns min	
t_5				
@ 25°C	90	90	ns min	Data Valid to Write Setup Time
T_{MIN} to T_{MAX}	90	90	ns min	
t_6				
@ 25°C	10	10	ns min	Data Valid to Write Hold Time
T_{MIN} to T_{MAX}	10	10	ns min	

NOTES
[1]Maximum possible reference voltage.
[2]Temperature ranges are as follows:
AD7224KN, LN: 0°C to +70°C
AD7224BQ, CQ: –25°C to +85°C
AD7224TD, UD: –55°C to +125°C
[3]See Terminology.
[4]Sample tested at 25°C by Product Assurance to ensure compliance.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

V_{DD} to AGND . . . . –0.3 V, +17 V
V_{DD} to DGND . . . . –0.3 V, +17 V
V_{DD} to V_{SS} . . . . –0.3 V, +24 V
AGND to DGND . . . . –0.3 V, V_{DD}
Digital Input Voltage to DGND . . . . –0.3 V, V_{DD} + 0.3 V
V_{REF} to AGND . . . . –0.3 V, V_{DD} + 0.3 V
V_{OUT} to AGND[2] . . . . V_{SS}, V_{DD}
Power Dissipation (Any Package) to +75°C . . . . 450 mW
  Derates above 75°C by . . . . 6 mW/°C
Operating Temperature
  Commercial (K, L Versions) . . . . –40°C to +85°C
  Industrial (B, C Versions) . . . . –40°C to +85°C
  Extended (T, U Versions) . . . . –55°C to +125°C
Storage Temperature . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 secs) . . . . +300°C

NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typically short circuit current to AGND is 60 mA.

ORDERING GUIDE

Model[1]	Temperature Range	Total Unadjusted Error (LSB)	Package Option[2]
AD7224KN	–40°C to +85°C	±2 max	N-18
AD7224LN	–40°C to +85°C	±1 max	N-18
AD7224KP	–40°C to +85°C	±2 max	P-20A
AD7224LP	–40°C to +85°C	±1 max	P-20A
AD7224KR-1	–40°C to +85°C	±2 max	R-20
AD7224LR-1	–40°C to +85°C	±1 max	R-20
AD7224KR-18	–40°C to +85°C	±2 max	R-18
AD7224LR-18	–40°C to +85°C	±1 max	R-18
AD7224BQ	–40°C to +85°C	±2 max	Q-18
AD7224CQ	–40°C to +85°C	±1 max	Q-18
AD7224TQ	–55°C to +125°C	±2 max	Q-18
AD7224UQ	–55°C to +125°C	±1 max	Q-18
AD7224TE	–55°C to +125°C	±2 max	E-20A
AD7224UE	–55°C to +125°C	±1 max	E-20A

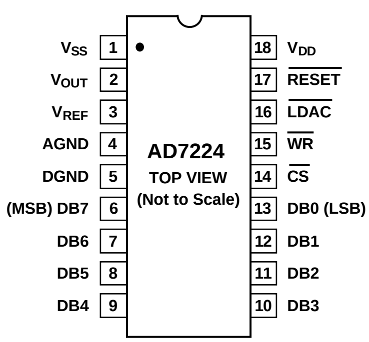
NOTES
[1]To order MIL-STD-883 processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[2]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

CAUTION

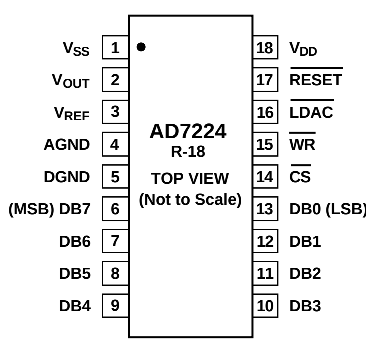
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7224 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

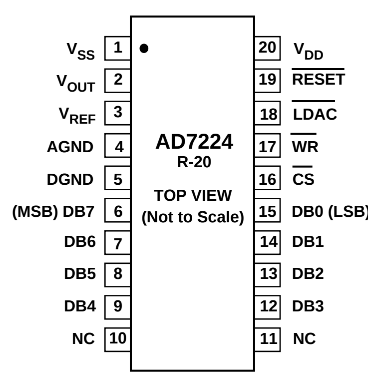
DIP and SOIC



(SOIC)

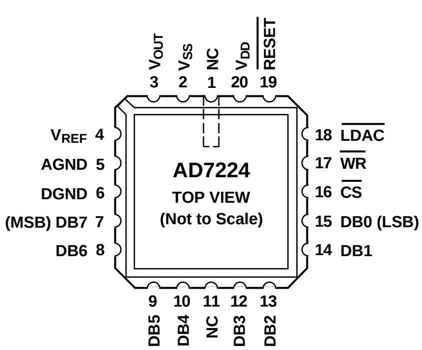


(SOIC)



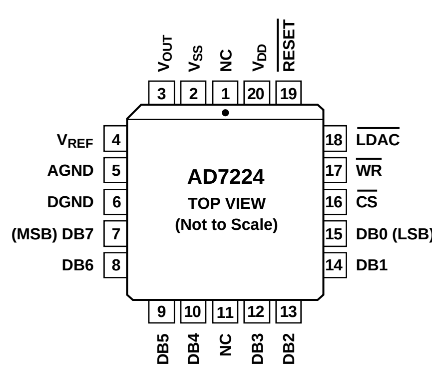
NC = NO CONNECT

LCCC



NC = NO CONNECT

PLCC



NC = NO CONNECT

$$V_{OUT} = D \bullet V_{REF}$$

where *D* is a fractional representation of the digital input code and can vary from 0 to 255/256.

OP-AMP SECTION

The voltage-mode D/A converter output is buffered by a unity gain noninverting CMOS amplifier. This buffer amplifier is capable of developing +10 V across a 2 kΩ load and can drive capacitive loads of 3300 pF.

The AD7224 can be operated single or dual supply resulting in different performance in some parameters from the output amplifier. In single supply operation (V_{SS} = 0 V = AGND) the sink capability of the amplifier, which is normally 400 μA, is reduced as the output voltage nears AGND. The full sink capability of 400 μA is maintained over the full output voltage range by tying V_{SS} to –5 V. This is indicated in Figure 2.

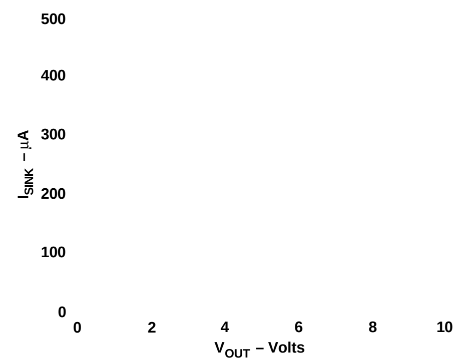


Table I. AD7224 Truth Table

$\overline{RESET}$	$\overline{LDAC}$	$\overline{WR}$	$\overline{CS}$	Function
H	L	L	L	Both Registers are Transparent
H	X	H	X	Both Registers are Latched
H	H	X	H	Both Registers are Latched
H	H	L	L	Input Register Transparent
H	H	↑	L	Input Register Latched
H	L	L	H	DAC Register Transparent
H	L	↑	H	DAC Register Latched
L	X	X	X	Both Registers Loaded With All Zeros
↑	H	H	H	Both Register Latched With All Zeros and Output Remains at Zero
↑	L	L	L	Both Registers are Transparent and Output Follows Input Data

H = High State, L = Low State, X = Don't Care.
All control inputs are level triggered.

The contents of both registers are reset by a low level on the $\overline{RESET}$ line. With both registers transparent, the $\overline{RESET}$ line functions like a zero override with the output brought to 0 V for the duration of the $\overline{RESET}$ pulse. If both registers are latched, a "LOW" pulse on $\overline{RESET}$ will latch all 0s into the registers and the output remains at 0 V after the $\overline{RESET}$ line has returned "HIGH". The $\overline{RESET}$ line can be used to ensure power-up to 0 V on the AD7224 output and is also useful, when used as a zero override, in system calibration cycles. Figure 3 shows the input control logic for the AD7224.

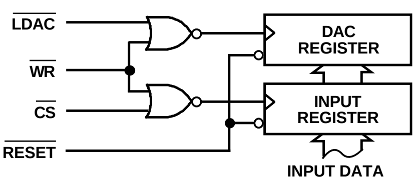
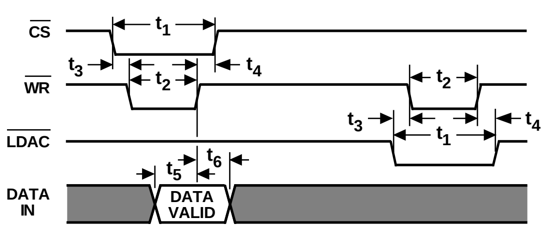


Figure 3. Input Control Logic



NOTES:
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD}. $t_r = t_f$ = 20ns OVER V_{DD} RANGE
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{INH} + V_{INL}}{2}$

Figure 4. Write Cycle Timing Diagram

SPECIFICATION RANGES

For the DAC to maintain specified accuracy, the reference voltage must be at least 4 V below the V_{DD} power supply voltage. This voltage differential is required for correct generation of bias voltages for the DAC switches.

With dual supply operation, the AD7224 has an extended V_{DD} range from +12 V ± 5% to +15 V ± 10% (i.e., from +11.4 V to +16.5 V). Operation is also specified for a single V_{DD} power supply of +15 V ± 5%.

Performance is specified over a wide range of reference voltages from 2 V to (V_{DD} – 4 V) with dual supplies. This allows a range of standard reference generators to be used such as the AD580, a +2.5 V bandgap reference and the AD584, a precision +10 V reference. Note that in order to achieve an output voltage range of 0 V to +10 V, a nominal +15 V ± 5% power supply voltage is required by the AD7224.

GROUND MANAGEMENT

AC or transient voltages between AGND and DGND can cause noise at the analog output. This is especially true in microprocessor systems where digital noise is prevalent. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7224. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7224 AGND and DGND pins (IN914 or equivalent).

Applying the AD7224

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7224, with the output voltage having the same positive polarity as V_{REF}. The AD7224 can be operated single supply (V_{SS} = AGND) or with positive/negative supplies (see op-amp section which outlines the advantages of having negative V_{SS}). Connections for the unipolar output operation are shown in Figure 5. The voltage at V_{REF} must never be negative with respect to DGND. Failure to observe this precaution may cause parasitic transistor action and possible device destruction. The code table for unipolar output operation is shown in Table II.

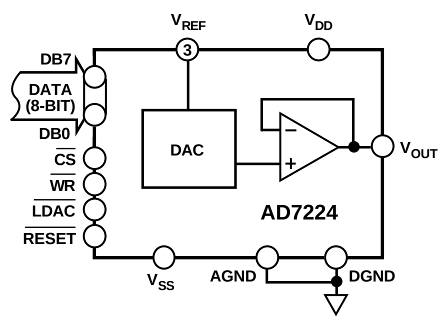


Figure 5. Unipolar Output Circuit

Table III. Unipolar Code Table

DAC Register Contents MSB	LSB	Analog Output
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{255}{256}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{129}{256}\right)$
1 0 0 0	0 0 0 0	$+V_{REF}\left(\frac{128}{256}\right) = +\frac{V_{REF}}{2}$
0 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{256}\right)$
0 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{256}\right)$
0 0 0 0	0 0 0 0	$0\ V$

Note: $1\ LSB = (V_{REF})(2^{-8}) = V_{REF}\left(\frac{1}{256}\right)$

BIPOLAR OUTPUT OPERATION

The AD7224 can be configured to provide bipolar output operation using one external amplifier and two resistors. Figure 6 shows a circuit used to implement offset binary coding. In this case

$$V_O = \left(1 + \frac{R2}{R1}\right) \bullet \left(D\ V_{REF}\right) - \left(\frac{R2}{R1}\right) \bullet \left(V_{REF}\right)$$

With $R1 = R2$

$$V_O = (2\,D - 1) \bullet V_{REF}$$

where D is a fractional representation of the digital word in the DAC register.

Mismatch between R1 and R2 causes gain and offset errors; therefore, these resistors must match and track over temperature. Once again, the AD7224 can be operated in single supply or from positive/negative supplies. Table III shows the digital code versus output voltage relationship for the circuit of Figure 6 with R1 = R2.

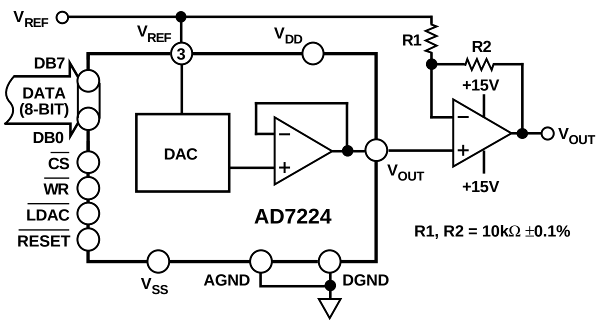


Figure 6. Bipolar Output Circuit

Table III. Bipolar (Offset Binary) Code Table

DAC Register Contents MSB	LSB	Analog Output
1 1 1 1	1 1 1 1	$+V_{REF}\left(\frac{127}{128}\right)$
1 0 0 0	0 0 0 1	$+V_{REF}\left(\frac{1}{128}\right)$
1 0 0 0	0 0 0 0	$0\ V$
0 1 1 1	1 1 1 1	$-V_{REF}\left(\frac{1}{128}\right)$
0 0 0 0	0 0 0 1	$-V_{REF}\left(\frac{127}{128}\right)$
0 0 0 0	0 0 0 0	$-V_{REF}\left(\frac{128}{128}\right) = -V_{REF}$

AGND BIAS

The AD7224 AGND pin can be biased above system GND (AD7224 DGND) to provide an offset "zero" analog output voltage level. Figure 7 shows a circuit configuration to achieve this. The output voltage, V_{OUT}, is expressed as:

$$V_{OUT} = V_{BIAS} + D \bullet (V_{IN})$$

where D is a fractional representation of the digital word in DAC register and can vary from 0 to 255/256.

For a given V_{IN}, increasing AGND above system GND will reduce the effective V_{DD}–V_{REF} which must be at least 4 V to ensure specified operation. Note that V_{DD} and V_{SS} for the AD7224 must be referenced to DGND.

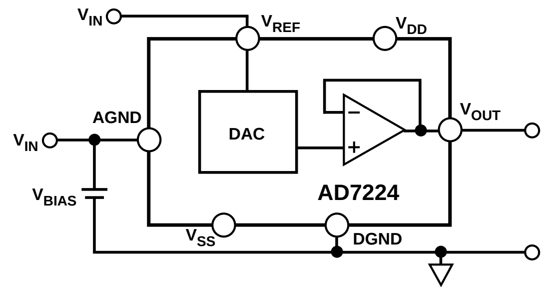


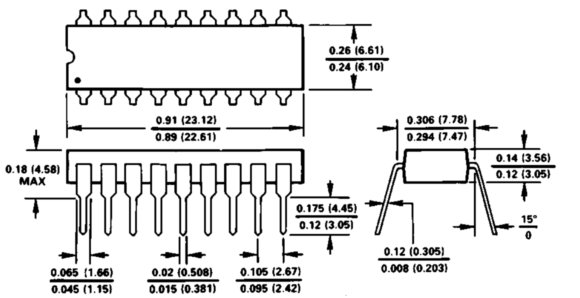
Figure 7. AGND Bias Circuit

MICROPROCESSOR INTERFACE

OUTLINE DIMENSIONS

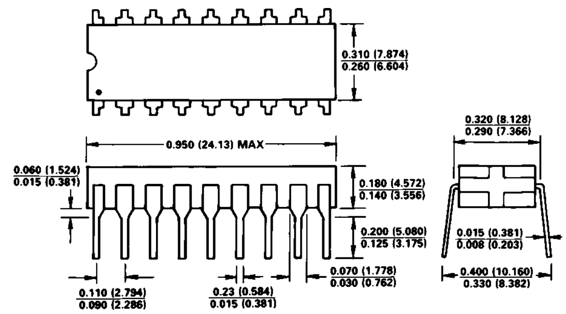
Dimensions shown in inches and (mm).

18-Pin Plastic (Suffix N)



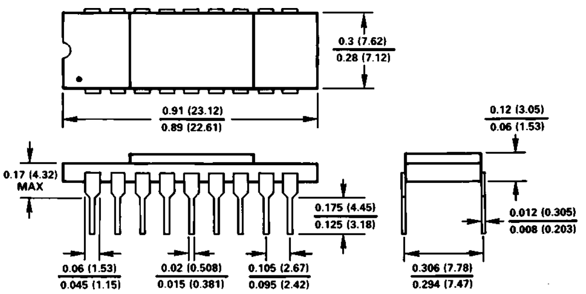
NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

18-Pin Cerdip (Suffix Q)



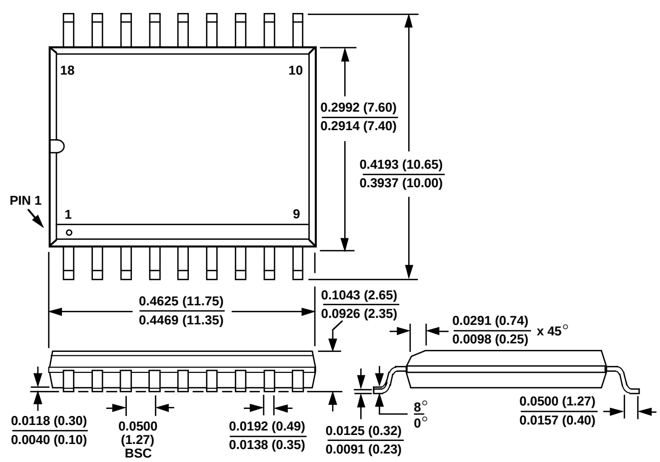
NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

18-Pin Ceramic (Suffix D)

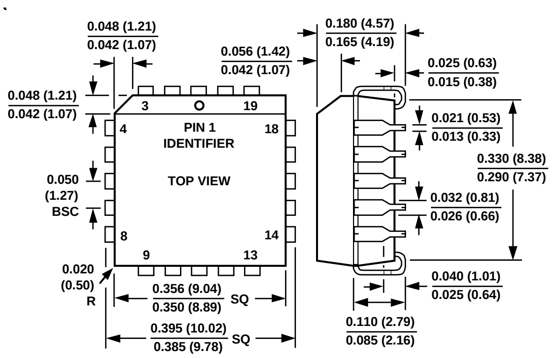


NOTES:
1. LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH.
2. CERAMIC DIP LEADS WILL BE EITHER GOLD OR TIN PLATED IN ACCORDANCE WITH MIL-M-38510 REQUIREMENTS.

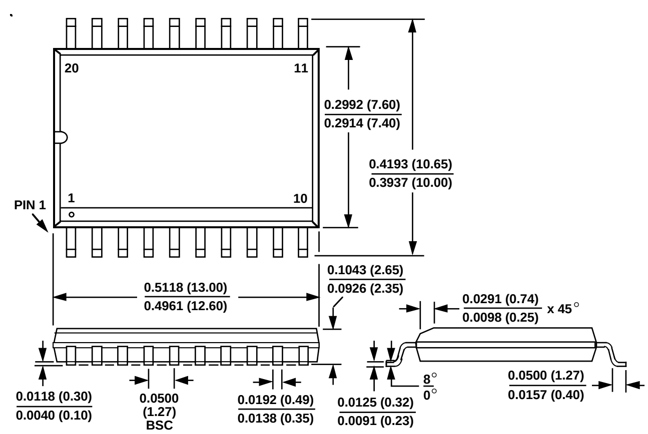
18-Lead SOIC (R-18)



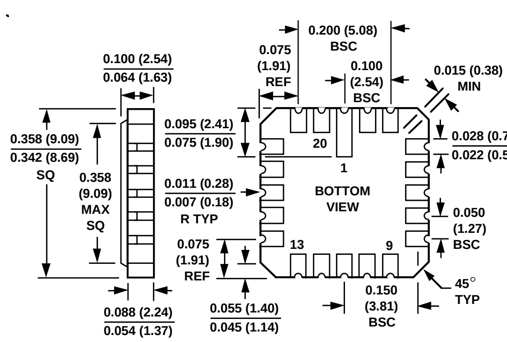
PLCC Package P-20A



20-Lead SOIC (R-20)



LCCC Package E-20A



C836a–10–10/84
PRINTED IN U.S.A.