PRELIMINARY

Am55DL128C8G

Stacked Multi-Chip Package (MCP) Flash Memory and SRAM

Two Am29DL640G 64 Megabit (4 M x 16-Bit) CMOS 3.0 Volt-only, Simultaneous Read/Write Flash Memories and 64 Mbit (4 M x 16-Bit) Fast Cycle RAM and 8 Mbit (512K x 16-Bit) Static RAM

DISTINCTIVE CHARACTERISTICS

MCP Features

- **Power supply voltage of 2.7 to 3.1 volt**
- **High performance**
  - — Access time as fast as 70 ns
- **Package**
  - — 93-Ball FBGA
- **Operating Temperature**
  - — –40°C to +85°C

Flash Memory Features

ARCHITECTURAL ADVANTAGES

- **Simultaneous Read/Write operations**
  - — Data can be continuously read from one bank while executing erase/program functions in another bank.
  - — Zero latency between read and write operations
- **Flexible Bank™ architecture**
  - — Read may occur in any of the three banks not being written or erased.
  - — Four banks may be grouped by customer to achieve desired bank divisions.
- **Manufactured on 0.17 µm process technology**
- **SecSi™ (Secured Silicon) Sector: Extra 256 Byte sector**
  - — *Factory locked and identifiable:* 16 bytes available for secure, random factory Electronic Serial Number; verifiable as factory locked through autoselect function. ExpressFlash option allows entire sector to be available for factory-secured data
  - — *Customer lockable:* Sector is one-time programmable. Once sector is locked, data cannot be changed.
- **Zero Power Operation**
  - — Sophisticated power management circuits reduce power consumed during inactive periods to nearly zero.
- **Boot sectors**
  - — Top and bottom boot sectors in the same device
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply flash standard

PERFORMANCE CHARACTERISTICS

- **High performance**
  - — Access time as fast as 70 ns
  - — Program time: 4 µs/word typical utilizing Accelerate function
- **Ultra low power consumption (typical values)**
  - — 2 mA active read current at 1 MHz
  - — 10 mA active read current at 5 MHz
  - — 200 nA in standby or automatic sleep mode
- **Minimum 1 million erase cycles guaranteed per sector**
- **20 year data retention at 125°C**
  - — Reliable operation for the life of the system

SOFTWARE FEATURES

- **Data Management Software (DMS)**
  - — AMD-supplied software manages data programming, enabling EEPROM emulation
  - — Eases historical sector erase flash limitations
- **Supports Common Flash Memory Interface (CFI)**
- **Program/Erase Suspend/Erase Resume**
  - — Suspends program/erase operations to allow programming/erasing in same bank
- **Data# Polling and Toggle Bits**
  - — Provides a software method of detecting the status of program or erase cycles
- **Unlock Bypass Program command**
  - — Reduces overall programming time when issuing multiple program command sequences

HARDWARE FEATURES

- **Any combination of sectors can be erased**
- **Ready/Busy# output (RY/BY#)**
  - — Hardware method for detecting program or erase cycle completion
- **Hardware reset pin (RESET#)**
  - — Hardware method of resetting the internal state machine to the read mode
- **WP#/ACC input pin**
  - — Write protect (WP#) function protects sectors 0, 1, 140, and 141, regardless of sector protect status
  - — Acceleration (ACC) function accelerates program timing
- **Sector protection**
  - — Hardware method of locking a sector, either in-system or using programming equipment, to prevent any program or erase operation within that sector
  - — Temporary Sector Unprotect allows changing data in protected sectors in-system

FCRAM Features

- **Power dissipation**
  - — Operating: 25 mA maximum
  - — Standby: 150 µA maximum
  - — Deep power-down standby: 10 µA
- **CE1s# and CE2s Chip Select**
- **Power down features using CE1s# and CE2s**
- **Data retention supply voltage: 2.7 to 3.1 volt**
- **Byte data control: LB#s (DQ7–DQ0), UB#s (DQ15–DQ8)**

SRAM Features

- **Power dissipation**
  - — Operating: 30 mA maximum
  - — Standby: 15µA maximum
- **CE1s# and CE2s Chip Select**
- **Power down features using CE1s# and CE2s**
- **Data retention supply voltage: 1.5 to 3.1 volt**
- **Byte data control: LB#s (DQ7–DQ0), UB#s (DQ15–DQ8)**

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GENERAL DESCRIPTION

Am29DL640G Features

The Am29DL640G is a 64 megabit, 3.0 volt-only flash memory device, organized as 4,194,304 words of 16 bits each or 8,388,608 bytes of 8 bits each. Word mode data appears on DQ15–DQ0; byte mode data appears on DQ7–DQ0. The device is designed to be programmed in-system with the standard 3.0 volt V_{CC} supply, and can also be programmed in standard EPROM programmers.

The device is available with an access time of 70 or 85 ns and is offered in a 93-ball FBGA package. Standard control pins—chip enable (CE#f), write enable (WE#), and output enable (OE#)—control normal read and write operations, and avoid bus contention issues.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

Simultaneous Read/Write Operations with Zero Latency

The Simultaneous Read/Write architecture provides **simultaneous operation** by dividing the memory space into **four banks,** two 8 Mb banks with small and large sectors, and two 24 Mb banks of large sectors only. Sector addresses are fixed, system software can be used to form user-defined bank groups.

During an Erase/Program operation, any of the three non-busy banks may be read from. Note that only two banks can operate simultaneously. The device can improve overall system performance by allowing a host system to program or erase in one bank, then immediately and simultaneously read from the other bank, with zero latency. This releases the system from waiting for the completion of program or erase operations.

The Am29DL640G can be organized as both a top and bottom boot sector configuration.

Bank	Megabits	Sector Sizes
Bank 1	8 Mb	Eight 8 Kbyte/4 Kword, Fifteen 64 Kbyte/32 Kword
Bank 2	24 Mb	Forty-eight 64 Kbyte/32 Kword
Bank 3	24 Mb	Forty-eight 64 Kbyte/32 Kword
Bank 4	8 Mb	Eight 8 Kbyte/4 Kword, Fifteen 64 Kbyte/32 Kword

The **SecSi™ (Secured Silicon) Sector** is an extra 256 byte sector capable of being permanently locked by AMD or customers. The **SecSi Indicator Bit** (DQ7) is permanently set to a 1 if the part is **factory locked**, and set to a 0 if **customer lockable**. This way, customer lockable parts can never be used to replace a factory locked part.

Factory locked parts provide several options. The SecSi Sector may store a secure, random 16 byte ESN (Electronic Serial Number), customer code (programmed through AMD's ExpressFlash service), or both. Customer Lockable parts may utilize the SecSi Sector as a one-time programmable area.

DMS (Data Management Software) allows systems to easily take advantage of the advanced architecture of the simultaneous read/write product line by allowing removal of EEPROM devices. DMS will also allow the system software to be simplified, as it will perform all functions necessary to modify data in file structures, as opposed to single-byte modifications. To write or update a particular piece of data (a phone number or configuration data, for example), the user only needs to state which piece of data is to be updated, and where the updated data is located in the system. This is an advantage compared to systems where user-written software must keep track of the old data location, status, logical to physical translation of the data onto the Flash memory device (or memory devices), and more. Using DMS, user-written software does not need to interface with the Flash memory directly. Instead, the user's software accesses the Flash memory by calling one of only six functions. AMD provides this software to simplify system design and software integration efforts.

The device offers complete compatibility with the **JEDEC single-power-supply Flash command set standard**. Commands are written to the command register using standard microprocessor write timings. Reading data out of the device is similar to reading from other Flash or EPROM devices.

The host system can detect whether a program or erase operation is complete by using the device **status bits:** RY/BY# pin, DQ7 (Data# Polling) and DQ6/DQ2 (toggle bits). After a program or erase cycle has been completed, the device automatically returns to the read mode.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

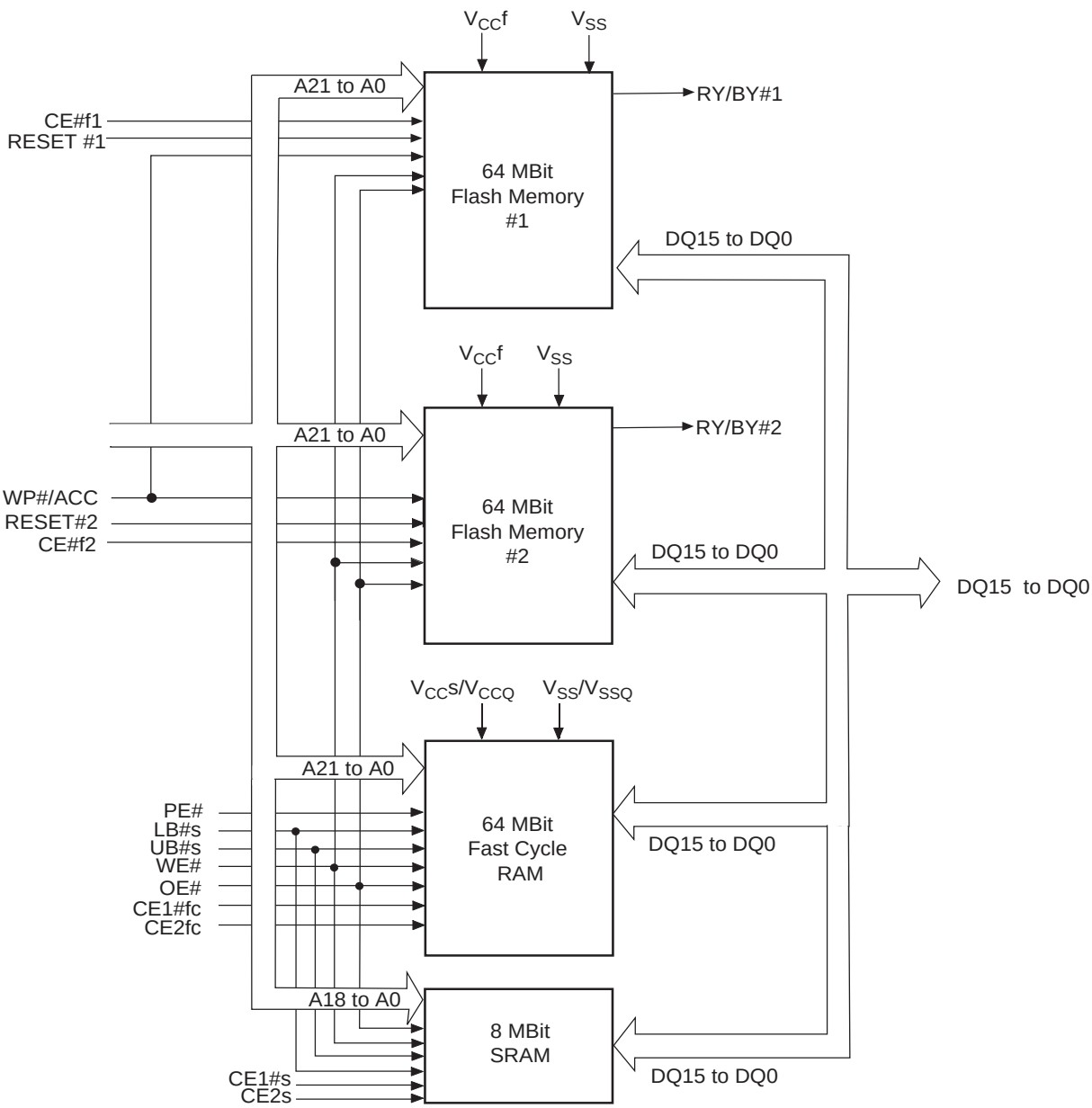
The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both modes.

TABLE OF CONTENTS

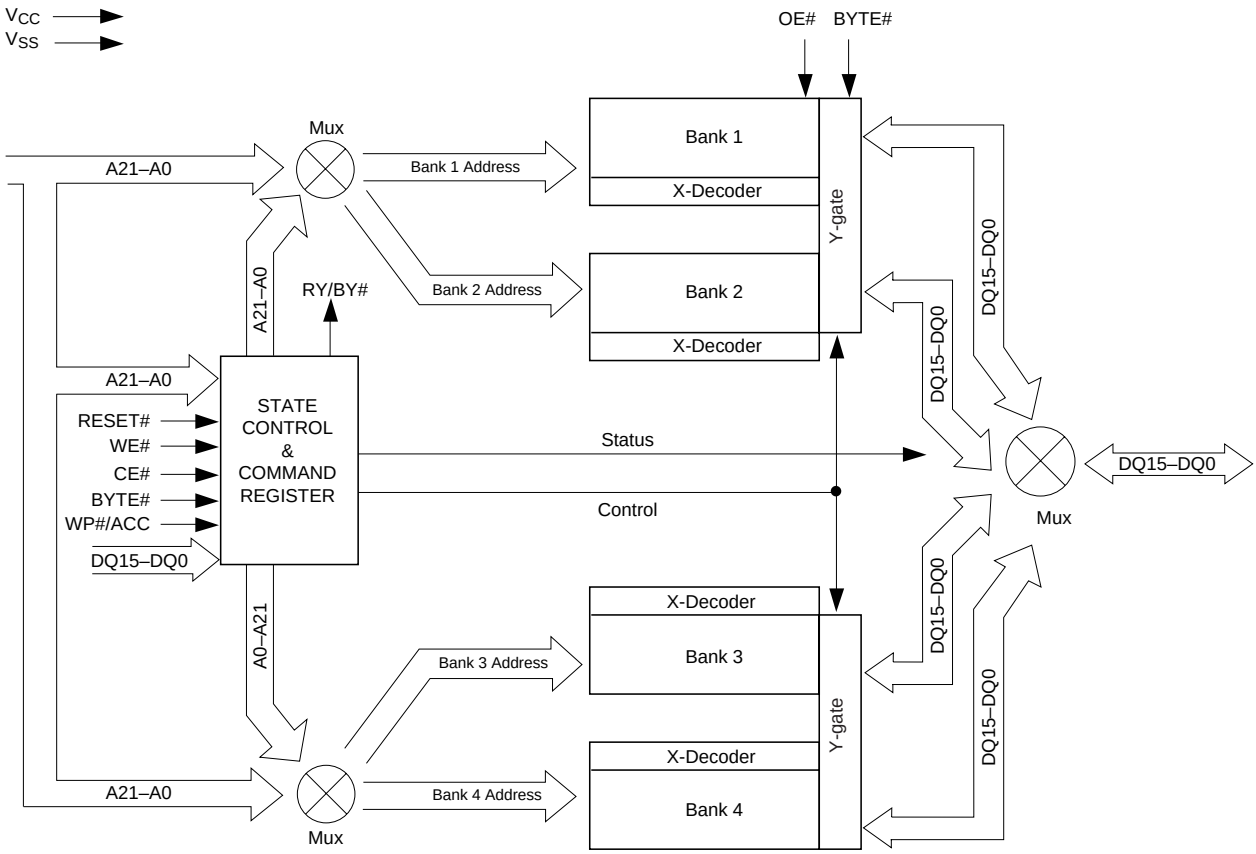
PRODUCT SELECTOR GUIDE

Part Number		Am55DL128C8G			
Speed Options	Standard Voltage Range: V_{CC} = 2.7–3.1 V	Flash Memory		Pseudo SRAM	
		70	85	70	85
Max Access Time, ns		70	85	70	85
CE#f Access, ns		70	85	70	85
OE# Access, ns		30	40	40	40

MCP BLOCK DIAGRAM

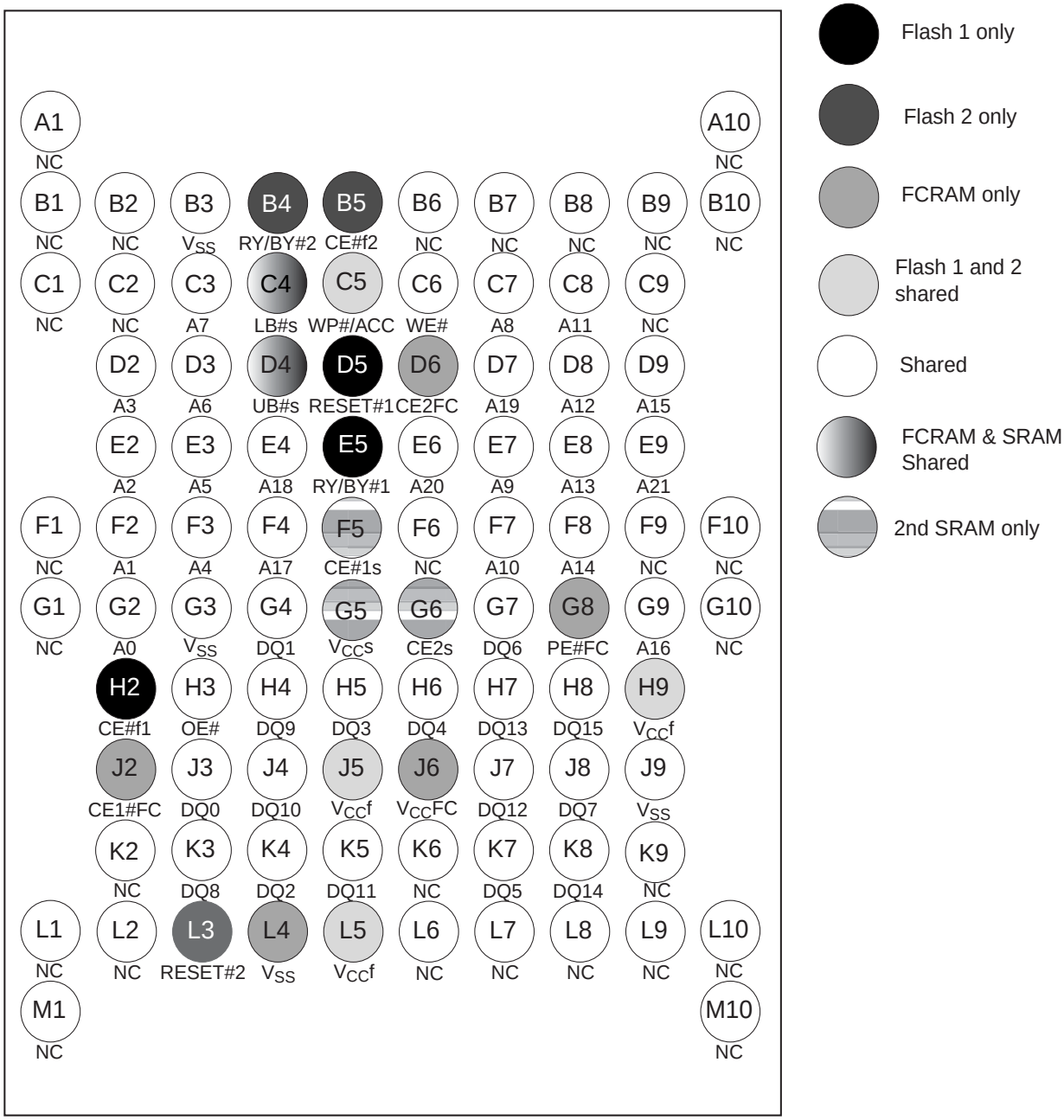


FLASH MEMORY BLOCK DIAGRAM



CONNECTION DIAGRAM

93-Ball FBGA
Top View



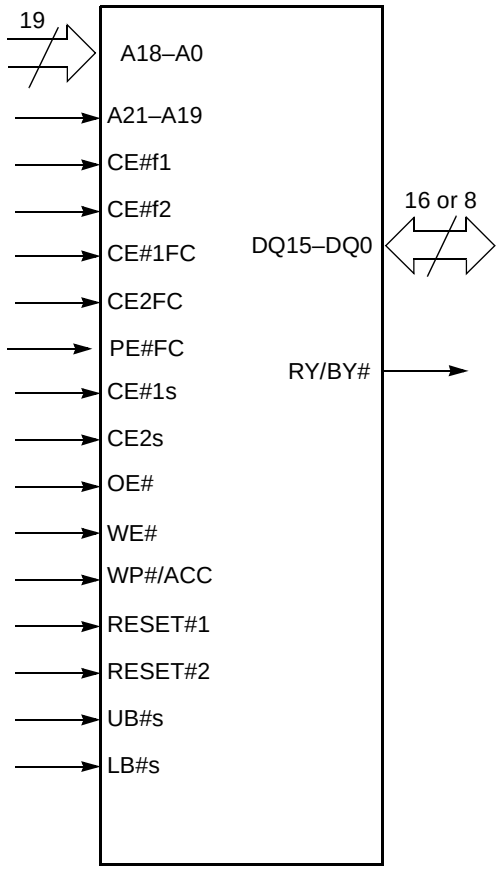
Special Package Handling Instructions

Special handling is required for Flash Memory products in molded packages (BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

PIN DESCRIPTION

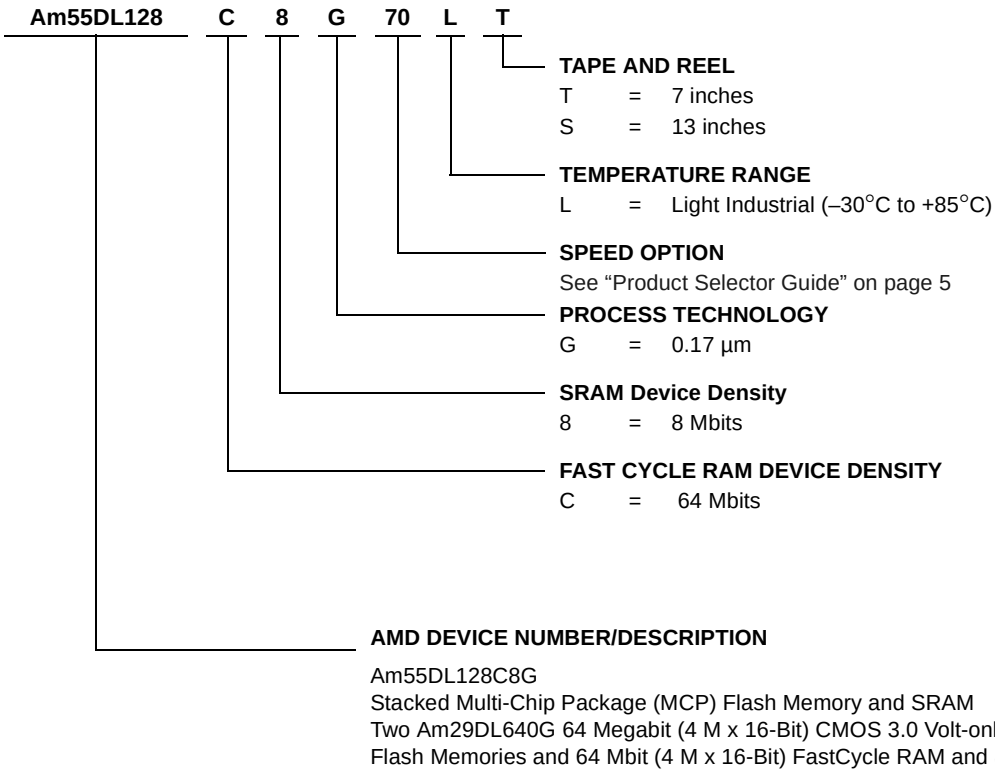
A18–A0	=	19 Address Inputs (Common)
A21–A19	=	2 Address Inputs (Flash + FCRAM)
DQ15–DQ0	=	16 Data Inputs/Outputs (Common)
CE#f1	=	Chip Enable 1 (Flash)
CE#f2	=	Chip Enable 2 (Flash)
OE#	=	Output Enable (Common)
WE#	=	Write Enable (Common)
RY/BY#1	=	Ready/Busy Output 1 (Flash 1)
RY/BY#2	=	Ready/Busy Output 2 (Flash 2)
UB#s	=	Upper Byte Control (FCRAM + SRAM)
LB#s	=	Lower Byte Control (FCRAM + SRAM)
RESET#1	=	Hardware Reset Pin, Active Low (Flash 1)
RESET#2	=	Hardware Reset Pin, Active Low (Flash 2)
WP#/ACC	=	Hardware Write Protect/ Acceleration Pin (Flash)
$V_{CC}f$	=	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
$V_{CC}s$	=	SRAM Power Supply
V_{SS}	=	Device Ground (Common)
NC	=	Pin Not Connected Internally
CE#1FC	=	Chip Enabled #1 (FCRAM)
CE2FC	=	Chip Enable #2 (FCRAM)
CE#1s	=	Chip Enable #1 (SRAM)
CE2s	=	Chip Enable #2 (SRAM)
$V_{CC}FC$	=	FCRAM power supply
PE#FC	=	FCRAM power down enable

LOGIC SYMBOL



ORDERING INFORMATION

The order number (Valid Combination) is formed by the following:



Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Valid Combinations		
Order Number		**Package Marking**
Am55DL128C8G70L	T, S	M550000000
Am55DL128C8G85L	T, S	M550000001

MCP DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Tables 1-2 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations—Flash Word Mode, (Notes 1, 2, 3)

Operation	Notes	CE#f Active (Note 3)	CE#f Inactive (Note 3)	CE#1s	CE2s	CE#1FC	CE2FC	PE#FC	OE#	WE#	Addr.	LB#s	UB#s	RESET#	WP#/ACC (Note 6)	DQ7–DQ0	DQ15–DQ8
Read from Active Flash	9	L	H	H	X	H	H	H	L	H	A_{IN}	X	X	H	L/H	D_{OUT}	D_{OUT}
	10			X	L												
Write to Active Flash	9	L	H	H	X	H	H	H	H	L	A_{IN}	X	X	H	6	D_{IN}	D_{IN}
	10			X	L												
Standby		$V_{CC} \pm 0.3$ V		H	H	H	H	H	X	X	X	X	X	$V_{CC} \pm 0.3$ V	H	High-Z	High-Z
				X	L												
Deep Power-down Standby		$V_{CC} \pm 0.3$ V		NA	NA	X	L	X	X	X	X	X	X	$V_{CC} \pm 0.3$ V	H	High-Z	High-Z
Output Disable	11	L	H	L	H	L	H	H	H	H	X	X	X	H	L/H	High-Z	High-Z
									H	H	X	X	X				
Flash Hardware Reset	9	X		H	X	H	H	H	X	X	X	X	X	L	L/H	High-Z	High-Z
	10			X	L												
Sector Protect	7, 9, 11	L	H	H	X	H	H	H	H	L	SADD, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	L/H	D_{IN}	X
	7,10, 11			X	L												
Sector Unprotect	7, 9, 11	L	H	H	X	H	H	H	H	L	SADD, A6 = H, A1 = H, A0 = L	X	X	V_{ID}	8	D_{IN}	X
	7,10, 11			X	L												
Temporary Sector Unprotect	9	X		H	X	H	H	H	X	X	X	X	X	V_{ID}	8	D_{IN}	High-Z
	10			X	L												
Read from SRAM		H	H	L	H	H	H	H	L	H	A_{IN}	L	L	H	X	D_{OUT}	D_{OUT}
												H	L			High-Z	D_{OUT}
												L	H			D_{OUT}	High-Z
Write to SRAM		H	H	L	H	H	H	H	X	L	A_{IN}	L	L	H	X	D_{IN}	D_{IN}
												H	L			High-Z	D_{IN}
												L	H			D_{IN}	High-Z
Read from FCRAM		H	H	H	X	L	H	H	L	H	A_{IN}	L	L	H	X	D_{OUT}	D_{OUT}
												H	L			High-Z	D_{OUT}
				X	L							L	H			D_{OUT}	High-Z
Write to FCRAM		H	H	H	X	L	H	H	H	L	A_{IN}	L	L	H	X	D_{OUT}	D_{OUT}
												H	L			High-Z	D_{OUT}
				X	L							L	H			D_{OUT}	High-Z
Power Down Program	13	$V_{CC} \pm 0.3$ V		H	X	H	H	L	X	X	Key (12)	X	X	$V_{CC} \pm 0.3$ V	H	High-Z	High-Z
				X	L												

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SADD = Flash Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Other operations except for those indicated in this column are inhibited.*
2. *Do not apply CE#f1 or 2 = V_{IL}, CE#1s = V_{IL} and CE2s = V_{IH} at the same time.*
3. *All operations assume FCRAM is in standby. To put in Power Down program PE must be Low. To put in Power Down CE2 must be Low.*
4. *Active flash is device being addressed.*
5. *Don't care or open LB#s or UB#s.*
6. *If WP#/ACC = V_{IL}, the boot sectors will be protected. If WP#/ACC = V_{IH} the boot sectors protection will be removed. If WP#/ACC = V_{ACC} (9V), the program time will be reduced by 40%.*
7. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "Sector/Sector Block Protection and Unprotection" section.*
8. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "Sector/Sector Block Protection and Unprotection". If WP#/ACC = V_{HH}, all sectors will be unprotected.*
9. *Data will be retained in FCRAM.*
10. *Data will be lost in FCRAM.*
11. *CE# inputs on both flash devices may be held low for this operation.*
12. *See "Power Down Program Key Table" on p. 13*
13. *Valid for FCRAM only.*

FCRAM POWER DOWN PROGRAM

Definition	A0	A8	A21	A20
KEY	Mode Select	Area Select		

A18	A21	A20	AREA
L	L	L	BOTTOM (2)
L	H	X	RESERVED
H	L	X	RESERVED
H	H	H	TOP (3)

A0	A8	Mode
L	L	NAP (4)
L	H	RESERVED
H	L	16M Partial
H	H	SLEEP (4, 5)

Table 2. Basic Key Table

Mode	A0	A8	A18	A21	A20	Data Retention Area
	Mode Select		Area Select			
NAP	L	L	X	X	X	None
16M Partial	H	L	L	L	L	Bottom 16M only
	H	L	H	H	H	Top 16M only
SLEEP	H	H	X	X	X	None

Table 3. Available Key Table

Notes:

1. *The Power Down Program can be performed one time after compliance of Power-up timings and it should not be re-programmed after regular Read or Write. Unspecified addresses, A1 to A7, A9 to A17 and A19, can be either High or Low during the programming. The RESERVED key should not be used.*
2. *BOTTOM area is from the lowest address location.*
3. *TOP area is from the highest address location.*
4. *NAP and SLEEP do not retain the data and Area Select is ignored.*
5. *Default state. Power Down Program to this SLEEP mode can be omitted.*

FLASH DEVICE BUS OPERATIONS

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE#f and OE# pins to V_{IL}. CE#f is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. Each bank remains enabled for read access until the command register contents are altered.

Refer to the Flash Read-Only Operations table for timing specifications and to Figure 15 for the timing diagram. I_{CC1} in the DC Characteristics table represents the active current specification for reading array data.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE#f to V_{IL}, and OE# to V_{IH}.

For program operations, the CIOf pin determines whether the device accepts program data in bytes or words. Refer to “Flash Device Bus Operations” for more information.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once a bank enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The “Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Table 4 indicates the address space that each sector occupies. Similarly, a “sector address” is the address bits required to uniquely select a sector. The “Flash Command Definitions” section has details on erasing a sector or the entire chip, or suspending/resuming the erase operation.

The device address space is divided into four banks. A “bank address” is the address bits required to uniquely select a bank.

I_{CC2} in the DC Characteristics table represents the active current specification for the write mode. The Flash AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that V_{HH} must not be asserted on WP#/ACC for operations other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result*. See “Write Protect (WP#)” on page 19 for related information.

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ15–DQ0. Standard read cycle timings apply in this mode. Refer to the Sector/Sector Block Protection and Unprotection and Autoselect Command Sequence sections for more information.

Simultaneous Read/Write Operations with Zero Latency

This device is capable of reading data from one bank of memory while programming or erasing in the other bank of memory. An erase operation may also be suspended to read from or program to another location within the same bank (except the sector being erased). Figure 20 shows how read and write cycles may be initiated for simultaneous operation with zero latency. I_{CC6}f and I_{CC7}f in the table represent the current specifications for read-while-program and read-while-erase, respectively.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE#f and RESET# pins are both held at $V_{CC} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE#f and RESET# are held at V_{IH}, but not

within V_{CC} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

I_{CC3}f in the table represents the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#f, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. I_{CC5}f in the table represents the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}f). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

If RESET# is asserted during a program or erase operation, the RY/BY# pin remains a “0” (busy) until the internal reset operation is complete, which requires a time of t_{READY} (during Embedded Algorithms). The system can thus monitor RY/BY# to determine whether the reset operation is complete. If RESET# is asserted when a program or erase operation is not executing (RY/BY# pin is “1”), the reset operation is completed within a time of t_{READY} (not during Embedded Algorithms). The system can read data t_{RH} after the RESET# pin returns to V_{IH}.

Refer to the MCP AC Characteristics tables for RESET# parameters and to Figure 16 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 4. Am29DL640G Sector Architecture

Bank	Sector	Sector Address A21–A12	Sector Size (Kbytes/Kwords)	(x16) Address Range
Bank 1	SA0	0000000000	8/4	00000h–00FFFh
	SA1	0000000001	8/4	01000h–01FFFh
	SA2	0000000010	8/4	02000h–02FFFh
	SA3	0000000011	8/4	03000h–03FFFh
	SA4	0000000100	8/4	04000h–04FFFh
	SA5	0000000101	8/4	05000h–05FFFh
	SA6	0000000110	8/4	06000h–06FFFh
	SA7	0000000111	8/4	07000h–07FFFh
	SA8	0000001xxx	64/32	08000h–0FFFFh
	SA9	0000010xxx	64/32	10000h–17FFFh
	SA10	0000011xxx	64/32	18000h–1FFFFh
	SA11	0000100xxx	64/32	20000h–27FFFh
	SA12	0000101xxx	64/32	28000h–2FFFFh
	SA13	0000110xxx	64/32	30000h–37FFFh
	SA14	0000111xxx	64/32	38000h–3FFFFh
	SA15	0001000xxx	64/32	40000h–47FFFh
	SA16	0001001xxx	64/32	48000h–4FFFFh
	SA17	0001010xxx	64/32	50000h–57FFFh
	SA18	0001011xxx	64/32	58000h–5FFFFh
	SA19	0001100xxx	64/32	60000h–67FFFh
	SA20	0001101xxx	64/32	68000h–6FFFFh
	SA21	0001101xxx	64/32	70000h–77FFFh
	SA22	0001111xxx	64/32	78000h–7FFFFh

Table 4. Am29DL640G Sector Architecture (Continued)

Bank	Sector	Sector Address A21–A12	Sector Size (Kbytes/Kwords)	(x16) Address Range
Bank 2	SA23	0010000xxx	64/32	80000h–87FFFh
	SA24	0010001xxx	64/32	88000h–8FFFFh
	SA25	0010010xxx	64/32	90000h–97FFFh
	SA26	0010011xxx	64/32	98000h–9FFFFh
	SA27	0010100xxx	64/32	A0000h–A7FFFh
	SA28	0010101xxx	64/32	A8000h–AFFFFh
	SA29	0010110xxx	64/32	B0000h–B7FFFh
	SA30	0010111xxx	64/32	B8000h–BFFFFh
	SA31	0011000xxx	64/32	C0000h–C7FFFh
	SA32	0011001xxx	64/32	C8000h–CFFFFh
	SA33	0011010xxx	64/32	D0000h–D7FFFh
	SA34	0011011xxx	64/32	D8000h–DFFFFh
	SA35	0011000xxx	64/32	E0000h–E7FFFh
	SA36	0011101xxx	64/32	E8000h–EFFFFh
	SA37	0011110xxx	64/32	F0000h–F7FFFh
	SA38	0011111xxx	64/32	F8000h–FFFFFh
	SA39	0100000xxx	64/32	F9000h–107FFFh
	SA40	0100001xxx	64/32	108000h–10FFFFh
	SA41	0100010xxx	64/32	110000h–117FFFh
	SA42	0101011xxx	64/32	118000h–11FFFFh
	SA43	0100100xxx	64/32	120000h–127FFFh
	SA44	0100101xxx	64/32	128000h–12FFFFh
	SA45	0100110xxx	64/32	130000h–137FFFh
	SA46	0100111xxx	64/32	138000h–13FFFFh
	SA47	0101000xxx	64/32	140000h–147FFFh
	SA48	0101001xxx	64/32	148000h–14FFFFh
	SA49	0101010xxx	64/32	150000h–157FFFh
	SA50	0101011xxx	64/32	158000h–15FFFFh
	SA51	0101100xxx	64/32	160000h–167FFFh
	SA52	0101101xxx	64/32	168000h–16FFFFh
	SA53	0101110xxx	64/32	170000h–177FFFh
	SA54	0101111xxx	64/32	178000h–17FFFFh
	SA55	0110000xxx	64/32	180000h–187FFFh
	SA56	0110001xxx	64/32	188000h–18FFFFh
	SA57	0110010xxx	64/32	190000h–197FFFh
	SA58	0110011xxx	64/32	198000h–19FFFFh
	SA59	0100100xxx	64/32	1A0000h–1A7FFFh
	SA60	0110101xxx	64/32	1A8000h–1AFFFFh
	SA61	0110110xxx	64/32	1B0000h–1B7FFFh
	SA62	0110111xxx	64/32	1B8000h–1BFFFFh
	SA63	0111000xxx	64/32	1C0000h–1C7FFFh
	SA64	0111001xxx	64/32	1C8000h–1CFFFFh
	SA65	0111010xxx	64/32	1D0000h–1D7FFFh
	SA66	0111011xxx	64/32	1D8000h–1DFFFFh
	SA67	0111100xxx	64/32	1E0000h–1E7FFFh
	SA68	0111101xxx	64/32	1E8000h–1EFFFFh
	SA69	0111110xxx	64/32	1F0000h–1F7FFFh
	SA70	0111111xxx	64/32	1F8000h–1FFFFFh

Table 4. Am29DL640G Sector Architecture (Continued)

Bank	Sector	Sector Address A21–A12	Sector Size (Kbytes/Kwords)	(x16) Address Range
Bank 3	SA71	1000000xxx	64/32	200000h–207FFFh
	SA72	1000001xxx	64/32	208000h–20FFFFh
	SA73	1000010xxx	64/32	210000h–217FFFh
	SA74	1000011xxx	64/32	218000h–21FFFFh
	SA75	1000100xxx	64/32	220000h–227FFFh
	SA76	1000101xxx	64/32	228000h–22FFFFh
	SA77	1000110xxx	64/32	230000h–237FFFh
	SA78	1000111xxx	64/32	238000h–23FFFFh
	SA79	1001000xxx	64/32	240000h–247FFFh
	SA80	1001001xxx	64/32	248000h–24FFFFh
	SA81	1001010xxx	64/32	250000h–257FFFh
	SA82	1001011xxx	64/32	258000h–25FFFFh
	SA83	1001100xxx	64/32	260000h–267FFFh
	SA84	1001101xxx	64/32	268000h–26FFFFh
	SA85	1001110xxx	64/32	270000h–277FFFh
	SA86	1001111xxx	64/32	278000h–27FFFFh
	SA87	1010000xxx	64/32	280000h–28FFFFh
	SA88	1010001xxx	64/32	288000h–28FFFFh
	SA89	1010010xxx	64/32	290000h–297FFFh
	SA90	1010011xxx	64/32	298000h–29FFFFh
	SA91	1010100xxx	64/32	2A0000h–2A7FFFh
	SA92	1010101xxx	64/32	2A8000h–2AFFFFh
	SA93	1010110xxx	64/32	2B0000h–2B7FFFh
	SA94	1010111xxx	64/32	2B8000h–2BFFFFh
	SA95	1011000xxx	64/32	2C0000h–2C7FFFh
	SA96	1011001xxx	64/32	2C8000h–2CFFFFh
	SA97	1011010xxx	64/32	2D0000h–2D7FFFh
	SA98	1011011xxx	64/32	2D8000h–2DFFFFh
	SA99	1011100xxx	64/32	2E0000h–2E7FFFh
	SA100	1011101xxx	64/32	2E8000h–2EFFFFh
	SA101	1011110xxx	64/32	2F0000h–2FFFFFh
	SA102	1011111xxx	64/32	2F8000h–2FFFFFh
	SA103	1100000xxx	64/32	300000h–307FFFh
	SA104	1100001xxx	64/32	308000h–30FFFFh
	SA105	1100010xxx	64/32	310000h–317FFFh
	SA106	1100011xxx	64/32	318000h–31FFFFh
	SA107	1100100xxx	64/32	320000h–327FFFh
	SA108	1100101xxx	64/32	328000h–32FFFFh
	SA109	1100110xxx	64/32	330000h–337FFFh
	SA110	1100111xxx	64/32	338000h–33FFFFh
	SA111	1101000xxx	64/32	340000h–347FFFh
	SA112	1101001xxx	64/32	348000h–34FFFFh
	SA113	1101010xxx	64/32	350000h–357FFFh
	SA114	1101011xxx	64/32	358000h–35FFFFh
	SA115	1101100xxx	64/32	360000h–367FFFh
	SA116	1101101xxx	64/32	368000h–36FFFFh
	SA117	1101110xxx	64/32	370000h–377FFFh
	SA118	1101111xxx	64/32	378000h–37FFFFh

Table 4. Am29DL640G Sector Architecture (Continued)

Bank	Sector	Sector Address A21–A12	Sector Size (Kbytes/Kwords)	(x16) Address Range
Bank 4	SA119	1110000xxx	64/32	380000h–387FFFh
	SA120	1110001xxx	64/32	388000h–38FFFFh
	SA121	1110010xxx	64/32	390000h–397FFFh
	SA122	1110011xxx	64/32	398000h–39FFFFh
	SA123	1110100xxx	64/32	3A0000h–3A7FFFh
	SA124	1110101xxx	64/32	3A8000h–3AFFFFh
	SA125	1110110xxx	64/32	3B0000h–3B7FFFh
	SA126	1110111xxx	64/32	3B8000h–3BFFFFh
	SA127	1111000xxx	64/32	3C0000h–3C7FFFh
	SA128	1111001xxx	64/32	3C8000h–3CFFFFh
	SA129	1111010xxx	64/32	3D0000h–3D7FFFh
	SA130	1111011xxx	64/32	3D8000h–3DFFFFh
	SA131	1111100xxx	64/32	3E0000h–3E7FFFh
	SA132	1111101xxx	64/32	3E8000h–3EFFFFh
	SA133	1111110xxx	64/32	3F0000h–3F7FFFh
	SA134	1111111000	8/4	3F8000h–3F8FFFh
	SA135	1111111001	8/4	3F9000h–3F9FFFh
	SA136	1111111010	8/4	3FA000h–3FAFFFh
	SA137	1111111011	8/4	3FB000h–3FBFFFh
	SA138	1111111100	8/4	3FC000h–3FCFFFh
	SA139	1111111101	8/4	3FD000h–3FDFFFh
	SA140	1111111110	8/4	3FE000h–3FEFFFh
	SA141	1111111111	8/4	3FF000h–3FFFFFh

Note: *A21:A0 in word mode.*

Table 5. Bank Address

Bank	A21–A19
1	000
2	001, 010, 011
3	100, 101, 110
4	111

Table 6. SecSi™ Sector Addresses

Device	Sector Size	(x16) Address Range
Am29DL640G	256 bytes	00000h–0007Fh

Sector/Sector Block Protection and Unprotection

(Note: For the following discussion, the term “sector” applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table 7).

The hardware sector protection feature disables both program and erase operations in any sector. The hardware sector unprotection feature re-enables both program and erase operations in previously protected sectors. Sector protection/unprotection can be implemented via two methods.

Table 7. Am29DL640G Boot Sector/Sector Block Addresses for Protection/Unprotection

Sector	A21–A12	Sector/ Sector Block Size
SA0	0000000000	8 Kbytes
SA1	0000000001	8 Kbytes
SA2	0000000010	8 Kbytes
SA3	0000000011	8 Kbytes
SA4	0000000100	8 Kbytes
SA5	0000000101	8 Kbytes
SA6	0000000110	8 Kbytes
SA7	0000000111	8 Kbytes
SA8–SA10	0000001XXX, 0000010XXX, 0000011XXX,	192 (3x64) Kbytes
SA11–SA14	00001XXXXX	256 (4x64) Kbytes
SA15–SA18	00010XXXXX	256 (4x64) Kbytes
SA19–SA22	00011XXXXX	256 (4x64) Kbytes
SA23–SA26	00100XXXXX	256 (4x64) Kbytes
SA27-SA30	00101XXXXX	256 (4x64) Kbytes
SA31-SA34	00110XXXXX	256 (4x64) Kbytes
SA35-SA38	00111XXXXX	256 (4x64) Kbytes
SA39-SA42	01000XXXXX	256 (4x64) Kbytes
SA43-SA46	01001XXXXX	256 (4x64) Kbytes
SA47-SA50	01010XXXXX	256 (4x64) Kbytes
SA51-SA54	01011XXXXX	256 (4x64) Kbytes
SA55–SA58	01100XXXXX	256 (4x64) Kbytes
SA59–SA62	01101XXXXX	256 (4x64) Kbytes
SA63–SA66	01110XXXXX	256 (4x64) Kbytes
SA67–SA70	01111XXXXX	256 (4x64) Kbytes
SA71–SA74	10000XXXXX	256 (4x64) Kbytes
SA75–SA78	10001XXXXX	256 (4x64) Kbytes
SA79–SA82	10010XXXXX	256 (4x64) Kbytes
SA83–SA86	10011XXXXX	256 (4x64) Kbytes
SA87–SA90	10100XXXXX	256 (4x64) Kbytes
SA91–SA94	10101XXXXX	256 (4x64) Kbytes
SA95–SA98	10110XXXXX	256 (4x64) Kbytes
SA99–SA102	10111XXXXX	256 (4x64) Kbytes
SA103–SA106	11000XXXXX	256 (4x64) Kbytes
SA107–SA110	11001XXXXX	256 (4x64) Kbytes
SA111–SA114	11010XXXXX	256 (4x64) Kbytes
SA115–SA118	11011XXXXX	256 (4x64) Kbytes
SA119–SA122	11100XXXXX	256 (4x64) Kbytes
SA123–SA126	11101XXXXX	256 (4x64) Kbytes
SA127–SA130	11110XXXXX	256 (4x64) Kbytes
SA131–SA133	1111100XXX, 1111101XXX, 1111110XXX	192 (3x64) Kbytes
SA134	1111111000	8 Kbytes
SA135	1111111001	8 Kbytes
SA136	1111111010	8 Kbytes
SA137	1111111011	8 Kbytes
SA138	1111111100	8 Kbytes
SA139	1111111101	8 Kbytes
SA140	1111111101	8 Kbytes
SA141	1111111111	8 Kbytes

Sector Protect/Sector Unprotect requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 25 shows the timing diagram. For sector unprotect, all unprotected sectors must first be protected prior to the first sector unprotect write cycle. *Note that the sector unprotect algorithm unprotects all sectors in parallel. All previously protected sectors must be individually re-protected.* To change data in protected sectors efficiently, the temporary sector unprotect function is available. See “Temporary Sector Unprotect”.

The device is shipped with all sectors unprotected. AMD offers the option of programming and protecting sectors at its factory prior to shipping the device through AMD’s ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector is protected or unprotected. See the Sector/Sector Block Protection and Unprotection section for details.

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting without using V_{ID}. This function is one of two provided by the WP#/ACC pin.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in sectors 0, 1, 140, and 141, independently of whether those sectors were protected or unprotected using the method described in “Sector/Sector Block Protection and Unprotection”.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether sectors 0, 1, 140, and 141 were last set to be protected or unprotected. That is, sector protection or unprotection for these sectors depends on whether they were last protected or unprotected using the method described in “Sector/Sector Block Protection and Unprotection”.

Note that the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.

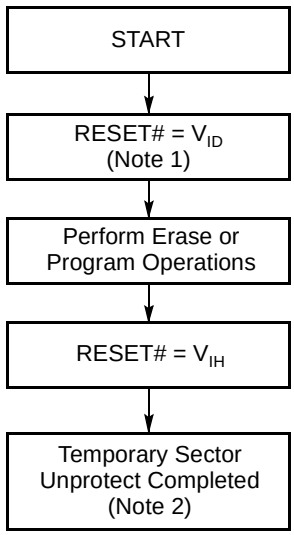
Table 8. WP#/ACC Modes

WP# Input Voltage	Device Mode
V_{IL}	Disables programming and erasing in SA0, SA1, SA140, and SA141
V_{IH}	Enables programming and erasing in SA0, SA1, SA140, and SA141
V_{HH}	Enables accelerated programming (ACC). See “Accelerated Program Operation” on page 13.

Temporary Sector Unprotect

(Note: For the following discussion, the term “sector” applies to both sectors and sector blocks. A sector block consists of two or more adjacent sectors that are protected or unprotected at the same time (see Table 7).

This feature allows temporary unprotection of previously protected sectors to change data in-system. The Sector Unprotect mode is activated by setting the RESET# pin to V_{ID}. During this mode, formerly protected sectors can be programmed or erased by selecting the sector addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sectors are protected again. Figure 1 shows the algorithm, and Figure 24 shows the timing diagrams, for this feature. If the WP#/ACC pin is at V_{IL}, sectors 0, 1, 140, and 141 will remain protected during the Temporary sector Unprotect mode.



Notes:

1. *All protected sectors unprotected (If WP#/ACC = V_{IL}, sectors 0, 1, 140, and 141 will remain protected).*
2. *All previously protected sectors are protected once again.*

Figure 1. Temporary Sector Unprotect Operation

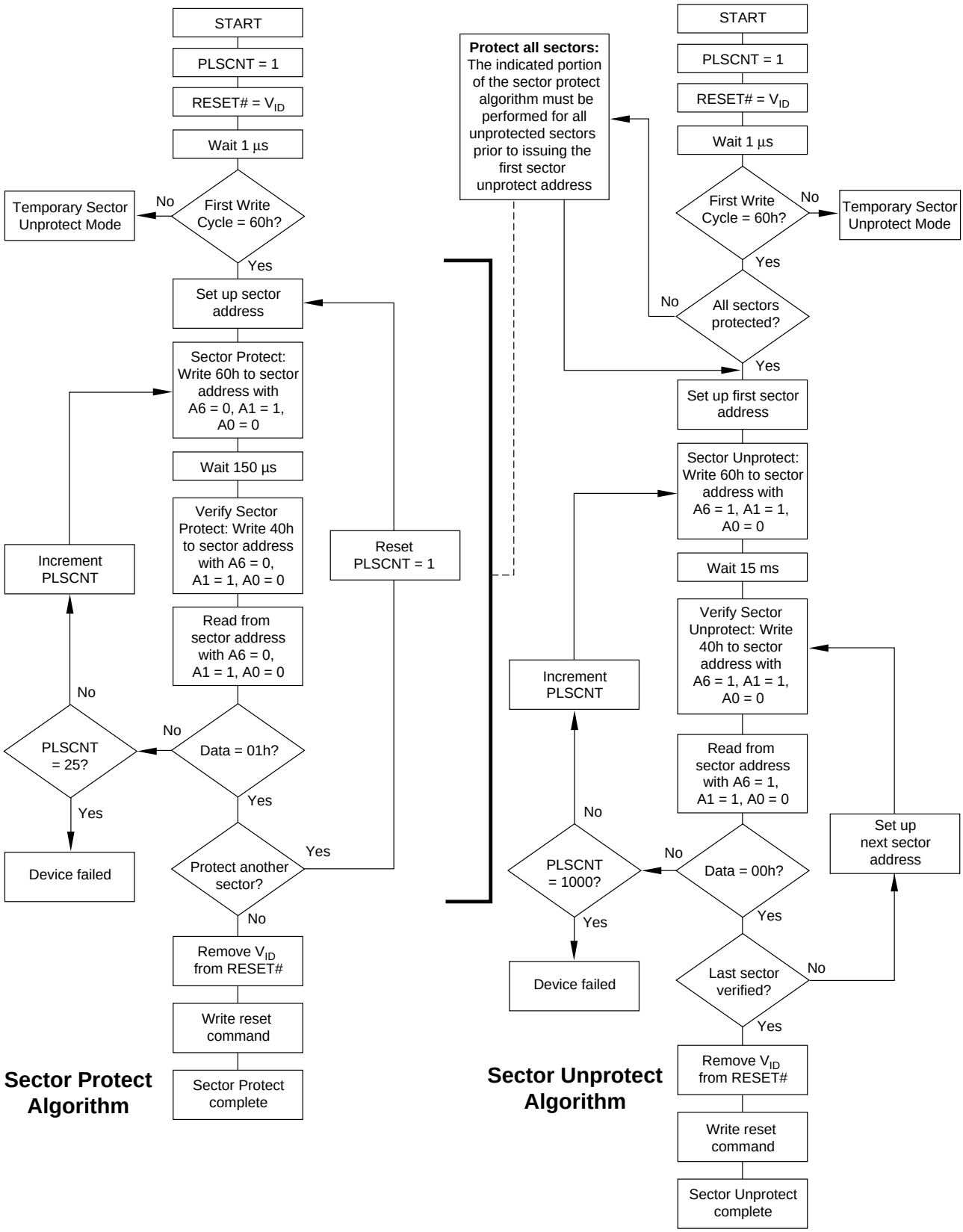


Figure 2. In-System Sector Protect/Unprotect Algorithms

SecSi™ (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 256 bytes in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

AMD offers the device with the SecSi Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "1." The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to utilize the that sector in any manner they choose. The customer-lockable version has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "0." Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The system accesses the SecSi Sector Secure through a command sequence (see "Enter SecSi™ Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the boot sectors. This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.* On power-up, or following a hardware reset, the device reverts to sending commands to the first 256 bytes of Sector 0.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In a factory locked device, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. The device is preprogrammed with both a random number and a secure ESN. The 8-word random number will at addresses 000000h–000007h in word mode (or 000000h–00000Fh in byte mode). The secure ESN will be programmed in the next 8 words at addresses 000008h–00000Fh (or 000010h–000020h in byte mode). The device is available preprogrammed with one of the following:

- A random, secure ESN only
- Customer code through the ExpressFlash service
- Both a random, secure ESN and customer code through the ExpressFlash service.

Customers may opt to have their code programmed by AMD through the AMD ExpressFlash service. AMD programs the customer's code, with or without the random ESN. The devices are then shipped from AMD's factory with the SecSi Sector permanently locked. Contact an AMD representative for details on using AMD's ExpressFlash service.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

If the security feature is not required, the SecSi Sector can be treated as an additional Flash memory space. The SecSi Sector can be read any number of times, but can be programmed and locked only once. Note that the accelerated programming (ACC) and unlock bypass functions are not available when programming the SecSi Sector.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either V_{IH} or V_{ID}*. This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 3.

Once the SecSi Sector is locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing the remainder of the array.

The SecSi Sector lock must be used with caution since, once locked, there is no procedure available for unlocking the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

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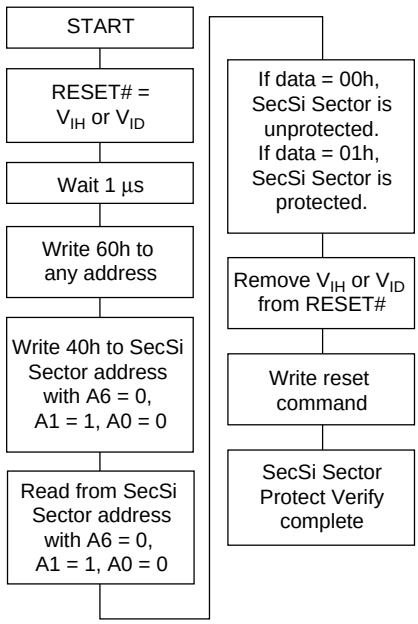


Figure 3. SecSi Sector Protect Verify

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Table 13 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE#f or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE#f = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE#f and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE#f = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h in word mode (or address AAh in byte mode), any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 9–12. To terminate reading CFI data, the system must write the reset command.The CFI Query mode is not accessible when the device is executing an Embedded Program or embedded Erase algorithm.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 9–12. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact an AMD representative for copies of these documents.

Table 9. CFI Query Identification String

Addresses (Word Mode)	Data	Description
10h 11h 12h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM Command Set
15h 16h	0040h 0000h	Address for Primary Extended Table
17h 18h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 10. System Interface String

Addresses (Word Mode)	Data	Description
1Bh	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	0004h	Typical timeout per single byte/word write 2^N µs
20h	0000h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	000Ah	Typical timeout per individual block erase 2^N ms
22h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	0005h	Max. timeout for byte/word write 2^N times typical
24h	0000h	Max. timeout for buffer write 2^N times typical
25h	0004h	Max. timeout per individual block erase 2^N times typical
26h	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 11. Device Geometry Definition

Addresses (Word Mode)	Data	Description
27h	0017h	Device Size = 2^N byte
28h 29h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	0000h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	0003h	Number of Erase Block Regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	007Dh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to the CFI specification or CFI publication 100)
35h 36h 37h 38h	0007h 0000h 0020h 0000h	Erase Block Region 3 Information (refer to the CFI specification or CFI publication 100)
39h 3Ah 3Bh 3Ch	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to the CFI specification or CFI publication 100)

Table 12. Primary Vendor-Specific Extended Query

Addresses (Word Mode)	Data	Description
40h 41h 42h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	0031h	Major version number, ASCII (reflects modifications to the silicon)
44h	0033h	Minor version number, ASCII (reflects modifications to the CFI table)
45h	0004h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Silicon Revision Number (Bits 7-2)
46h	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	0004h	Sector Protect/Unprotect scheme 01 =29F040 mode, 02 = 29F016 mode, 03 = 29F400, 04 = 29LV800 mode
4Ah	0077h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors (excluding Bank 1)
4Bh	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	0000h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	0085h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	0095h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	0001h	Top/Bottom Boot Sector Flag 00h = Uniform device, 01h = 8 x 8 Kbyte Sectors, Top And Bottom Boot with Write Protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Both Top and Bottom
50h	0001h	Program Suspend 0 = Not supported, 1 = Supported
57h	0004h	Bank Organization 00 = Data at 4Ah is zero, X = Number of Banks
58h	0017h	Bank 1 Region Information X = Number of Sectors in Bank 1
59h	0030h	Bank 2 Region Information X = Number of Sectors in Bank 2
5Ah	0030h	Bank 3 Region Information X = Number of Sectors in Bank 3
5Bh	0017h	Bank 4 Region Information X = Number of Sectors in Bank 4

FLASH COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Table 13 defines the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#f, whichever happens later. All data is latched on the rising edge of WE# or CE#f, whichever happens first. Refer to the MCP AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. Each bank is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the corresponding bank enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector within the same bank. The system can read array data using the standard read timing, except that if it reads at an address within erase-suspended sectors, the device outputs status data. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return a bank to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the bank is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the section for more information. The Flash Read-Only Operations table provides the read parameters, and Figure 15 shows the timing diagram.

Reset Command

Writing the reset command resets the banks to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the bank to which the system was writing to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the bank to which the system was writing to the read mode. If the program command sequence is written to a bank that is in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If a bank entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns that bank to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the banks to the read mode (or erase-suspend-read mode if that bank was in Erase Suspend).

Autoselect Command Sequence

The autoselect command sequence allows the host system to access the manufacturer and device codes, and determine whether or not a sector is protected. The autoselect command sequence may be written to an address within a bank that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing in the other bank.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the bank address and the autoselect command. The bank then enters the autoselect mode. The system may read any number of autoselect codes without reinitiating the command sequence.

Table 13 shows the address and data requirements. To determine sector protection information, the system must write to the appropriate bank address (BA) and sector address (SADD). Table 4 shows the address range and bank number associated with each sector.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the bank was previously in Erase Suspend).

Enter SecSi™ Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing a random, sixteen-byte electronic serial number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi

Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. The SecSi Sector is not accessible when the device is executing an Embedded Program or embedded Erase algorithm. Table 13 shows the address and data requirements for both command sequences. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.* See also "SecSi™ (Secured Silicon) Sector Flash Memory Region" for further information.

Word Program Command Sequence

The system may program the device by word. Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Table 13 shows the address and data requirements for the byte program command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

When the Embedded Program algorithm is complete, that bank then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7, DQ6, or RY/BY#. Refer to the Flash Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once that bank has returned to the read mode, to ensure data integrity.

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause that bank to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

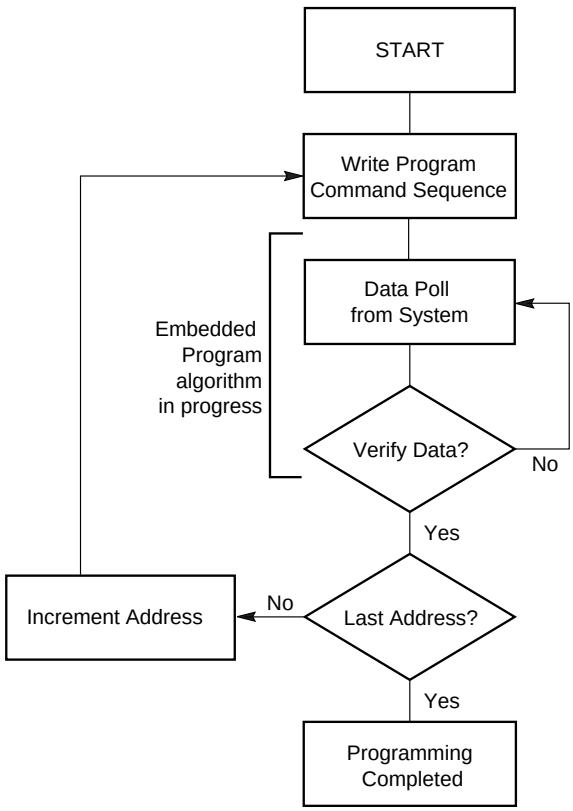
Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program bytes or words to a bank faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. That bank then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Table 13 shows the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. (See Table 13).

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the WP#/ACC pin must not be at V_{HH} any operation other than accelerated programming, or device damage may result. In addition, the WP#/ACC pin must not be left floating or unconnected; inconsistent behavior of the device may result.*

Figure 4 illustrates the algorithm for the program operation. Refer to the Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 17 for timing diagrams.



Note: *See Table 13 for program command sequence.*

Figure 4. Program Operation

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Table 13 shows the address and data requirements for the chip erase command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

When the Embedded Erase algorithm is complete, that bank returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, DQ2, or RY/BY#. Refer to the Flash Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 5 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 19 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Table 13 shows the address and data requirements for the sector erase command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a [program/erase] operation is in progress.*

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 80 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 80 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets that bank to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3: Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the bank returns to reading array data and addresses are no longer latched. Note that while the Embedded Erase operation is in progress, the system can read

data from the non-erasing bank. The system can determine the status of the erase operation by reading DQ7, DQ6, DQ2, or RY/BY# in the erasing bank. Refer to the Flash Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once that bank has returned to reading array data, to ensure data integrity.

Figure 5 illustrates the algorithm for the erase operation. Refer to the Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 19 section for timing diagrams.

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. The bank address is required when writing this command. This command is valid only during the sector erase operation, including the 80 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

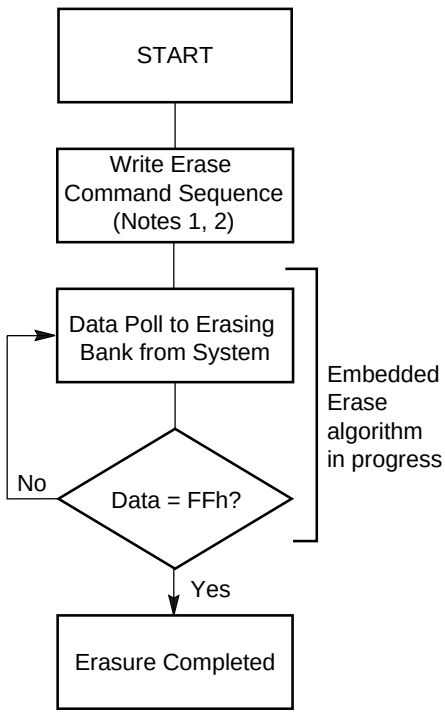
When the Erase Suspend command is written during the sector erase operation, the device requires a maximum of 20 µs to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation. Addresses are “don’t-cares” when writing the Erase suspend command.

After the erase operation has been suspended, the bank enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Flash Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the bank returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard Byte Program operation. Refer to the Flash Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. The device allows reading autoselect codes even at addresses within erasing sectors, since the codes are not stored in the memory array. When the device exits the autoselect mode, the device reverts to the Erase Suspend mode, and is ready for another valid operation. Refer to the Sector/Sector Block Protection and Unprotection and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command (address bits are don’t care). The bank address of the erase-suspended bank is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.



Notes:

1. *See Table 13 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 5. Erase Operation

Table 13. Am29DL640G Command Definitions

Command Sequence 1			Cycles	Bus Cycles (Notes 2–5)											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read 6			1	RA	RD										
Reset 7			1	XXX	F0										
Autoselect 8	Manufacturer ID	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X00	01				
	Device ID 9	Word	6	555	AA	2AA	55	(BA)555	90	(BA)X01	7E	(BA)X0E	02	(BA)X0F	01
	SecSi Sector Factory Protect 10	Word	4	555	AA	2AA	55	(BA)555	90	(BA)X03	80/00				
	Sector/Sector Block Protect Verify 11	Word	4	555	AA	2AA	55	(BA)555	90	(SADD) X02	00/01				
Enter SecSi Sector Region		Word	3	555	AA	2AA	55	555	88						
Exit SecSi Sector Region		Word	4	555	AA	2AA	55	555	90	XXX	00				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
Unlock Bypass Program 12			2	XXX	A0	PA	PD								
Unlock Bypass Reset 13			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SADD	30
Erase Suspend 14			1	BA	B0										
Erase Resume 15			1	BA	30										
CFI Query 16		Word	1	55	98										

Legend:

X = Don't care

RA = Address of the memory location to be read.

RD = Data read from location RA during read operation.

PA = Address of the memory location to be programmed. Addresses latch on the falling edge of the WE# or CE#f pulse, whichever happens later.

PD = Data to be programmed at location PA. Data latches on the rising edge of WE# or CE#f pulse, whichever happens first.

SADD = Address of the sector to be verified (in autoselect mode) or erased. Address bits A21–A12 uniquely select any sector. Refer to Table 4 for information on sector addresses.

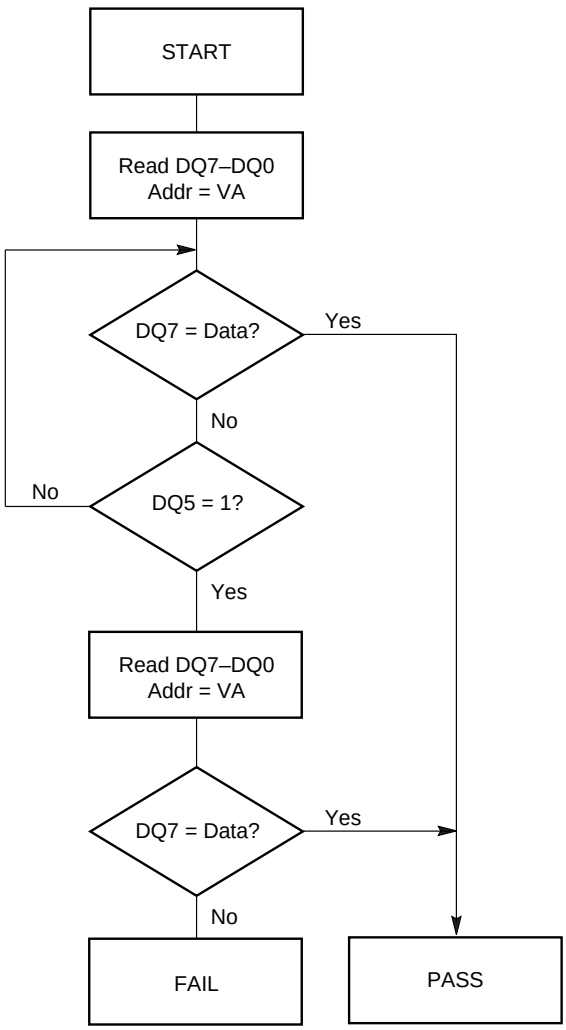
BA = Address of the bank that is being switched to autoselect mode, is in bypass mode, or is being erased. Address bits A21–A19 select a bank. Refer to Table 5 for information on sector addresses.

Notes:

1. *See Tables 1–2 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *Data bits DQ15–DQ8 are don't care in command sequences, except for RD and PD.*
5. *Unless otherwise noted, address bits A21–A12 are don't cares for unlock and command cycles, unless SADD or PA is required.*
6. *No unlock or command cycles required when bank is reading array data.*
7. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when a bank is in the autoselect mode, or if DQ5 goes high (while the bank is providing status information).*
8. *The fourth cycle of the autoselect command sequence is a read cycle. The system must provide the bank address to obtain the manufacturer ID, device ID, or SecSi Sector factory protect information. Data bits DQ15–DQ8 are don't care. See the Autoselect Command Sequence section for more information.*
9. *The device ID must be read across the fourth, fifth, and sixth cycles.*
10. *The data is 80h for factory locked and 00h for not factory locked.*
11. *The data is 00h for an unprotected sector/sector block and 01h for a protected sector/sector block.*
12. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
13. *The Unlock Bypass Reset command is required to return to the read mode when the bank is in the unlock bypass mode.*
14. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation, and requires the bank address.*
15. *The Erase Resume command is valid only during the Erase Suspend mode, and requires the bank address.*
16. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

FLASH WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 14 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = "1" because DQ7 may change simultaneously with DQ5.*

Figure 6. Data# Polling Algorithm

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether a bank is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then that bank returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a "0" on DQ7. When the Embedded Erase algorithm is complete, or if the bank enters the Erase Suspend mode, Data# Polling produces a "1" on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the bank returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

When the system detects DQ7 has changed from the complement to true data, it can read valid data at DQ15–DQ0 (or DQ7–DQ0 for byte mode) on the *following* read cycles. Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ15–DQ8 (DQ7–DQ0 in byte mode) while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ15–DQ0 may be still invalid. Valid data on DQ15–DQ0 (or DQ7–DQ0 for byte mode) will appear on successive read cycles.

Table 14 shows the outputs for Data# Polling on DQ7. Figure 5 shows the Data# Polling algorithm. Figure 21 in the MCP AC Characteristics section shows the Data# Polling timing diagram.

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or one of the banks is in the erase-suspend-read mode.

Table 14 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE#f to control the read cycles. When the operation is complete, DQ6 stops toggling.

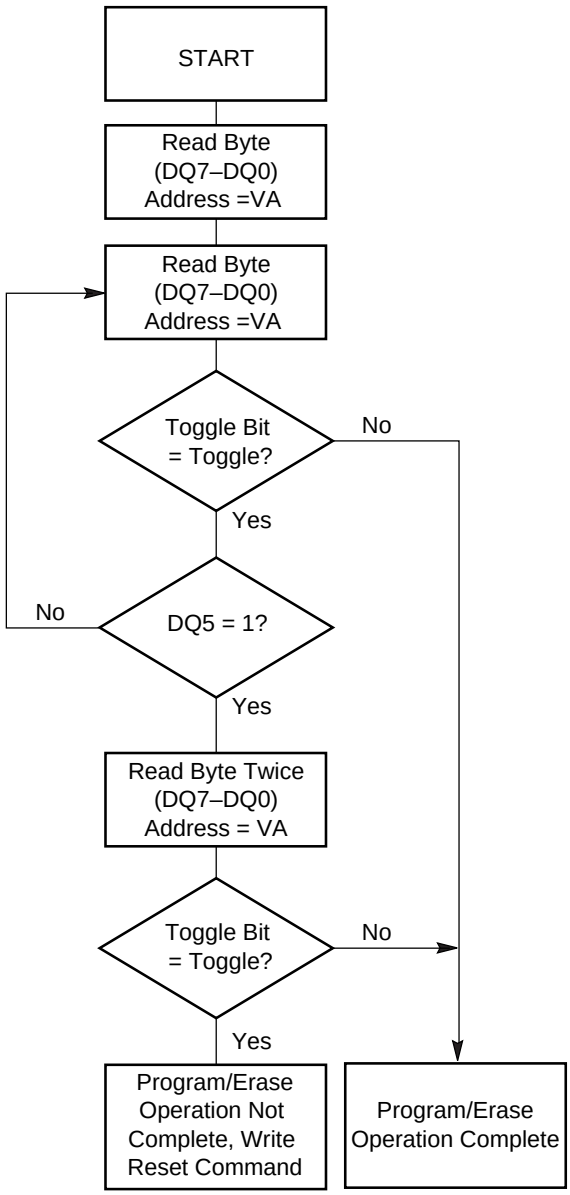
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 14 shows the outputs for Toggle Bit I on DQ6. Figure 7 shows the toggle bit algorithm. Figure 22 in the “Flash AC Characteristics” section shows the toggle bit timing diagrams. Figure 23 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note: *The system should recheck the toggle bit even if DQ5 = “1” because the toggle bit may stop toggling as DQ5 changes to “1.” See the subsections on DQ6 and DQ2 for more information.*

Figure 7. Toggle Bit Algorithm

DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE#f to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 14 to compare outputs for DQ2 and DQ6.

Figure 7 shows the toggle bit algorithm in flowchart form, and the section “DQ2: Toggle Bit II” explains the algorithm. See also the DQ6: Toggle Bit I subsection. Figure 22 shows the toggle bit timing diagram. Figure 23 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 7 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ15–DQ0 (or DQ7–DQ0 for byte mode) at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ15–DQ0 (or DQ7–DQ0 for byte mode) on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 7).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program or erase time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a “1,” indicating that the program or erase cycle was not successfully completed.

The device may output a “1” on DQ5 if the system tries to program a “1” to a location that was previously programmed to “0.” **Only an erase operation can change a “0” back to a “1.”** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a “1.”

Under both these conditions, the system must write the reset command to return to the read mode (or to the erase-suspend-read mode if a bank was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a “0” to a “1.” If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is “1,” the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is “0,” the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 14 shows the status of DQ3 relative to the other status bits.

Table 14. Write Operation Status

Status			DQ7 2	DQ6	DQ5 1	DQ3	DQ2 2	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	0
Erase Suspend Mode	Erase-Suspend-Read	Erase Suspended Sector	1	No toggle	0	N/A	Toggle	1
		Non-Erase Suspended Sector	Data	Data	Data	Data	Data	1
	Erase-Suspend-Program		DQ7#	Toggle	0	N/A	N/A	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program or Embedded Erase operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *When reading write operation status bits, the system must always provide the bank address where the Embedded Algorithm is in progress. The device outputs array data if the system addresses a non-busy bank.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –55°C to +125°C

Ambient Temperature
with Power Applied . . . . . –30°C to +85°C

Voltage with Respect to Ground

V_{CC}f, V_{CC}s (Note 1) . . . . . –0.5 V to +4.0 V

RESET# (Note 2) . . . . . –0.5 V to +12.5 V

WP#/ACC . . . . . –0.5 V to +10.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 8. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 9.*
2. *Minimum DC input voltage on pins RESET#, and WP#/ACC is –0.5 V. During voltage transitions, WP#/ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 8. Maximum DC input voltage on pin RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns. Maximum DC input voltage on WP#/ACC is +9.5 V which may overshoot to +12.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

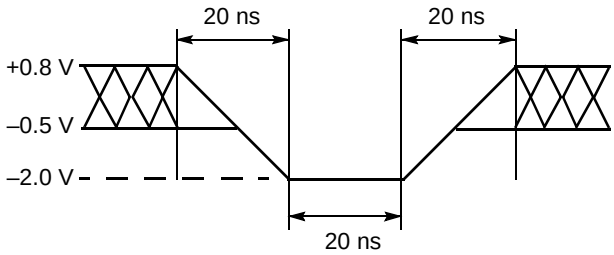


Figure 8. Maximum Negative Overshoot Waveform

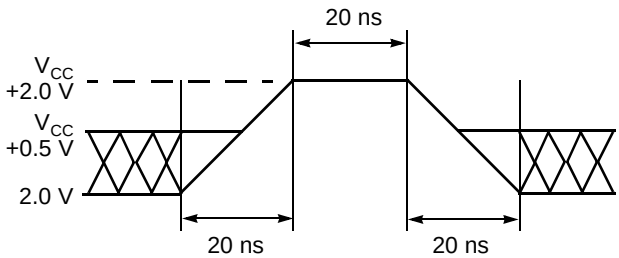


Figure 9. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –30°C to +85°C

V_{CC}f/V_{CC}s Supply Voltages

V_{CC}f/V_{CC}s for standard voltage range . . 2.7 V to 3.1 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

FLASH DC CHARACTERISTICS

CMOS Compatible

Parameter Symbol	Parameter Description	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	RESET# Input Load Current	$V_{CC} = V_{CC\ max}$; RESET# = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\ max}$= 12.5 V				35	µA
I_{LIA}	ACC Input Leakage Current	$V_{CC} = V_{CC\ max}$, WP#/ACC = $V_{ACC\ max}$				35	µA
$I_{CC1}f$	Flash V_{CC} Active Read Current (Notes 1, 2)	CE#f = V_{IL}, OE# = V_{IH}, Byte Mode	5 MHz		10	16	mA
			1 MHz		2	4	
		CE#f = V_{IL}, OE# = V_{IH}, Word Mode	5 MHz		10	16	
			1 MHz		2	4	
$I_{CC2}f$	Flash V_{CC} Active Write Current (Notes 2, 3)	CE#f = V_{IL}, OE# = V_{IH}, WE# = V_{IL}			15	30	mA
$I_{CC3}f$	Flash V_{CC} Standby Current 2 (Note 6)	$V_{CC}f = V_{CC\ max}$, CE#f, RESET#, WP#/ACC = $V_{CC}f \pm 0.3$ V			0.2	5	µA
$I_{CC4}f$	Flash V_{CC} Reset Current 2 (Note 6)	$V_{CC}f = V_{CC\ max}$, RESET# = $V_{SS} \pm 0.3$ V, WP#/ACC = $V_{CC}f \pm 0.3$ V			0.2	5	µA
$I_{CC5}f$	Flash V_{CC} Current Automatic Sleep Mode (Notes 2, 4, 6)	$V_{CC}f = V_{CC\ max}$, $V_{IH} = V_{CC} \pm 0.3$ V; $V_{IL} = V_{SS} \pm 0.3$ V			0.2	5	µA
$I_{CC6}f$	Flash V_{CC} Active Read-While-Program Current (Notes 1, 2)	CE#f = V_{IL}, OE# = V_{IH}	Byte		21	45	mA
			Word		21	45	
$I_{CC7}f$	Flash V_{CC} Active Read-While-Erase Current (Notes 1, 2)	CE#f = V_{IL}, OE# = V_{IH}	Byte		21	45	mA
			Word		21	45	
$I_{CC8}f$	Flash V_{CC} Active Program-While-Erase-Suspended Current (Notes 2, 5)	CE#f = V_{IL}, OE#f = V_{IH}			17	35	mA
V_{IL}	Input Low Voltage			–0.2		0.8	V
V_{IH}	Input High Voltage			2.4		V_{CC} + 0.2	V
V_{HH}	Voltage for WP#/ACC Program Acceleration and Sector Protection/Unprotection			8.5		9.5	V
V_{ID}	Voltage for Sector Protection, Autoselect and Temporary Sector Unprotect			11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC}f = V_{CC}s = V_{CC\ min}$				0.45	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC}f = V_{CC}s = V_{CC\ min}$		0.85 x V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min}$		V_{CC}–0.4			
V_{LKO}	Flash Low V_{CC} Lock-Out Voltage 5			2.3		2.5	V

Notes:

1. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
2. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
3. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
4. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
5. *Not 100% tested.*
6. *Typical and maximum specification are double for MCP because there are 2 flash components.*

SRAM DC AND OPERATING CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	–1.0		1.0	µA
I_{LO}	Output Leakage Current	CE#1s = V_{IH}, CE2s = V_{IL} or OE# = V_{IH} or WE# = V_{IL}, V_{IO}= V_{SS} to V_{CC}	–1.0		1.0	µA
I_{CC}	Operating Power Supply Current	I_{IO} = 0 mA, CE#1s = V_{IL}, CE2s = WE# = V_{IH}, V_{IN} = V_{IH} or V_{IL}			3	mA
$I_{CC1}s$	Average Operating Current	Cycle time = 1 µs, 100% duty, I_{IO} = 0 mA, CE#1s ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V			3	mA
$I_{CC2}s$	Average Operating Current	Cycle time = Min., I_{IO} = 0 mA, 100% duty, CE#1s = V_{IL}, CE2s = V_{IH}, V_{IN} = V_{IL} = or V_{IH}			30	mA
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1.0 mA	2.4			V
I_{SB}	Standby Current (TTL)	CE#1s = V_{IH}, CE2 = V_{IL}, Other inputs = V_{IH} or V_{IL}			0.3	mA
I_{SB1}	Standby Current (CMOS)	CE#1s ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V (CE#1s controlled) or CE2 ≤ 0.2 V (CE2s controlled), CIOs = V_{SS} or V_{CC}, Other input = 0 ~ V_{CC}			15	µA
V_{IL}	Input Low Voltage		–0.2 (Note 1)		0.6	
V_{IH}	Input High Voltage		2.2			V_{CC}+0.2 (Note 2)

Notes:

1. *Undershoot: –1.0 V in case of pulse width* ≤ 20 ns.
2. *V_{CC}+1.0 V in case of pulse width* ≤ 20 ns.
3. *Undershoot and overshoot are samples and not 100% tested.*

FCRAM DC CHARACTERISTICS

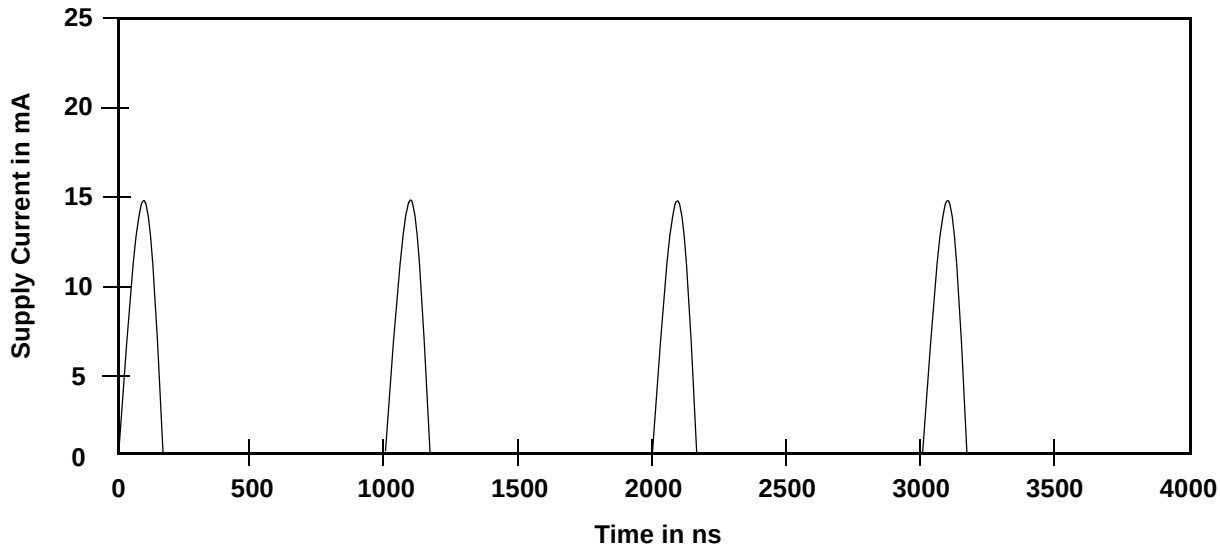
Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		–1.0	+1.0	µA
Output Leakage Current	I_{LO}	V_{OUT}= V_{SS} to V_{CC}, Output Disable		–1.0	+1.0	µA
Output High Voltage Level	V_{OH}	V_{CC}= V_{CC}, I_{OH}= –0.5mA		2.2	–	V
Output Low Voltage Level	V_{OL}	I_{OL}= 1mA		–	0.4	V
V_{CC} Power Down Current	I_{DDPS}	V_{CC}= V_{CC} max, V_{IN}= V_{IH} or V_{IL}, CE2 ≤ 0.2V	SLEEP	–	10	µA
	I_{DDPN}		NAP	–	65	µA
	I_{DDP16}		16M Partial	–	85	µA
V_{CC} Standby Current	I_{DDS}	V_{CC}= V_{CC} max, V_{IN}= V_{IH} or V_{IL} CE1= CE2= V_{IH}		–	1.5	mA
	I_{DDS1}	V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CC}–0.2V, CE1= CE2 ≥ V_{DD}–0.2V		–	150	µA
V_{CC} Active Current	I_{DDA1}	V_{IN} = V_{IH} or V_{IL} CE1= V_{IL} and CE2= V_{IH}, I_{OUT}= 0mA	T_{RC}/T_{WC}= minimum	–	25	mA
	I_{DDA2}		T_{RC}/T_{WC}= 1 µA	–	3	mA
Input Low Voltage (Note 4)	V_{IL}			–0.3	0.5	V
Input High Voltage (Note 5)	V_{IH}			2.2		V

Note:

1. *All voltages are referenced to V_{SS}.*
2. *DC Characteristics are measured after the following POWER-UP timing.*
3. *I_{OUT} depends on the output load conditions.*
4. *Minimum DC voltage on input or I/O pin are –0.3 V. During voltage transitions, inputs may negative overshoot V_{SS} to –1.0 V for periods of up to 5 ns.*
5. *Maximum DC voltage or Input and I/O pin are V_{DD}+0.3 V. During voltage transitions, input may positive overshoot to V_{DD}+1.0 V for periods of up to 5 ns.*

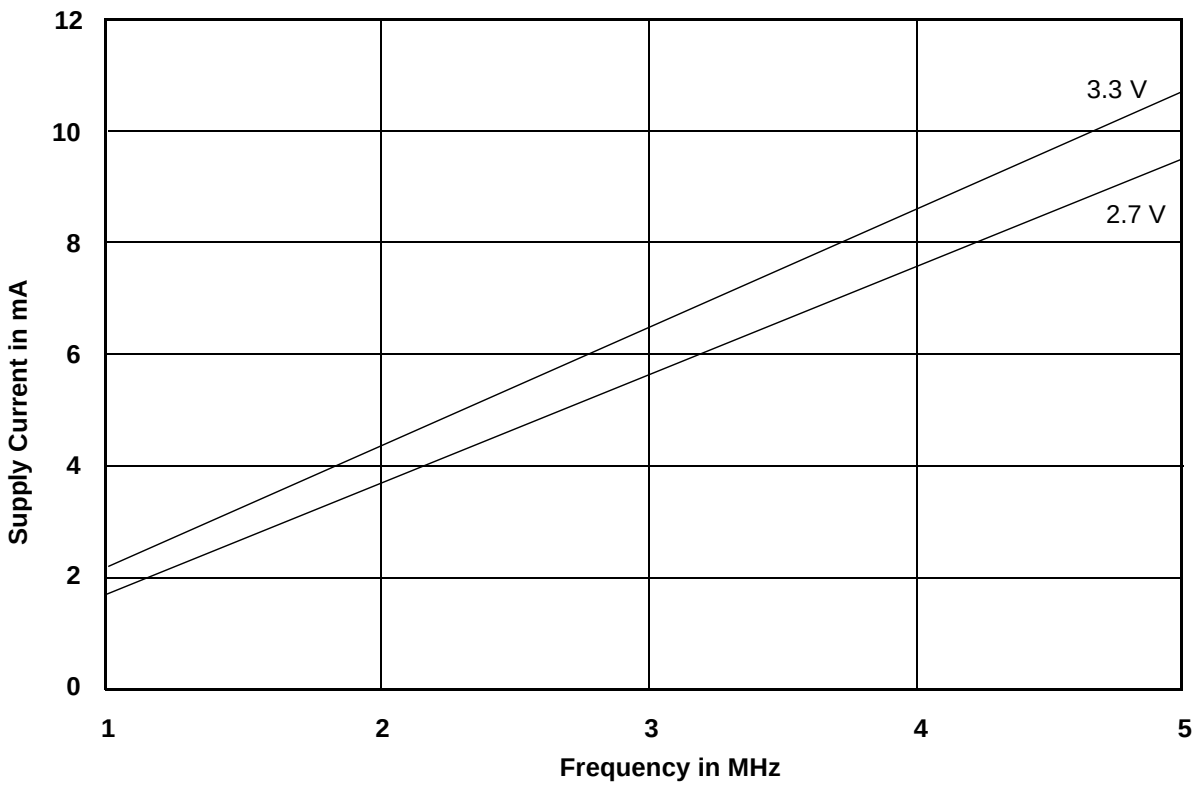
DC CHARACTERISTICS

Zero-Power Flash



Note: *Addresses are switching at 1 MHz*

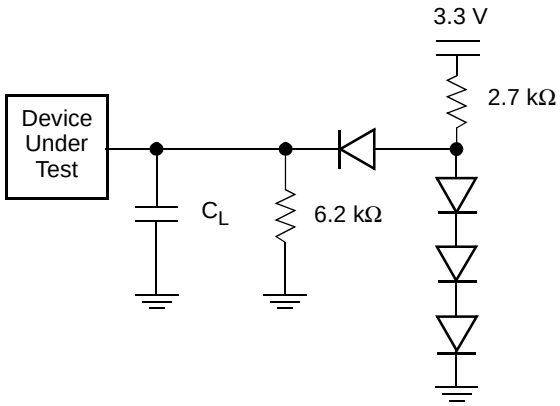
Figure 10. I_{CC1} Current vs. Time (Showing Active and Automatic Sleep Currents)



Note: *T = 25 °C*

Figure 11. Typical I_{CC1} vs. Frequency

MCP TEST CONDITIONS



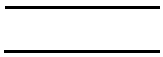
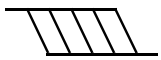
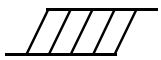
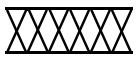
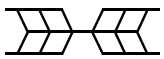
Note: *Diodes are IN3064 or equivalent*

Figure 12. Test Setup

Table 15. Test Specifications

Test Condition	70, 85	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don’t Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

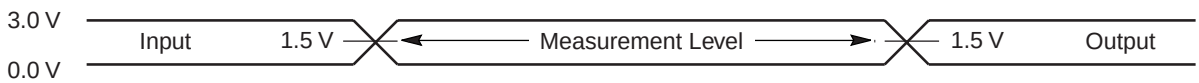


Figure 13. Input Waveforms and Measurement Levels

MCP AC CHARACTERISTICS

CE#s Timing

Parameter		Description	Test Setup		All Speeds	Unit
JEDEC	Std					
—	t_{CCR}	CE#s Recover Time	—	Min	0	ns

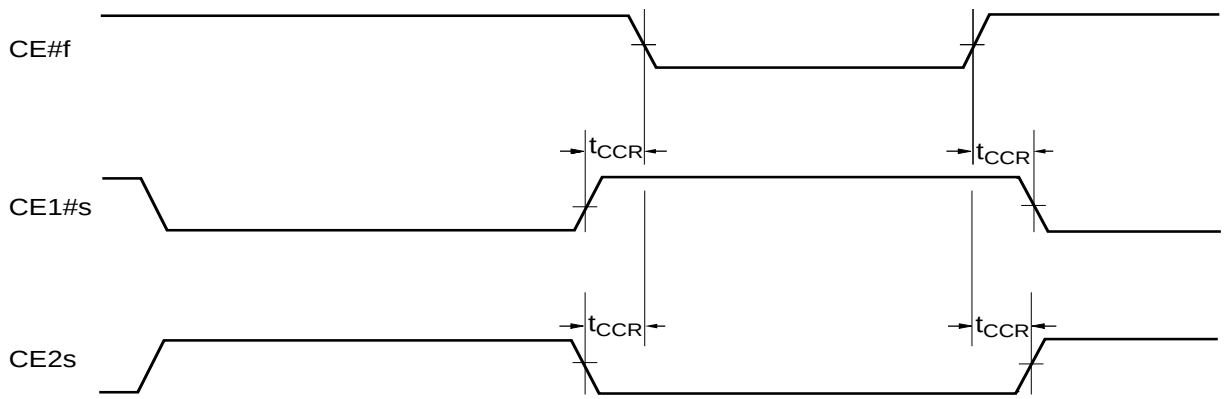


Figure 14. Timing Diagram for Alternating Between SRAM to Flash or FCRAM

FLASH AC CHARACTERISTICS

Flash Read-Only Operations

Parameter		Description		Test Setup		Speed		Unit
JEDEC	Std.					70	85	
t_{AVAV}	t_{RC}	Read Cycle Time 1			Min	70	85	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#f, OE# = V_{IL}	Max	70	85	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	70	85	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	40	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Notes 1, 3)			Max	16		ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Notes 1, 3)			Max	16		ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE#f or OE#, Whichever Occurs First			Min	0		ns
	t_{OEH}	Output Enable Hold Time 1	Read		Min	0		ns
			Toggle and Data# Polling		Min	10		ns

Notes:

1. *Not 100% tested.*
2. *See Figure 12 and Table 15 for test specifications*
3. *Measurements performed by placing a 50Ω termination on the data pin with a bias of $V_{CC}/2$. The time from OE# high to the data bus driven to $V_{CC}/2$ is taken as t_{DF}*

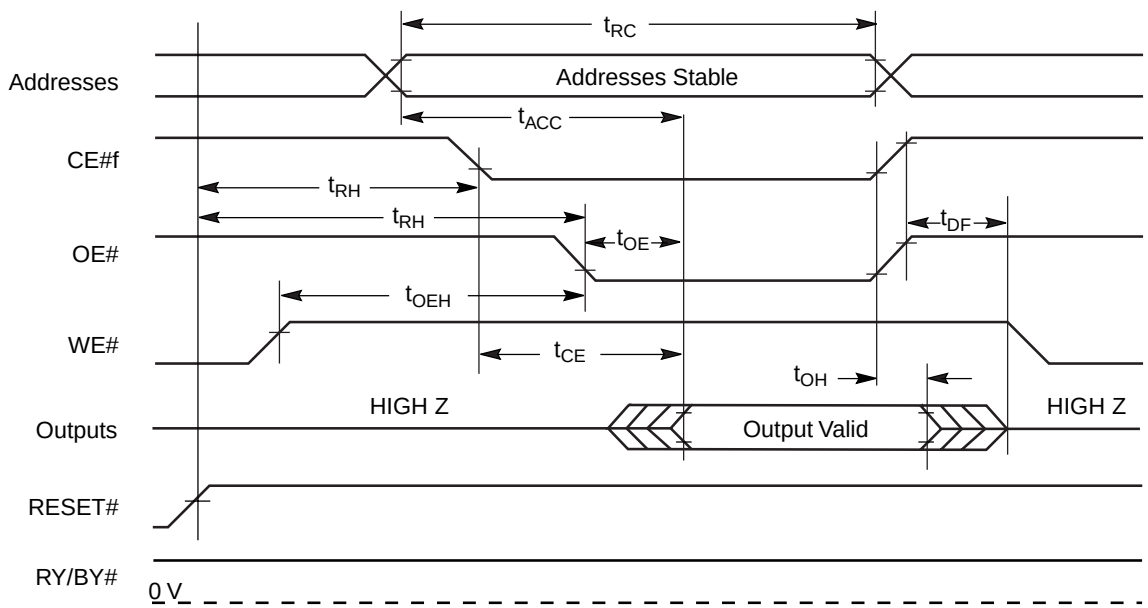


Figure 15. Read Operation Timings

FLASH AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{Ready}	RESET# Pin Low (During Embedded Algorithms) to Read Mode (See Note)	Max	20	µs
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs
	t_{RB}	RY/BY# Recovery Time	Min	0	ns

Note: *Not 100% tested.*

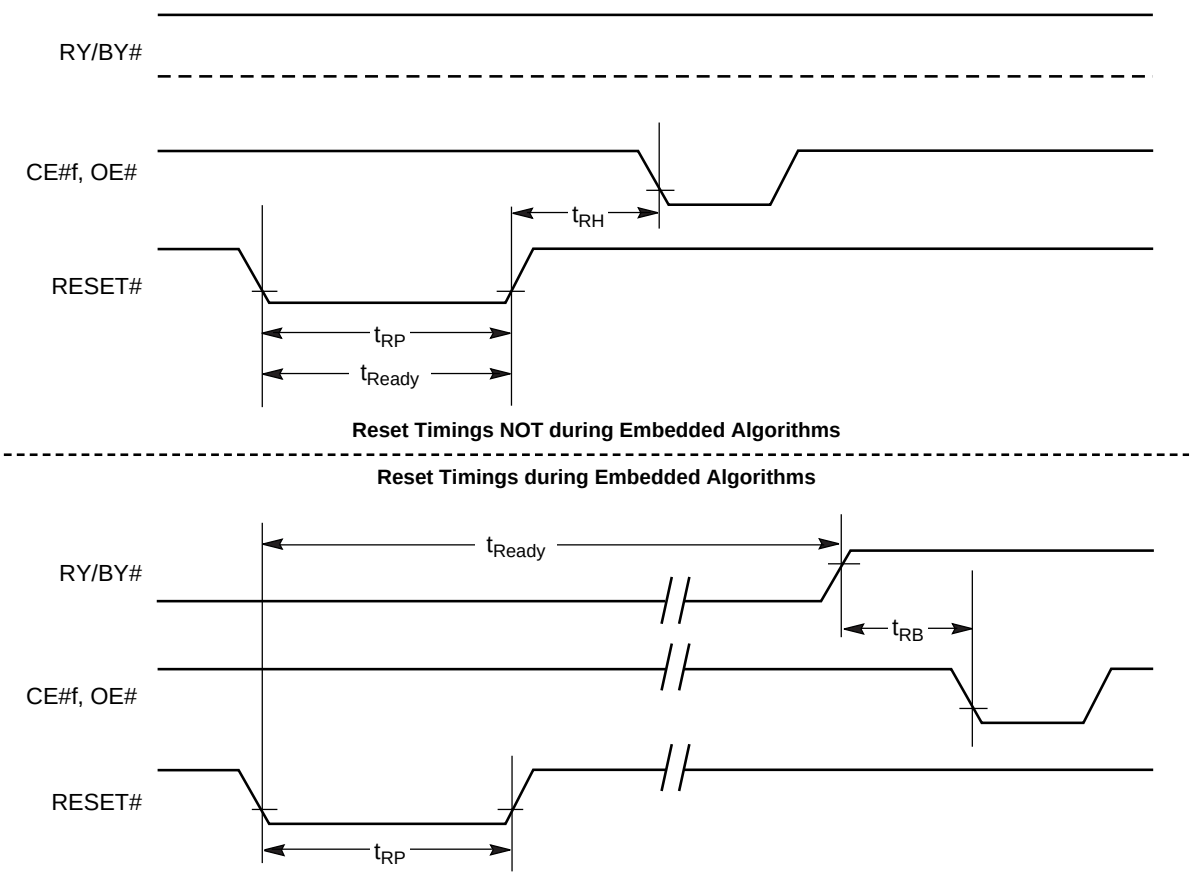


Figure 16. Reset Timings

FLASH AC CHARACTERISTICS

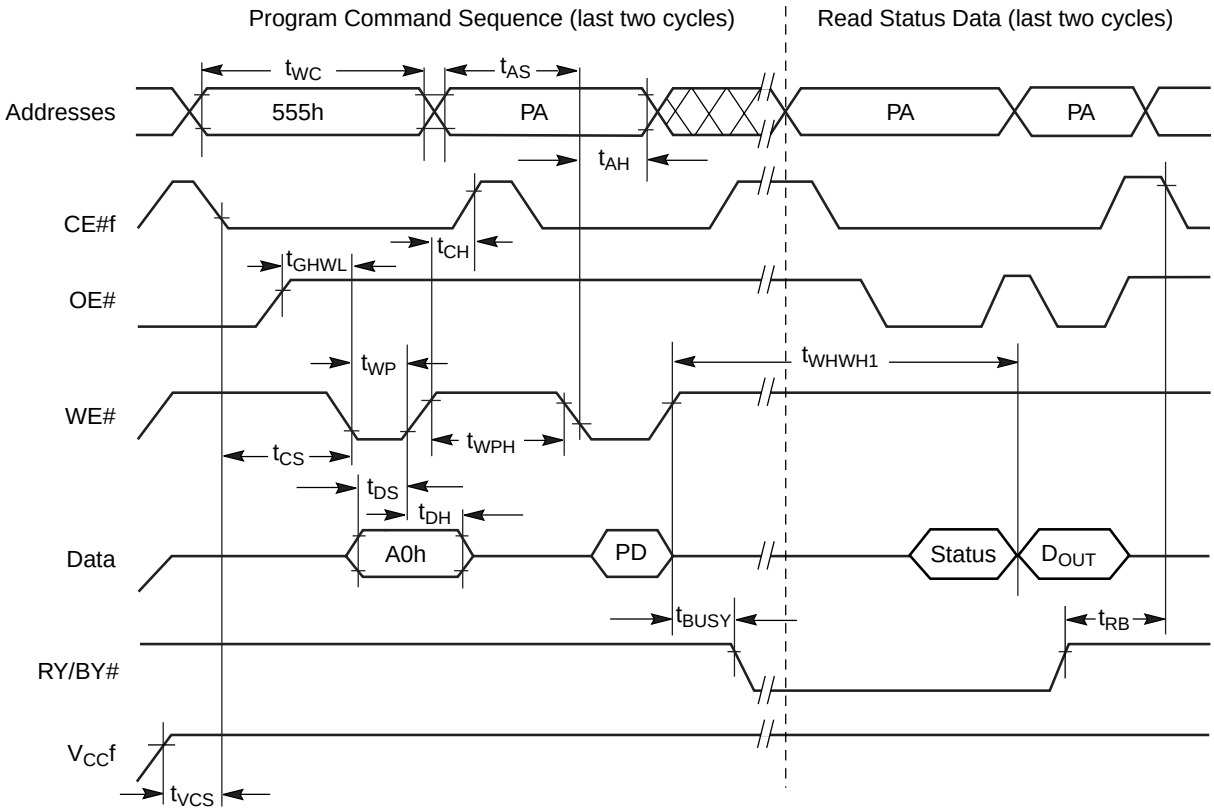
Erase and Program Operations

Parameter		Description			Speed		Unit
JEDEC	Std				70	85	
t_{AVAV}	t_{WC}	Write Cycle Time 1		Min	70	85	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15		ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	40	45	ns
	t_{AHT}	Address Hold Time From CE#f or OE# high during toggle bit polling		Min	0		ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	40	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0		ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20		ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time (CE#f to WE#)		Min	0		ns
t_{ELWL}	t_{CS}	CE#f Setup Time		Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time (CE#f to WE#)		Min	0		ns
t_{WHEH}	t_{CH}	CE#f Hold Time		Min	0		ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	30	35	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30		ns
	$t_{SR/W}$	Latency Between Read and Write Operations		Min	0		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation 2	Byte	Typ	5		µs
			Word	Typ	7		
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte 2		Typ	4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation 2		Typ	0.4		sec
	t_{VCS}	V_{CC} Setup Time 1		Min	50		µs
	t_{RB}	Write Recovery Time from RY/BY#		Min	0		ns
	t_{BUSY}	Program/Erase Valid to RY/BY# Delay		Max	90		ns

Notes:

1. *Not 100% tested.*
2. *See the "Flash Erase And Programming Performance" section for more information.*

FLASH AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 17. Program Operation Timings

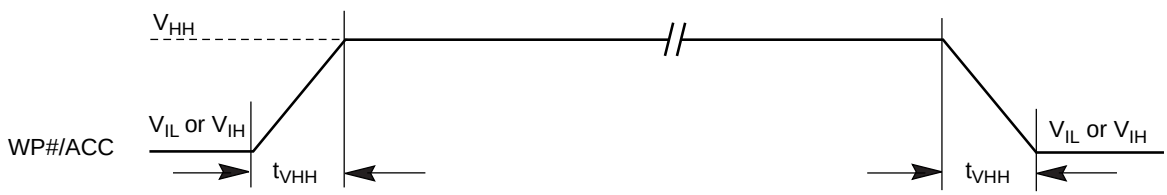
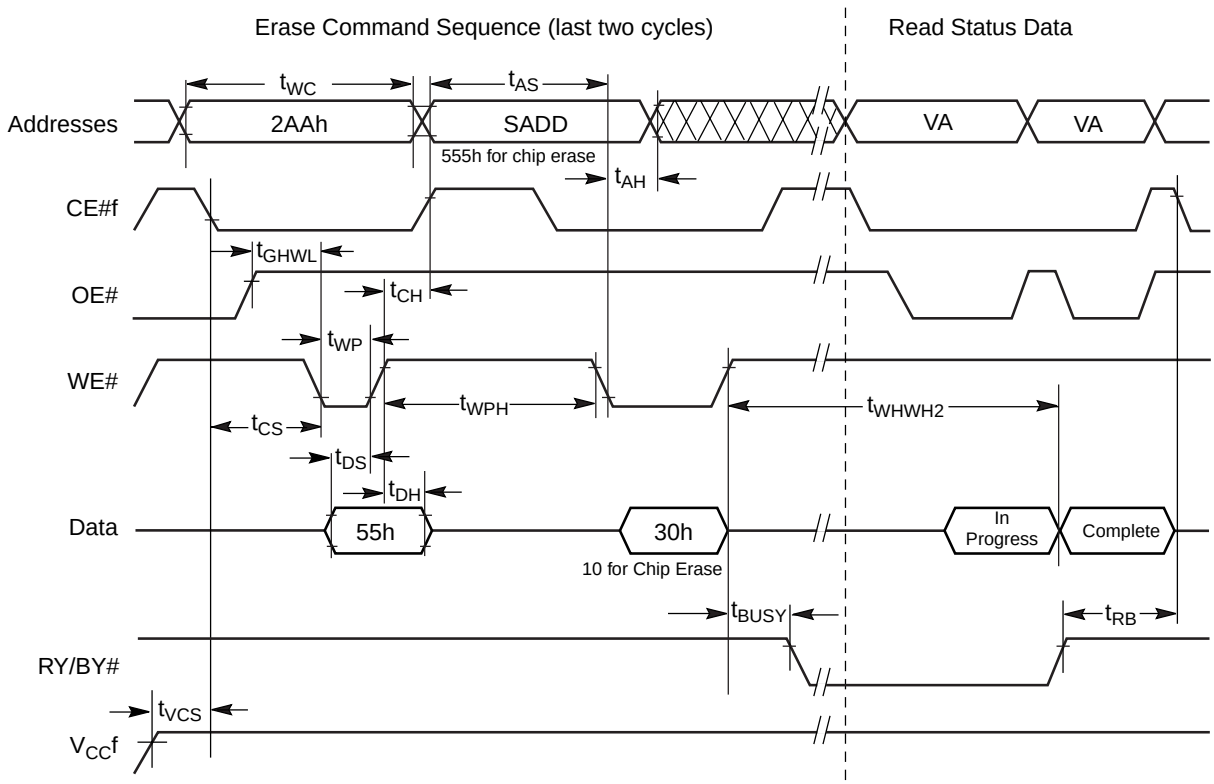


Figure 18. Accelerated Program Timing Diagram

FLASH AC CHARACTERISTICS



Notes:

1. *SADD = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Flash Write Operation Status".*
2. *These waveforms are for the word mode.*

Figure 19. Chip/Sector Erase Operation Timings

FLASH AC CHARACTERISTICS

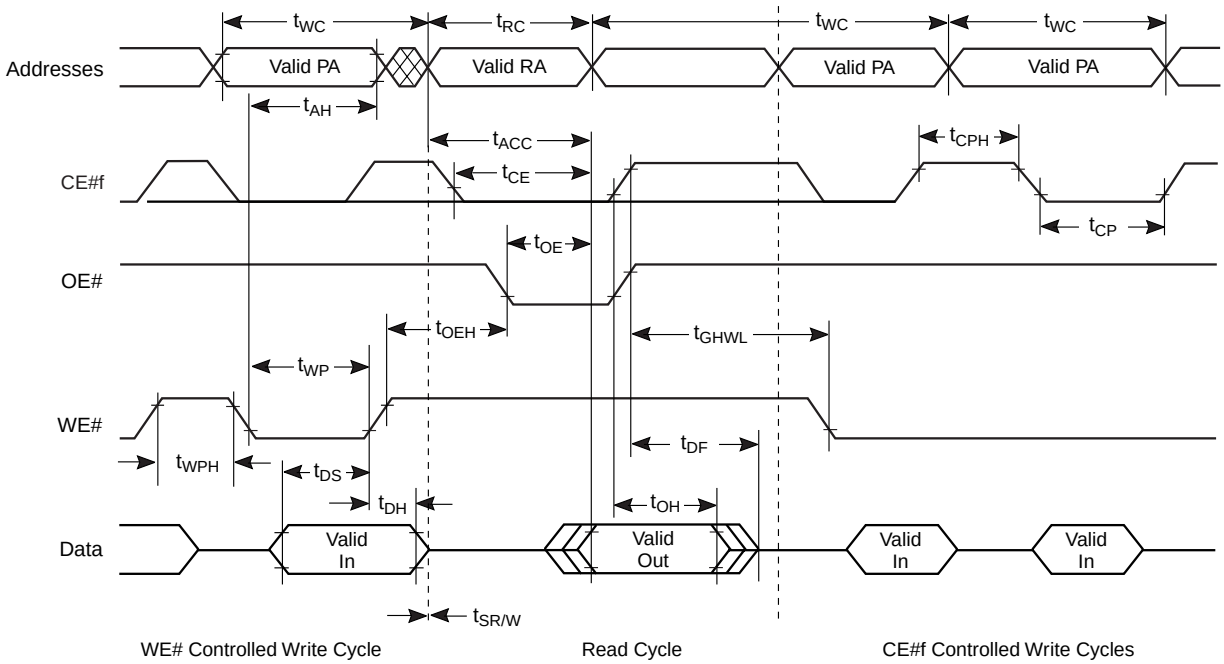
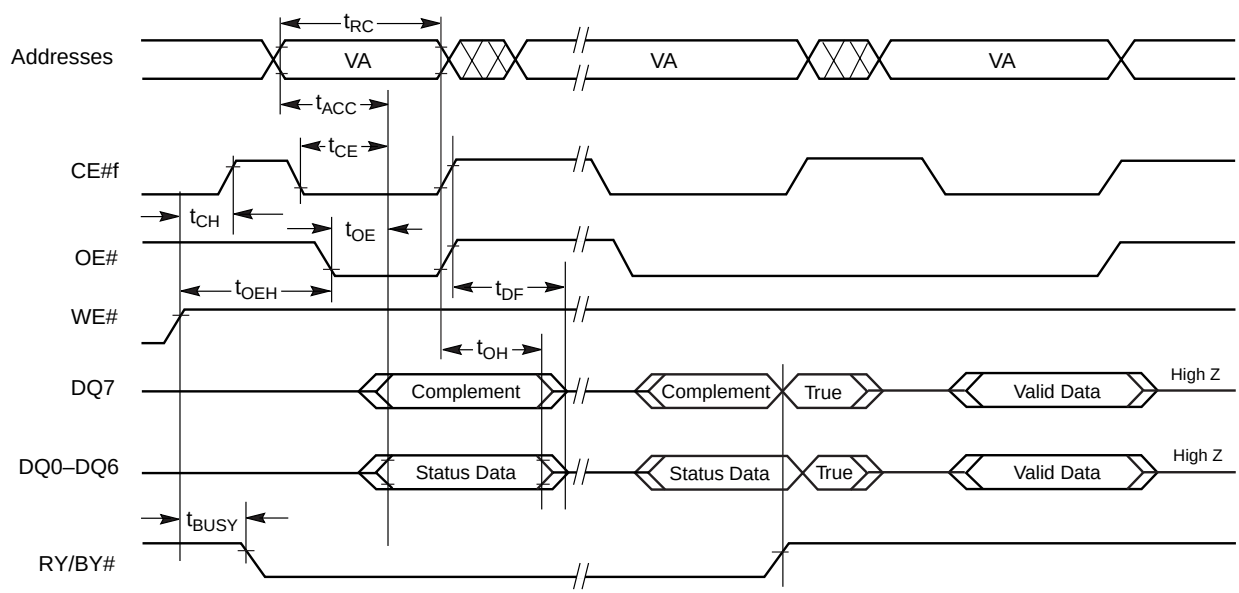


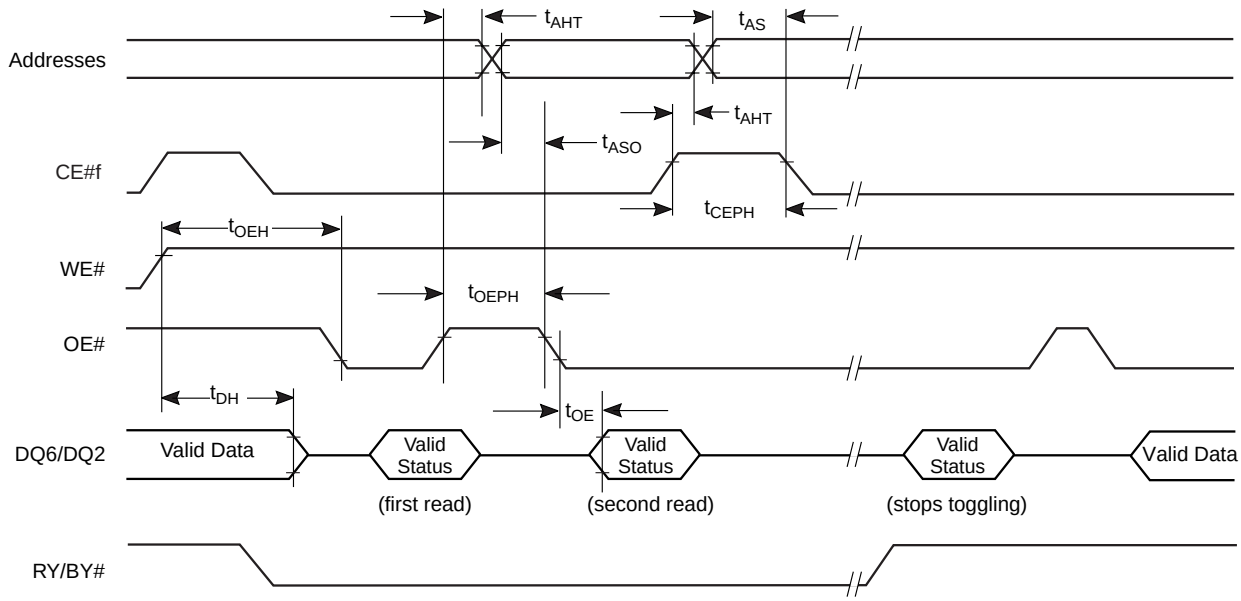
Figure 20. Back-to-back Read/Write Cycle Timings



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

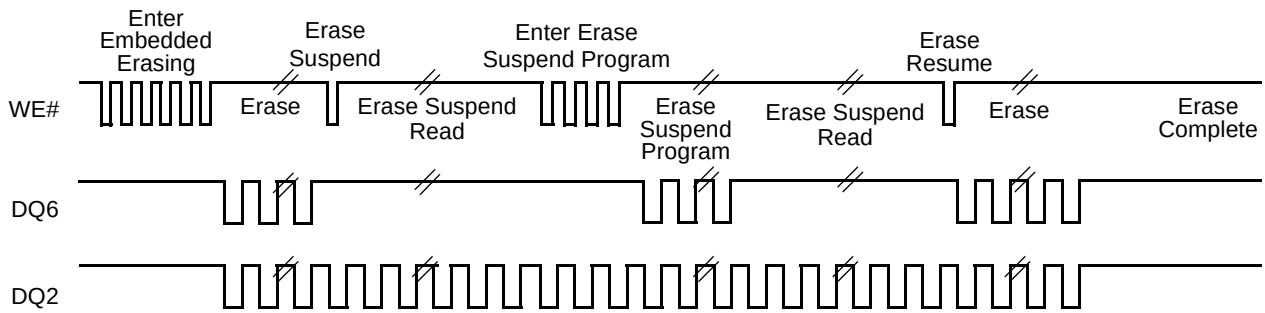
Figure 21. Data# Polling Timings (During Embedded Algorithms)

FLASH AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.*

Figure 22. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE#f to toggle DQ2 and DQ6.*

Figure 23. DQ2 vs. DQ6

FLASH AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter		Description		All Speed Options	Unit
JEDEC	Std				
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{VHH}	V_{HH} Rise and Fall Time (See Note)	Min	250	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs
	t_{RRB}	RESET# Hold Time from RY/BY# High for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

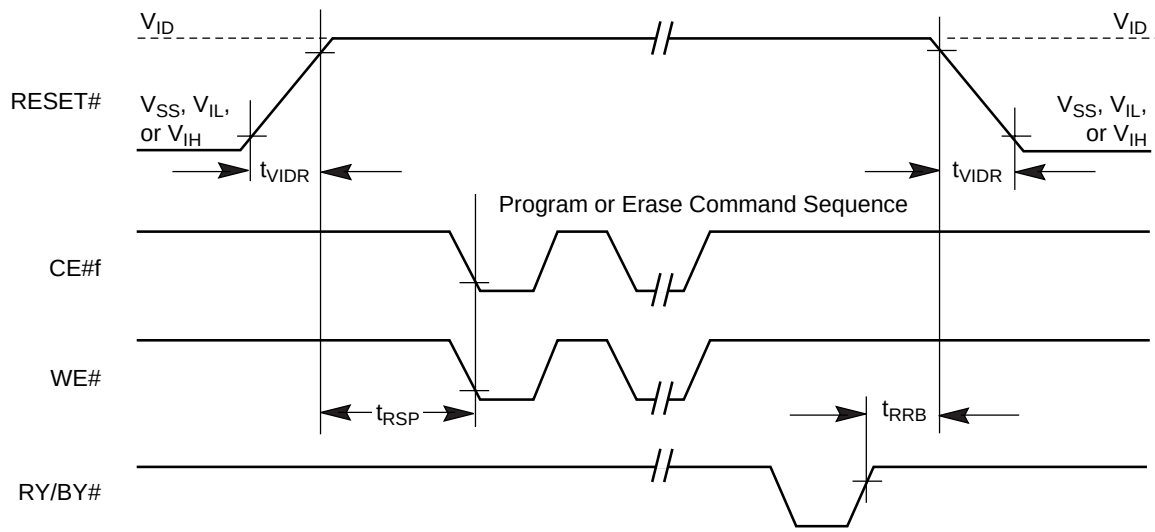
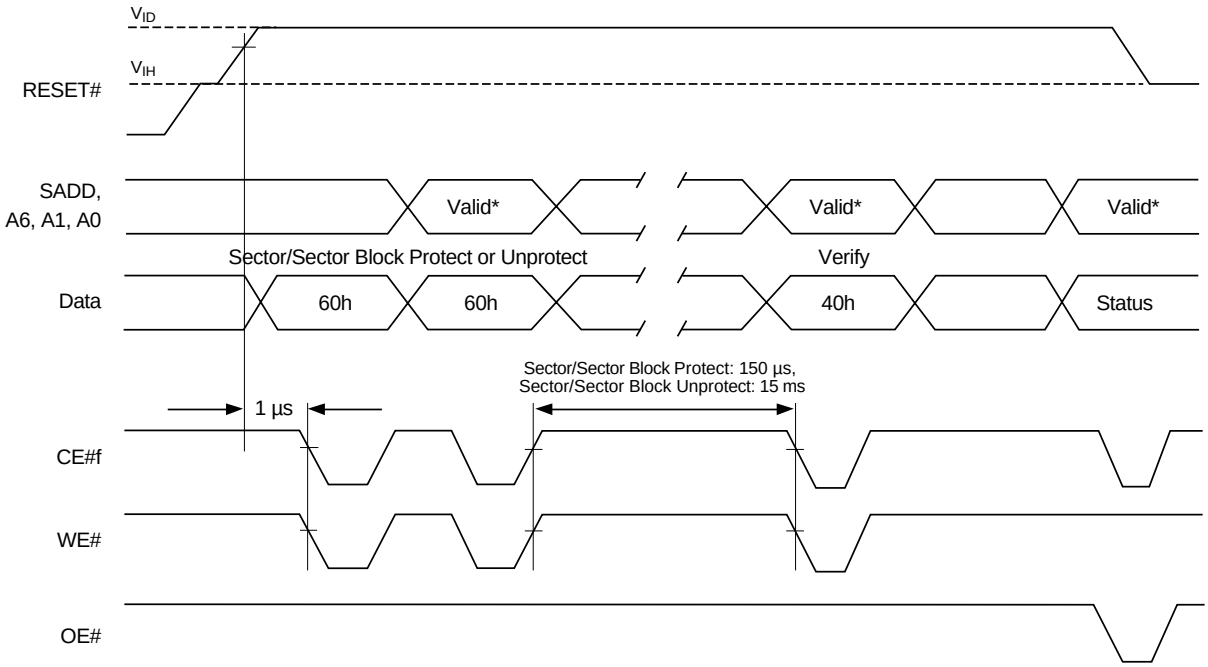


Figure 24. Temporary Sector Unprotect Timing Diagram

FLASH AC CHARACTERISTICS



** For sector protect, A6 = 0, A1 = 1, A0 = 0. For sector unprotect, A6 = 1, A1 = 1, A0 = 0, SADD = Sector Address.*

Figure 25. Sector/Sector Block Protect and Unprotect Timing Diagram

FLASH AC CHARACTERISTICS

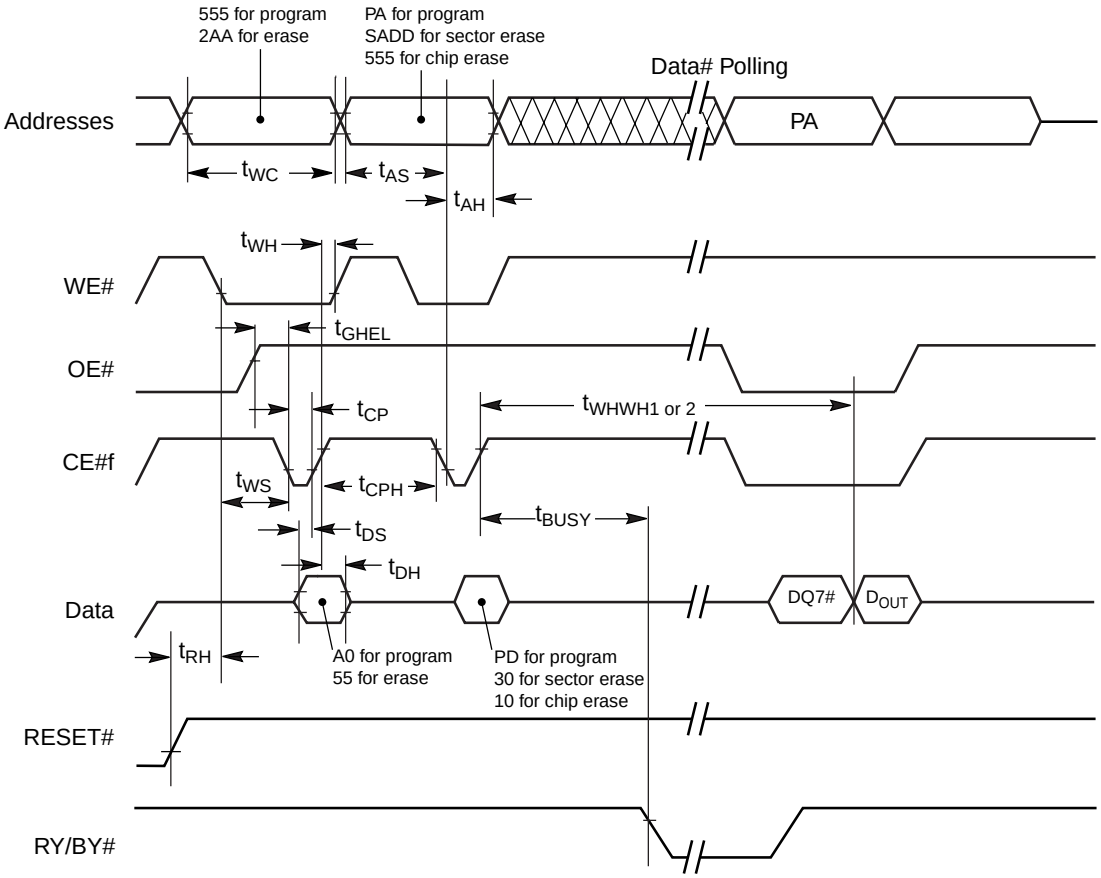
Alternate CE#f Controlled Erase and Program Operations

Parameter		Description			Speed		Unit
JEDEC	Std				70	85	
t_{AVAV}	t_{WC}	Write Cycle Time 1		Min	70	85	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0		ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	40	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	40	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0		ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0		ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0		ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0		ns
t_{ELEH}	t_{CP}	CE#f Pulse Width		Min	40	45	ns
t_{EHEL}	t_{CPH}	CE#f Pulse Width High		Min	30		ns
t_{WHWH1}	t_{WHWH1}	Programming Operation 2	Byte	Typ	5		µs
			Word	Typ	7		
t_{WHWH1}	t_{WHWH1}	Accelerated Programming Operation, Word or Byte 2		Typ	4		µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation 2		Typ	0.4		sec

Notes:

1. *Not 100% tested.*
2. *See the "Flash Erase And Programming Performance" section for more information.*

FLASH AC CHARACTERISTICS



Notes:

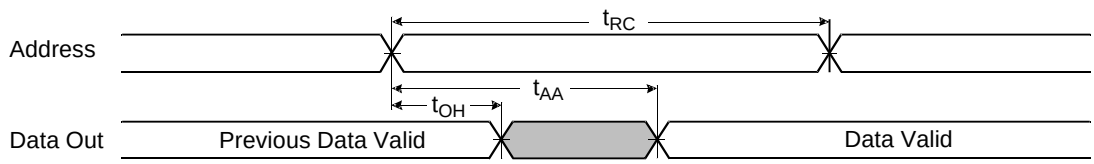
1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SADD = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*
4. *Waveforms are for the word mode.*

Figure 26. Flash Alternate CE#f Controlled Write (Erase/Program) Operation Timings

SRAM AC CHARACTERISTICS

Read Cycle

Parameter Symbol	Description		Speed		Unit
			70	85	
t_{RC}	Read Cycle Time	Min	70	85	ns
t_{AA}	Address Access Time	Max	70	85	ns
t_{CO1}, t_{CO2}	Chip Enable to Output	Max	70	85	ns
t_{OE}	Output Enable Access Time	Max	35	45	ns
t_{BA}	LB#s, UB#s to Access Time	Max	70	85	ns
t_{LZ1}, t_{LZ2}	Chip Enable (CE#1s Low and CE2s High) to Low-Z Output	Min	10		ns
t_{BLZ}	UB#, LB# Enable to Low-Z Output	Min	10		ns
t_{OLZ}	Output Enable to Low-Z Output	Min	5		ns
t_{HZ1}, t_{HZ2}	Chip Disable to High-Z Output	Max	25		ns
t_{BHZ}	UB#s, LB#s Disable to High-Z Output	Max	25		ns
t_{OHZ}	Output Disable to High-Z Output	Max	25		ns
t_{OH}	Output Data Hold from Address Change	Min	10		ns



Note: *CE#1s = OE# = V_{IL}, CE2s = WE# = V_{IH}, UB#s and/or LB#s = V_{IL}*

Figure 27. SRAM Read Cycle—Address Controlled

SRAM AC CHARACTERISTICS

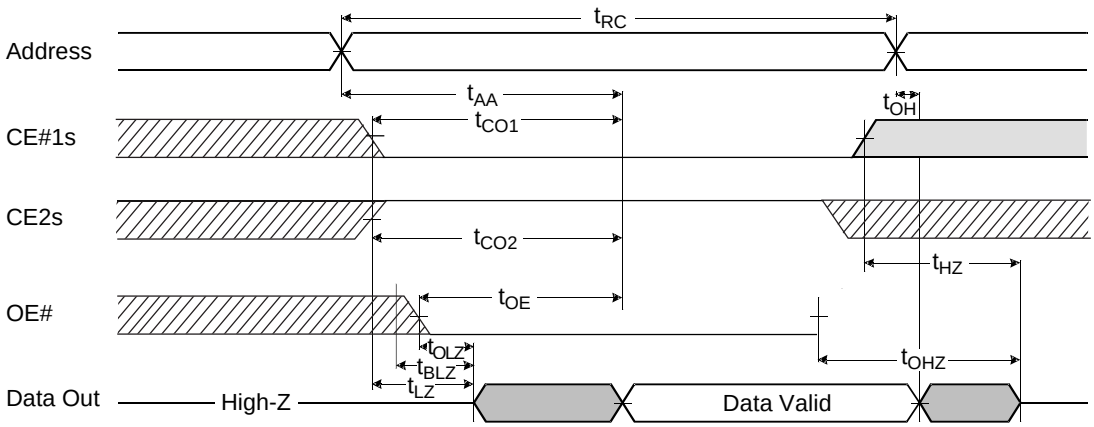


Figure 28. SRAM Read Cycle

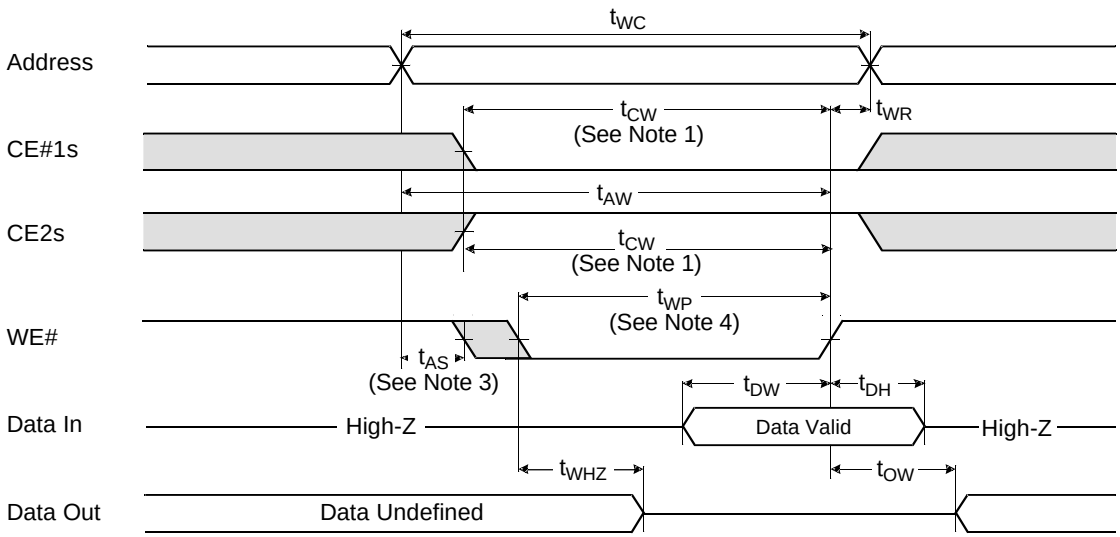
Notes:

1. *WE# = V_{IH}, if CIOs is low, ignore UB#s/LB#s timing.*
2. *t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
3. *At any given temperature and voltage condition, t_{HZ} (Max.) is less than t_{LZ} (Min.) both for a given device and from device to device interconnection.*

SRAM AC CHARACTERISTICS

Write Cycle

Parameter Symbol	Description		Speed		Unit
			70	85	
t_{WC}	Write Cycle Time	Min	70	85	ns
t_{Cw}	Chip Enable to End of Write	Min	60	70	ns
t_{AS}	Address Setup Time	Min	0		ns
t_{AW}	Address Valid to End of Write	Min	60	70	ns
t_{BW}	UB#s, LB#s to End of Write	Min	60	70	ns
t_{WP}	Write Pulse Time	Min	50	60	ns
t_{WR}	Write Recovery Time	Min	0		ns
t_{WHZ}	Write to Output High-Z	Min	0		ns
		Max	20	25	
t_{DW}	Data to Write Time Overlap	Min	30	35	ns
t_{DH}	Data Hold from Write Time	Min	0		ns
t_{OW}	End Write to Output Low-Z	min	5		ns

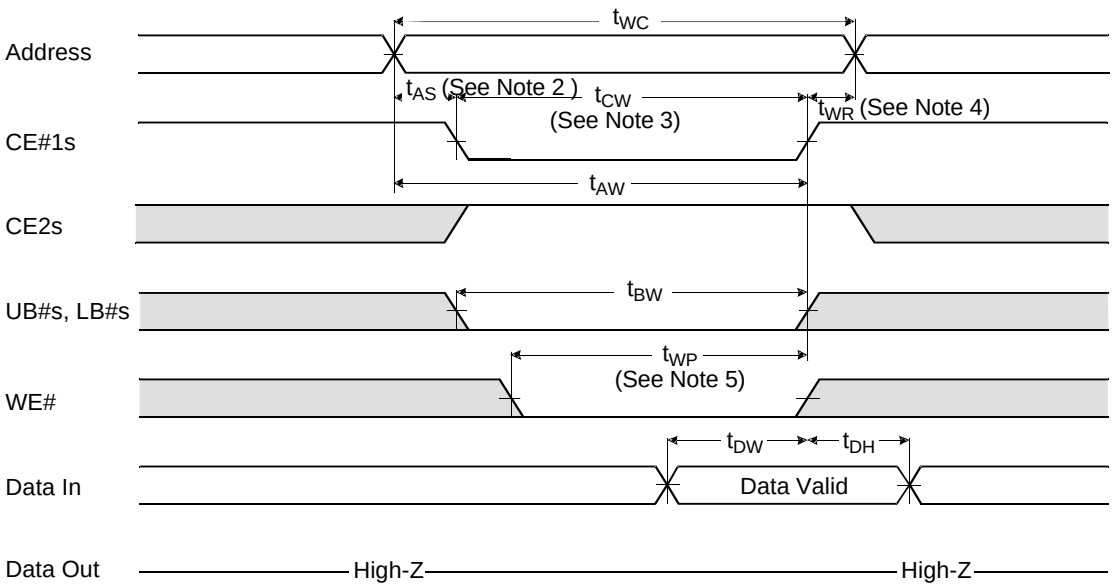


Notes:

1. *WE# controlled, if CIOs is low, ignore UB#s and LB#s timing.*
2. *t_{CW} is measured from CE#1s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE#1s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE#1s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE#1s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 29. SRAM Write Cycle—WE# Control

SRAM AC CHARACTERISTICS

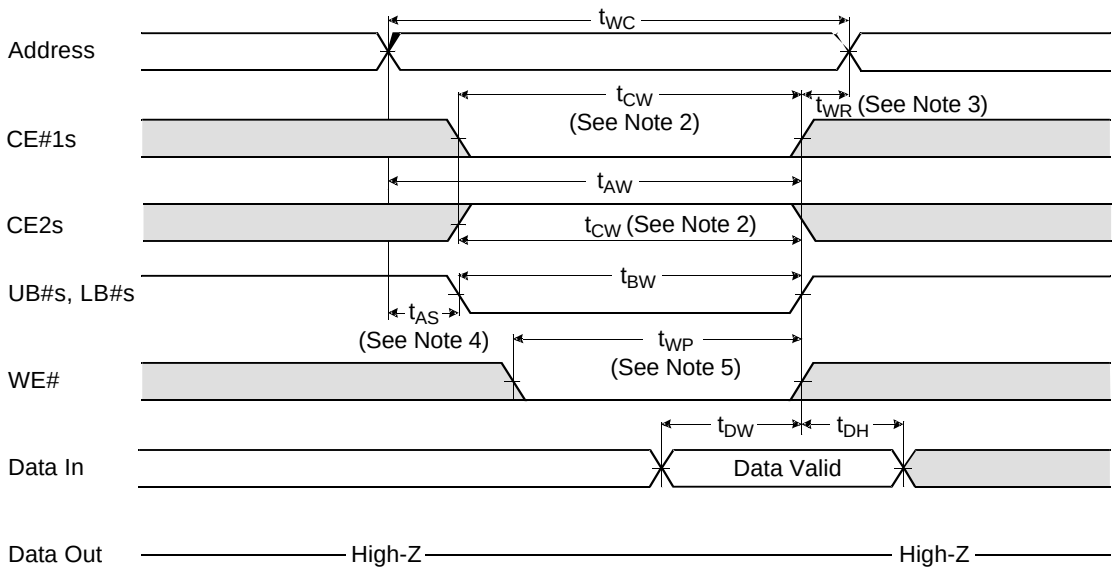


Notes:

1. *CE#1s controlled, if CIOs is low, ignore UB#s and LB#s timing.*
2. *t_{CW} is measured from CE#1s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE#1s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1s and low WE#. A write begins when CE#1s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE#1s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 30. SRAM Write Cycle—CE#1s Control

SRAM AC CHARACTERISTICS



Notes:

1. *UB#s and LB#s controlled, CIOs must be high.*
2. *t_{CW} is measured from CE#1s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE#1s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1s and low WE#. A write begins when CE#1s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE#1s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 31. SRAM Write Cycle—UB#s and LB#s Control

FCRAM AC CHARACTERISTICS

Read Operation

Parameter	Description (Notes)		Speed		Unit
			70	85	
t_{RC}	Read Cycle Time	Min	70		ns
t_{CE}	Chip Enable Access Time (1, 3)	Max	65		ns
t_{OE}	Output Enable Time (1)	Max	40		ns
t_{AA}	Address Access Time (1, 4)	Max	65		ns
t_{OH}	Output Data Hold Time (1)	Min	5		ns
t_{CLZ}	CE#1FC Low to Output Low-Z (2)	Min	5		ns
t_{OLZ}	OE Low to Output Low-Z (2)	Min	0		ns
t_{CLZ}	CE#1FC High to Output High-Z (2)	Max	20		ns
t_{OHZ}	OE High to Output High-Z (2)	Max	20		ns
t_{ASC}	Address Setup Time to CE#1FC Low (5)	Min	–5		ns
t_{ASO}	Address Setup Time to OE Low (3, 6, 7)	Min	25		ns
$t_{ASO[ABS]}$		Min	10		ns
t_{BSC}	LB#s/UB#s Setup Time to CE#1FC Low (5)	Min	–5		ns
t_{BSO}	LB#s/UB#s Setup Time to OE Low	Min	10		ns
t_{AX}	Address Invalid Time (4, 8)	Max	5		ns
t_{CLAH}	Address Hold Time from CE#1FC Low (4)	Min	70		ns
t_{OHAH}	Address Hold Time from OE Low (4, 9)	Min	45		ns
t_{CHAH}	Address Hold Time from CE#1FC High	Min	–5		ns
t_{OHAH}	Address Hold Time from OE High	Min	–5		ns
t_{CHBH}	LB#s/UB#s Hold Time from CE#1FC High	Min	–5		ns
t_{OHBH}	LB#s/UB#s Hold Time from OE High	Min	–5		ns
t_{CLOL}	CE#1FC Low to OE Low Delay Time (3, 6, 9, 10)	Min	1000		ns
		Max	25		
t_{OLCH}	OE Low to CE#1FC High Delay Time (9)	Min	45		ns
t_{CP}	CE#1FC High Pulse Width	Min	12		ns
t_{OP}	OE High Pulse Width (6, 7, 9, 10)	Min	1000		ns
		Max	25		
$t_{OP[ABS]}$		Min	12		ns

Notes:

1. *The output load is 50pF.*
2. *The output load is 5pF.*
3. *The tCE is applicable if OE is brought to Low before CE#1FC goes Low and is also applicable if actual value of both or either t_{ASO} or T_{CLOL} is shorter than specified value.*
4. *Applicable only to A14, A15 and A16 when both CE#1FC and OE are kept at Low for the address access.*
5. *Applicable if OE is brought to Low before CE#1FC goes Low.*
6. *The t_{ASO}, t_{CLOL} (min) and t_{OP} (min) are reference values when the access time is determined to t_{OE}. If actual value of each parameter is shorter that specified minimum value, t_{OE} become longer by the amount of subtracting actual value from specified minimum value. For example, if actual t_{ASO}, t_{ASO} (actual), is shorter than specified minimum value, t_{ASO} (min), during OE control access (i.e., CE#1FC stays Low), the t_{OE} become t_{OE} (max) + t_{ASO} (min)-t_{ASO} (actual).*
7. *The $t_{ASO[ABS]}$ and $t_{OP[ABS]}$ is the absolute minimum value during OE control access.*
8. *The t_{AX} is applicable when all of two addresses among A14 to A16 are switched from previous state.*
9. *If actual value of either t_{CLOL} or t_{OP} is shorter than specified minimum value, both t_{OLAH} and t_{OLCH} become t_{RC} (min)- t_{CLOL} (actual).*
10. *Maximum value is applicable if CE#1FC is kept at Low.*

FCRAM AC CHARACTERISTICS

Write Operation

Parameter	Description (Notes)		Speed		Unit
			70	85	
t_{WC}	Write Cycle Time (1)	Min	70		ns
t_{AS}	Address Setup Time (2)	Min	0		ns
		Max	65		
t_{AH}	Address Hold Time (2)	Min	35		ns
		Max	40		
t_{CS}	Address Access Time	Min	0		ns
		Max	65		
t_{CH}	CE#1FC Write Setup Time	Min	0		ns
t_{WS}	CE#1FC Write Hold Time	Min	0		ns
t_{WH}	WE# Setup Time	Min	0		ns
t_{BS}	WE# Hold Time	Min	0		ns
		Max	20		
t_{BH}	LB#s and UB#s Setup Time	Min	–5		ns
		Max	20		
t_{OES}	LB#s and US Hold Time (3)	Min	–5		ns
t_{OEH}	OE# Hold Time (3, 4, 5)	Min	25		ns
$t_{OEH[ABS]}$		Min	12		ns
t_{OHCL}	OE# High to CE#1FC Low Setup Time (6)	Min	–5		ns
t_{OHAH}	OE# High to Address Hold Time (7)	Min	–5		ns
t_{CW}	CE#1FC Write Pulse Width (1, 8)	Min	45		ns
		Max	5		
t_{WP}	WE# Write Pulse Width (1, 8)	Min	45		ns
t_{WRC}	CE#1FC Write Recovery Time (1, 9)	Min	10		ns
t_{WR}	WE# Write Recovery Time (1, 3 ,9)	Min	10		ns
t_{DS}	Data Setup Time	Min	15		ns
t_{DH}	Data Hold Time	Min	0		ns
t_{CP}	CE#1FC High Pulse (9)	Min	12		ns

Notes:

1. *Minimum value must be equal or greater than the sum of actual t_{CW} (or tWP) and tWRC (or tWR).*
2. *New write address is valid from either CE#1 or WE is bought to High.*
3. *The t_{OEH} is specified from end of t_{WC}(min). The t_{OEH} (min) is a reference value when the access time is determined by t_{OE}. If actual value, t_{OEH} (actual) is shorter than specified minimum value, t_{OE} become longer by the amount of subtracting actual value from specified minimum value.*
4. *The t_{OEH} (max) is applicable if CE#1 is kept at Low and both WE and OE# are kept at High.*
5. *The t_{OEH}[ABS] is the absolute minimum value if write cycle is terminated by WE and CE#1 stays Low*
6. *t_{OHCL} (min) must be satisfied if read operation is not performed prior to write operation. In case OE# is disabled after t_{OHCL} (min), WE Low must be asserted after tRC (min) from CE#1 Low. In other words, read operation is initiated if t_{OHCL} (min) is not satisfied.*
7. *Applicable if CE#1 stays Low after read operation.*
8. *t_{CW} and t_{WP} is applicable if write operation is initiated by CE#1 and WE, respectively.*
9. *t_{WRC} and t_{WR} is applicable if write operation is terminated by CE#1 and WE, respectively. The t_{WR} (min) can be ignored if CE#1 is brought to High together or after WE is brought to High. In such case, the t_{CP} (min) must be satisfied.*

FCRAM AC CHARACTERISTICS

Power Down and Power Down Program Parameters

Parameter	Description (Notes)		Speed		Unit
			70	85	
t_{CSP}	CE2 Low Setup for Power Down Entry	Min	10		ns
t_{C2LP}	CE2 Low Hold Time after Power Down Entry	Min	70		ns
t_{CHH}	CE#1FC High Hold Time following CE2 High after Power Down Exit [SLEEP mode only]	Min	350		µs
t_{CHHN}	CE#1FC High Hold Time following CE2 High after Power Down Exit [Except for SLEEP mode]	Min	1		µs
t_{CHS}	CE#1FC High Setup Time following CE2 High after Power Down Exit	Min	10		ns
t_{EPS}	CE#1FC High to PE Low Setup Time (1)	Min	70		ns
t_{EP}	PE Pulse Width (1)	Min	70		ns
t_{EPH}	PE High to CE#1FC Low Hold Time (1)	Min	70		ns
t_{EAS}	Address Setup Time to PE High (1)	Min	15		ns
t_{EAH}	Address Hold Time from PE High (1)	Min	0		ns

Note:

1. *Applicable to Power Down Program*

Other Timing Parameters

Parameter	Description (Notes)		Speed		Unit
			70	85	
t_{CHOX}	CE#1FC High to OE# Invalid Time for Standby Entry	Min	7		ns
t_{CHWX}	CE#1FC High to WE# Invalid Time for Standby Entry (1)	Min	7		ns
t_{C2LH}	CE2 Low Hold Time after Power-up (2)	Min	50		µs
t_{C2HL}	CE2 High Hold Time after Power-up (3)	Min	50		µs
t_{CHH}	CE#1FC High Hold Time following CE2 High after Power-up (2)	Min	350		µs
t_T	Input Transition Time (4)	Min	1		ns
		Max	25		

Notes:

1. *Some data might be written into any address location if t_{CHWX} (min) is not satisfied.*
2. *Must satisfy t_{CHH} (min) after t_{C2LH} (min).*
3. *Requires Power Down mode entry and exit after t_{C2LH}.*
4. *The Input Transition Time (t_T) at AC testing is 5n as shown in below. If actual t_T is longer than 5 ns, it may violate AC specification of some timing parameters.*

FCRAM AC CHARACTERISTICS

AC Test Conditions

Symbol	Description	Test Setup	Value	Unit
V_{IH}	Input High Level		2.3	V
V_{IL}	Input Low Level		0.4	V
V_{REF}	Input Timing Measurement Level		1.3	V
t_T	Input Transition Time	Between V_{IL} and V_{IH}	5	ns

Read Timing

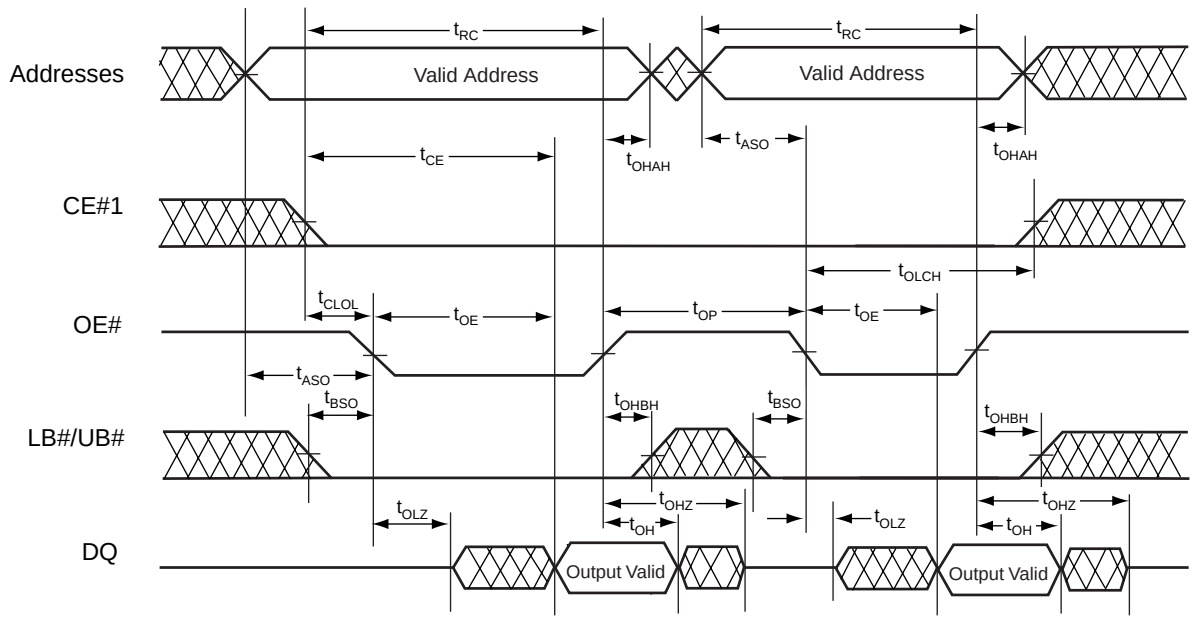


Figure 32. OE# Control Access

Notes:

1. *CE2, PE# and WE# must be High for entire read cycle.*
2. *Either or both LB# and UB# must be Low when both CE#1 and OE# are Low.*

FCRAM AC Characteristics

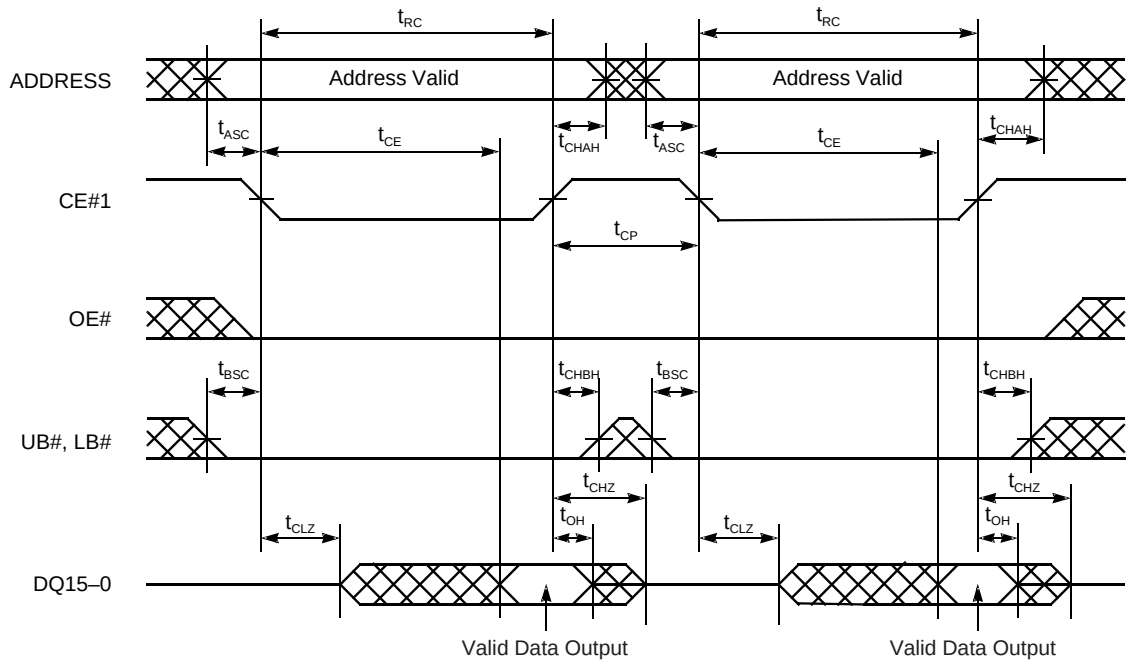


Figure 33. CE#1 Control Access

Notes:

1. *CE2, PE# and WE# must be High for entire read cycle.*
2. *Either or both LB# and UB# must be Low when both CE#1 and OE# are Low.*

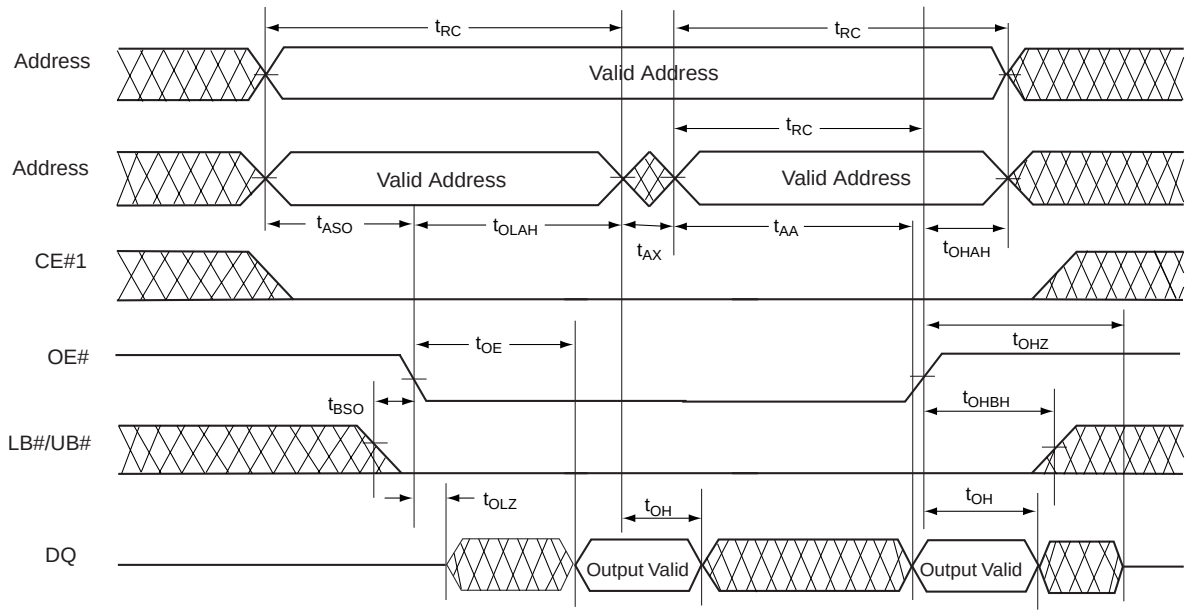


Figure 34. Address after OE# Control Access

Notes:

1. *CE2, PE# and WE# must be High for entire read cycle.*
2. *Either or both LB# and UB# must be Low when both CE#1 and OE# are Low.*

FCRAM AC CHARACTERISTICS

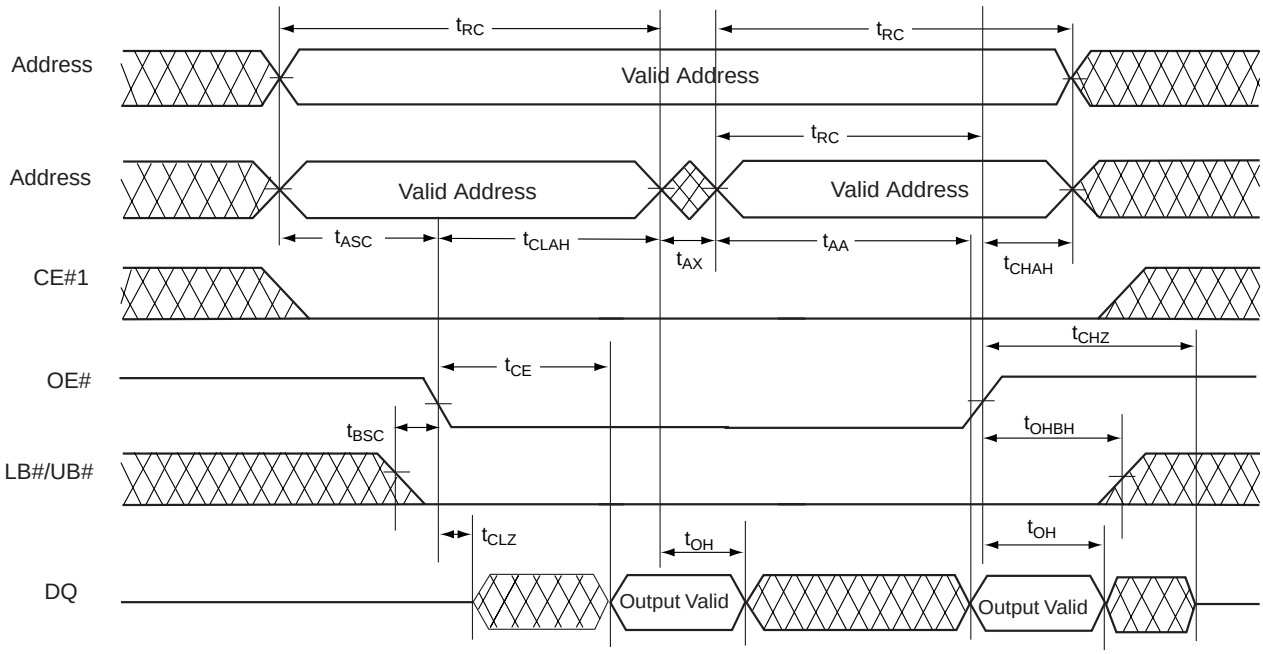


Figure 35. Address Access after CE#1 Control Access

Notes:

1. *CE2, PE# and WE# must be High for entire read cycle.*
2. *Either or both LB# and UB# must be Low when both CE#1 and OE# are Low.*

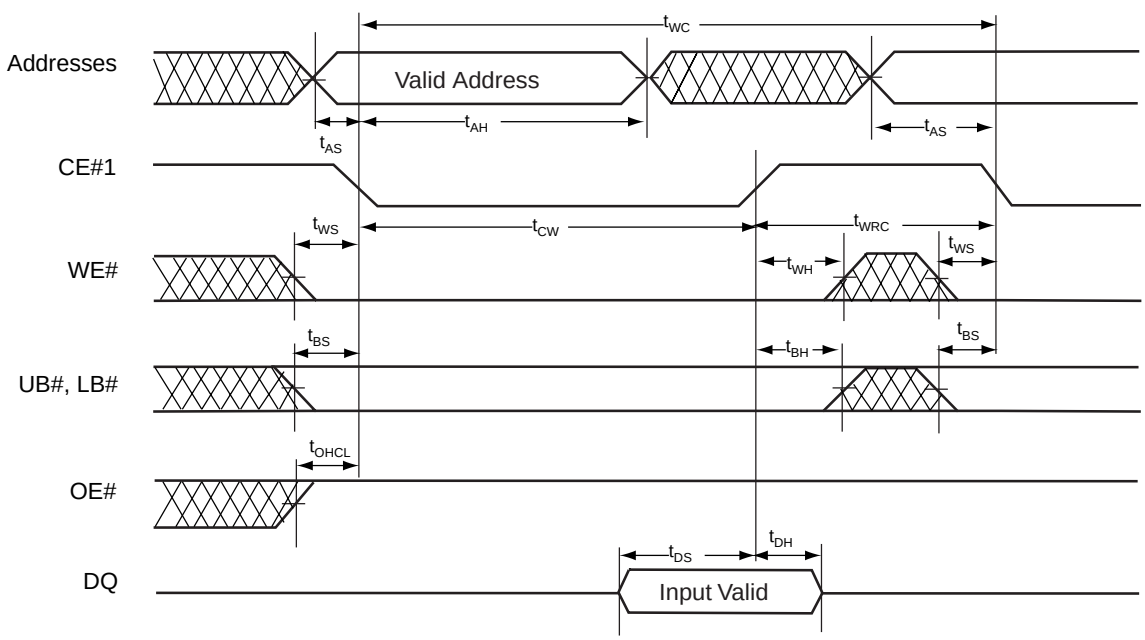


Figure 36. CE#1 Control

Notes:

1. *CE2 and PE# must be High for write cycle.*

FCRAM AC CHARACTERISTICS

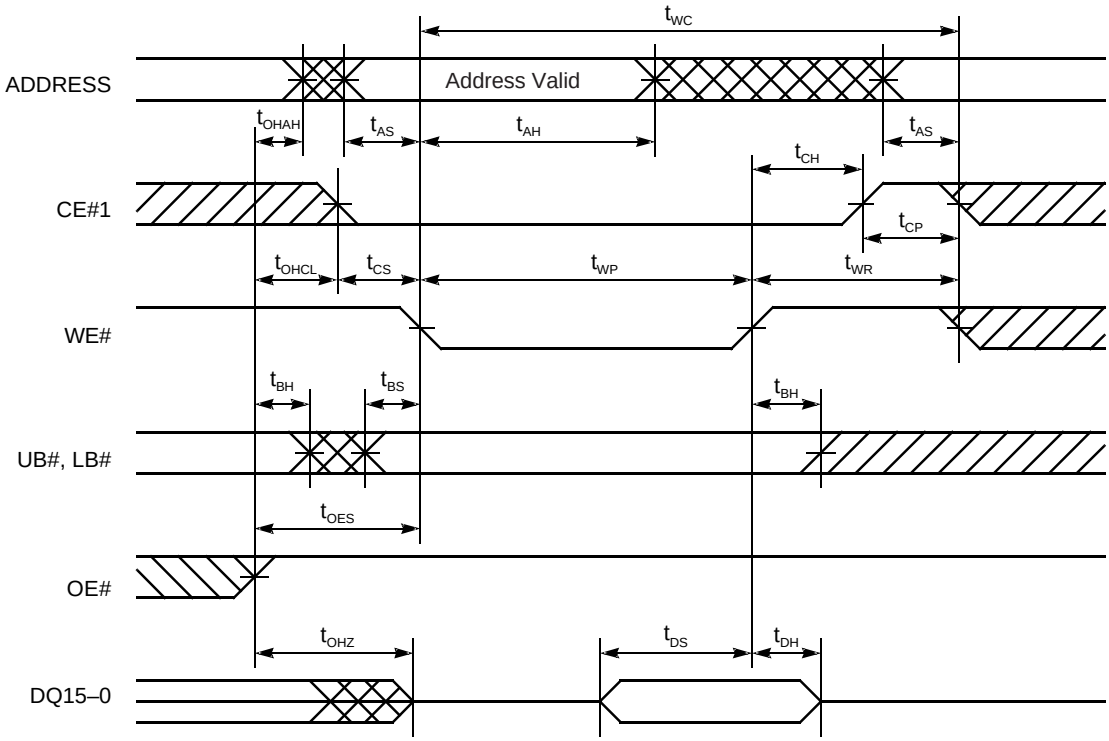


Figure 37. WE# Control Single Write Operation

Note: *CE2 and PE# must be High for write cycle.*

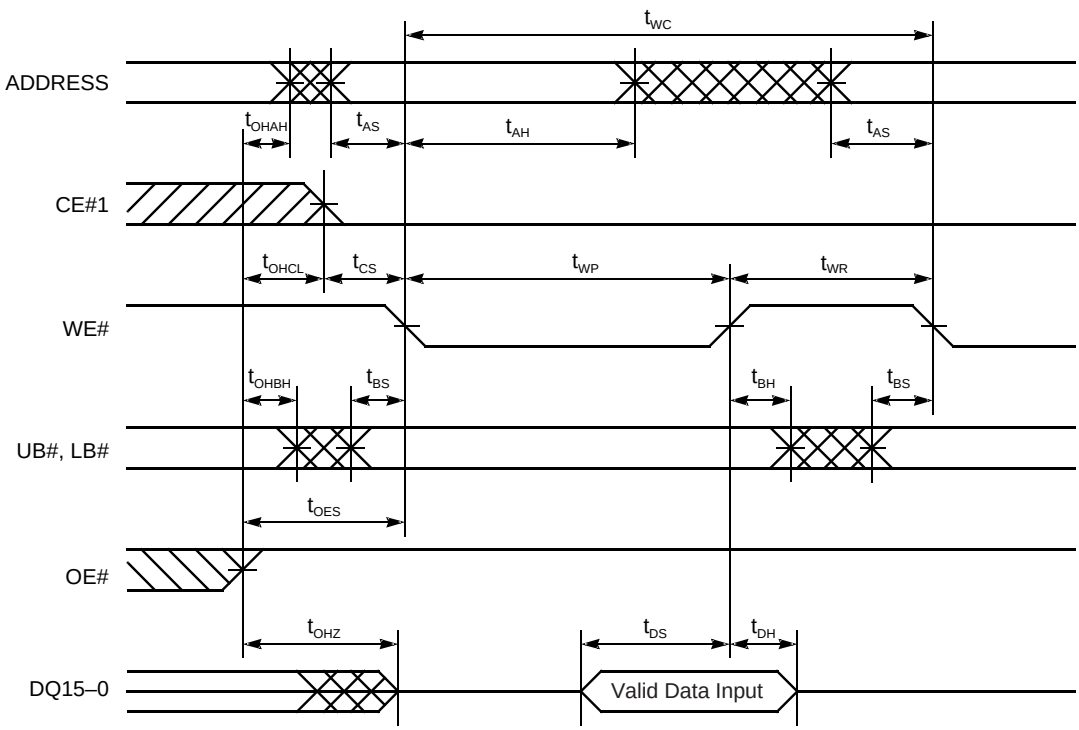


Figure 38. WE# Control Continuous Write Operation

Note: *CE2 and PE# must be High for write cycle.*

FCRAM AC CHARACTERISTICS

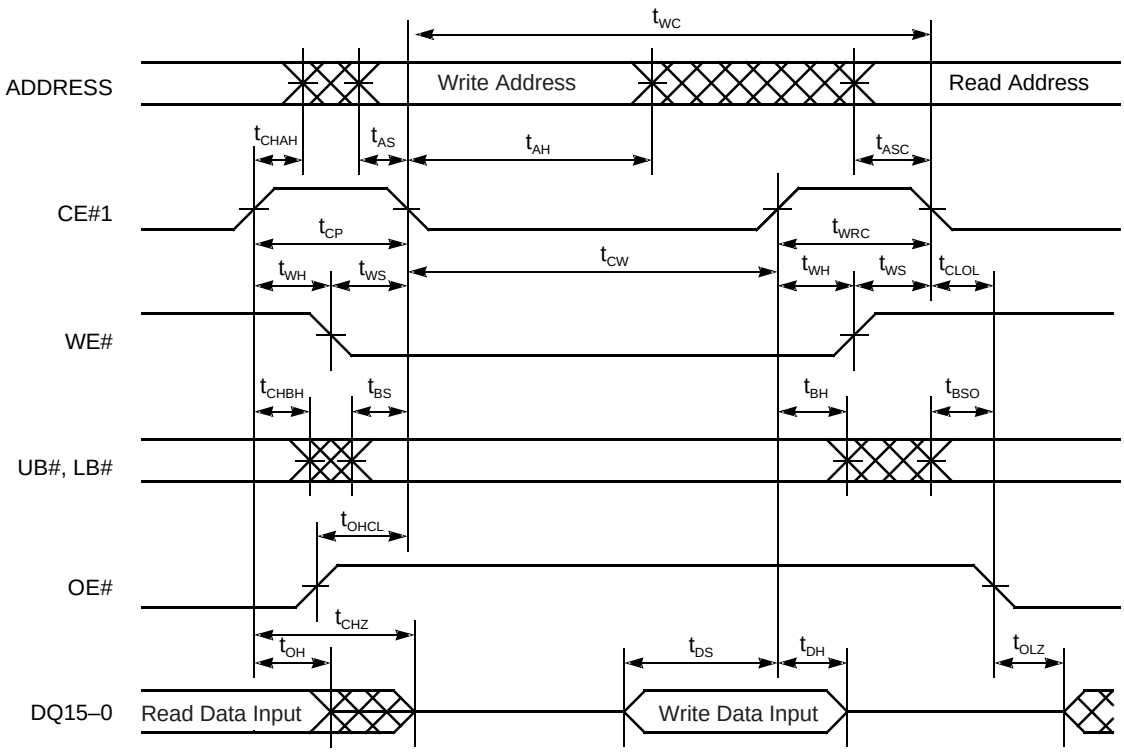


Figure 39. Read/Write Timing CE#1 Control, Read Cycle First

Note: *Write address is valid from either CE#1 or WE# of last falling edge.*

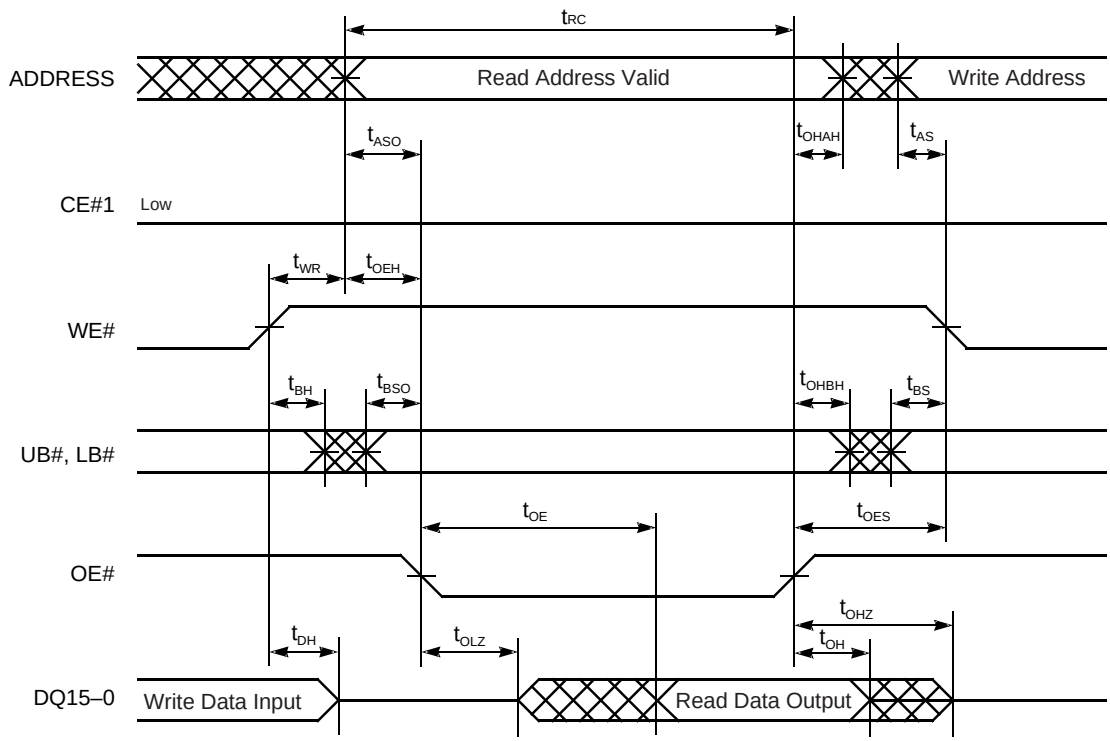


Figure 40. Read/Write Timing CE#1 Control, Write Cycle First

Note: *The t_{OEH} is specified from the time satisfied both t_{WRC} and t_{WR} (min).*

FCRAM AC CHARACTERISTICS

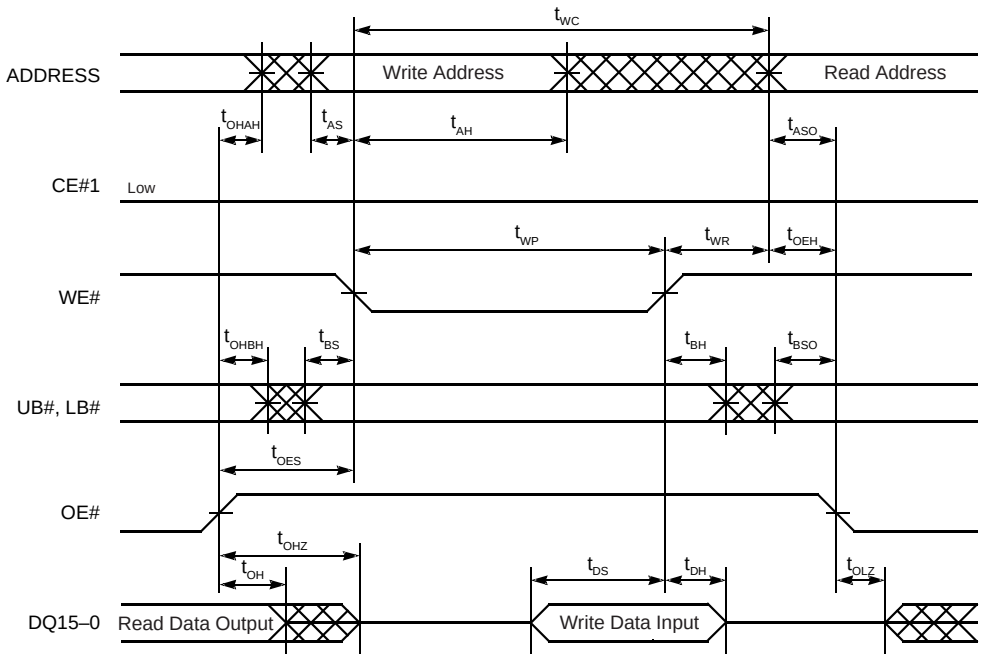


Figure 41. Read (OE# Control)/Write (WE# Control) Timing, Read Cycle First

Notes:

1. *CE#1 can be tied to Low for WE# and OE# controlled operation.*
2. *When CE#1 is tied to Low, output is exclusively controlled by OE#*

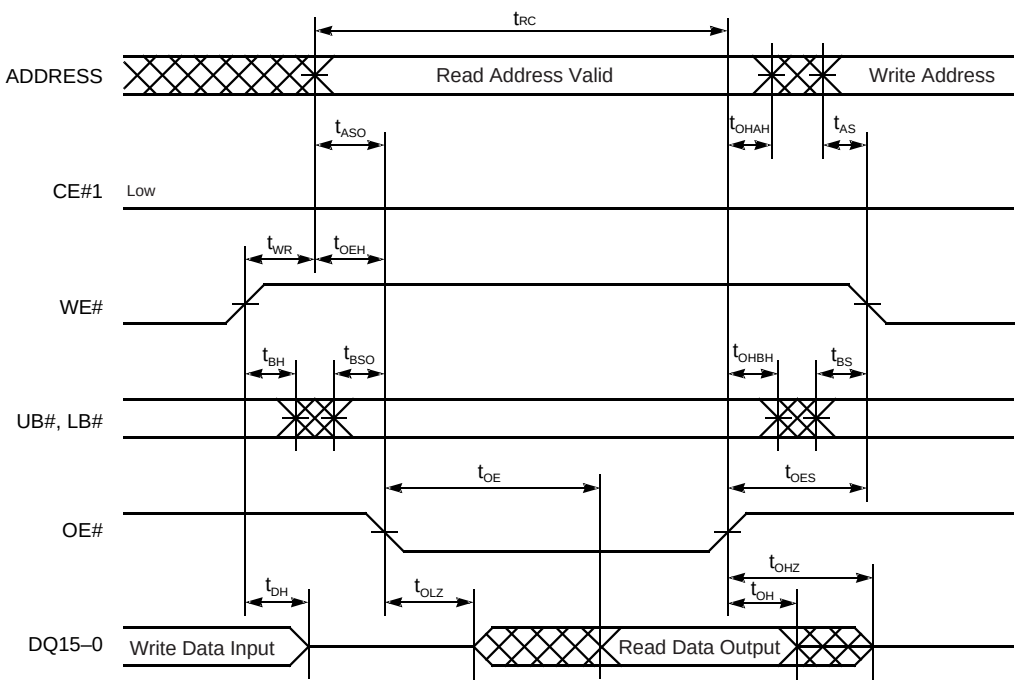


Figure 42. Read (OE# Control)/Write (WE# Control) Timing, Write Cycle First

Notes:

1. *CE#1 can be tied to Low for WE# and OE# controlled operation.*
2. *When CE#1 is tied to Low, output is exclusively controlled by OE#*

FCRAM AC CHARACTERISTICS

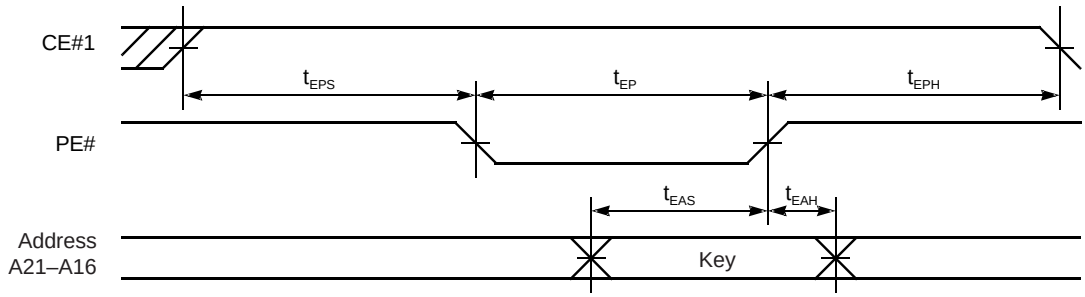


Figure 43. Power Down Program Timing

Notes:

1. *CE2 must be High for Power Down Program operation.*
2. *Any other inputs not specified above can be either High or Low.*

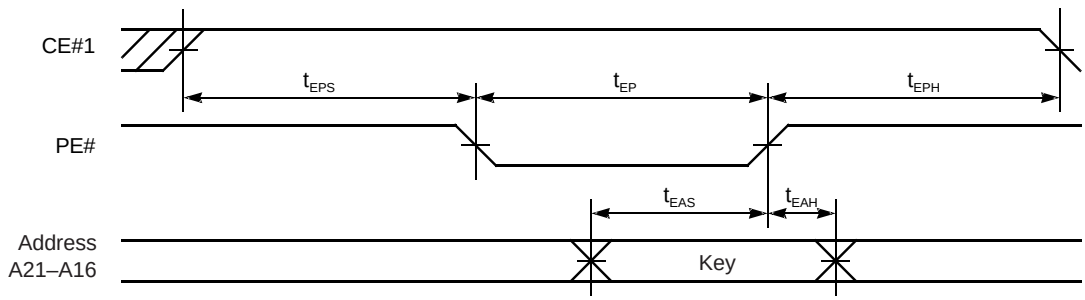


Figure 44. Power Down Program Timing

Notes:

1. *CE2 must be High for Power Down Program operation.*
2. *Any other inputs not specified above can be either High or Low.*

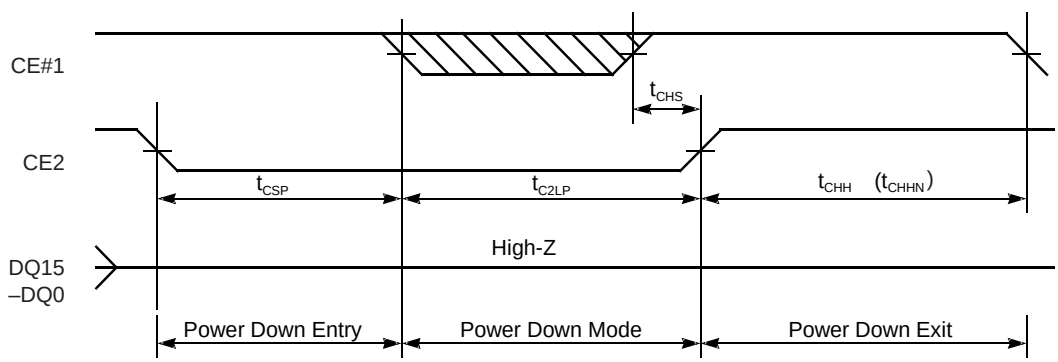


Figure 45. Power Down Entry and Exit Timing

Note:

1. *This Power Down mode can be also used for Power up #2 below except that t_{CHHN} can not be used at Power up timing.*

FCRAM AC CHARACTERISTICS

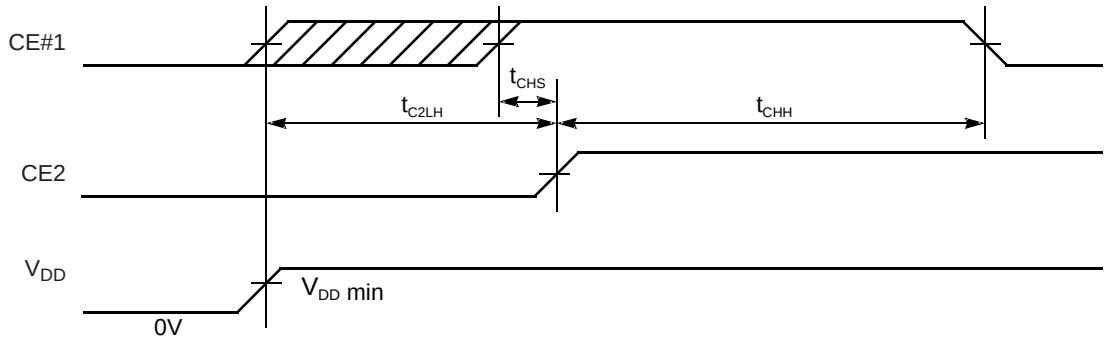


Figure 46. Power Up Timing #1

Notes:

1. *The t_{C2LH} specifies after V_{DD} reaches specified minimum level.*

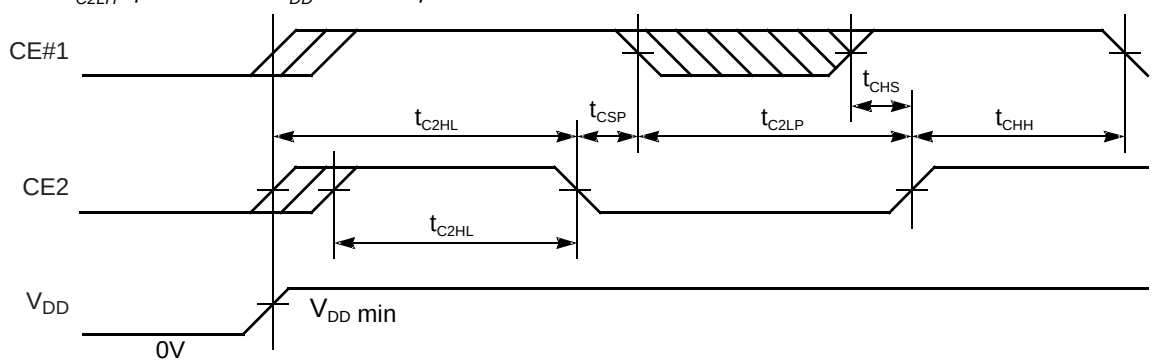


Figure 47. Power Up Timing #2

Notes:

1. *The t_{C2LH} specifies from CE2 Low to High transition after V_{DD} reaches specified minimum level.*
2. *CE#1 must be brought to High prior to or together with CE2 Low to High transition.*

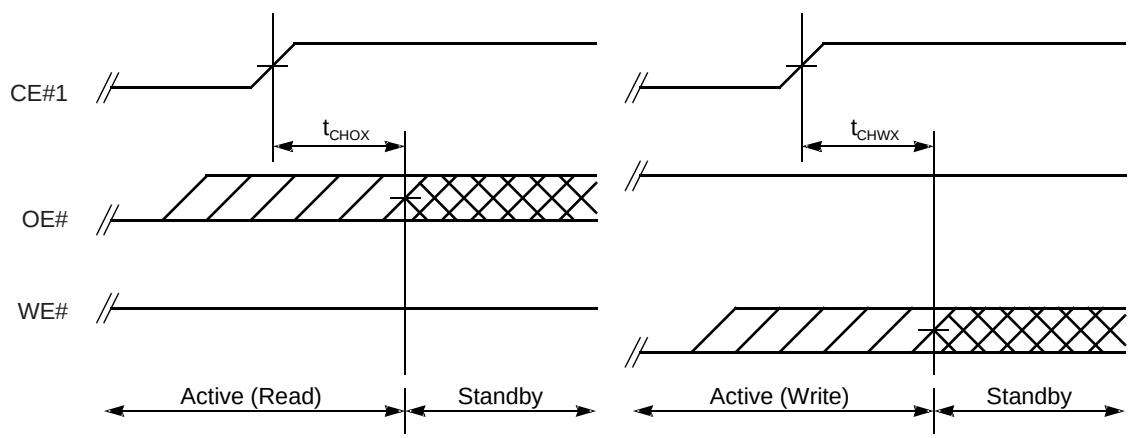


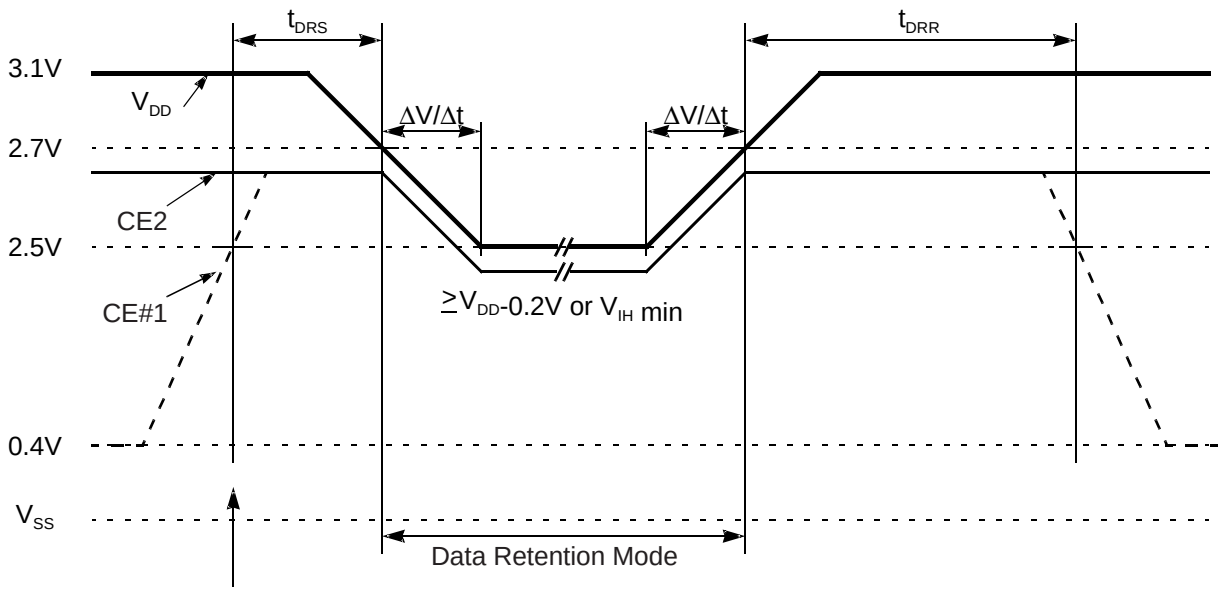
Figure 48. Standby Entry Timing after Read or Write

Note:*Both t_{CHOX} and t_{CHWX} define the earliest entry timing for Standby mode. If either of timing is not satisfied, it takes t_{RC} (min) period from either last address transition of A0, A1, and A2, or CE#1 Low to High transition.*

FCRAM DATA RETENTION

Low V_{DD} Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{DR}	V_{DD} Data Retention Supply Voltage	CE#1 = CE2 ≥ V_{DD} – 0.2V or, CE#1 = CE2 = V_{IH}	2.5	3.1	V
I_{DR}	V_{DD} Data Retention Supply Current	V_{DD} = V_{DR}, V_{IN} = V_{DD} – 0.2 to V_{IH} or V_{IL}, CE#1 = CE2 = V_{IH}, I_{OUT} = 0 mA	–	1.5	mA
I_{DR1}		V_{DD} = V_{DR}, V_{IN} ≤ 0.2 or V_{IN} ≥ V_{DD} – 0.2, CE#1 = CE2 = V_{DD} – 0.2, I_{OUT} = 0 mA	–	150	µA
t_{DRS}	Data Retention Setup Time	V_{DD} = V_{DD} at data retention entry	0	–	ns
t_{DRR}	Data Retention Recovery Time	V_{DD} = V_{DD} after data retention	200	–	ns
Δv/Δt	VDD Voltage Transition Time		0.2	0.2	V/µs



Data bits must be in High-Z at data retention entry.

Figure 49. Data Retention Timing

FLASH ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ 1	Max 2	Unit	Comments
Sector Erase Time		0.4	5	sec	Excludes 00h programming prior to erasure (Note 4)
Chip Erase Time		56		sec	
Byte Program Time		5	150	µs	Excludes system level overhead (Note 5)
Accelerated Byte/Word Program Time		4	120	µs	
Word Program Time		7	210	µs	
Chip Program Time (Note 3)	Byte Mode	42	126	sec	
	Word Mode	28	84		

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, 1,000,000 cycles. Additionally, programming typicals assume checkerboard pattern.*
2. *Under worst case conditions of 90°C, V_{CC} = 2.7 V, 1,000,000 cycles.*
3. *The typical chip programming time is considerably less than the maximum chip programming time listed, since most bytes program faster than the maximum program times listed.*
4. *In the pre-programming step of the Embedded Erase algorithm, all bytes are programmed to 00h before erasure.*
5. *System-level overhead is the time required to execute the two- or four-bus-cycle sequence for the program command. See Table 13 for further information on command definitions.*
6. *The device has a minimum erase and program cycle endurance of 1,000,000 cycles.*

LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including A9, OE#, and RESET#)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

BGA PACKAGE PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup	Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	TBA	TBA	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	TBA	TBA	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	TBA	TBA	pF
C_{IN3}	WP#/ACC Pin Capacitance	V_{IN} = 0	TBA	TBA	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

SRAM DATA RETENTION

Parameter Symbol	Parameter Description	Test Setup	Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention	CS1#s ≥ V_{CC} – 0.2 V 1	1.5		3.3	V
I_{DR}	Data Retention Current	V_{CC} = 3.0 V, CE#1s ≥ V_{CC} – 0.2 V 1		1.0 2	15	µA
t_{SDR}	Data Retention Set-Up Time	See data retention waveforms	0			ns
t_{RDR}	Recovery Time		t_{RC}			ns

Notes:

1. *CE#1s ≥ V_{CC} – 0.2 V, CE2s ≥ V_{CC} – 0.2 V (CE#1s controlled) or CE2s ≤ 0.2 V (CE2s controlled), CIOs = V_{SS} or V_{CC}.*
2. *Typical values are not 100% tested.*

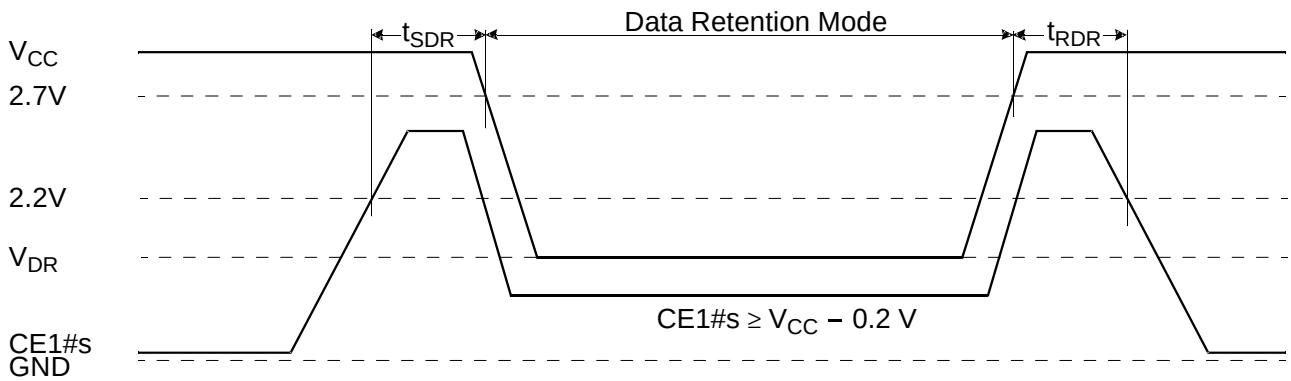


Figure 50. CE#1s Controlled Data Retention Mode

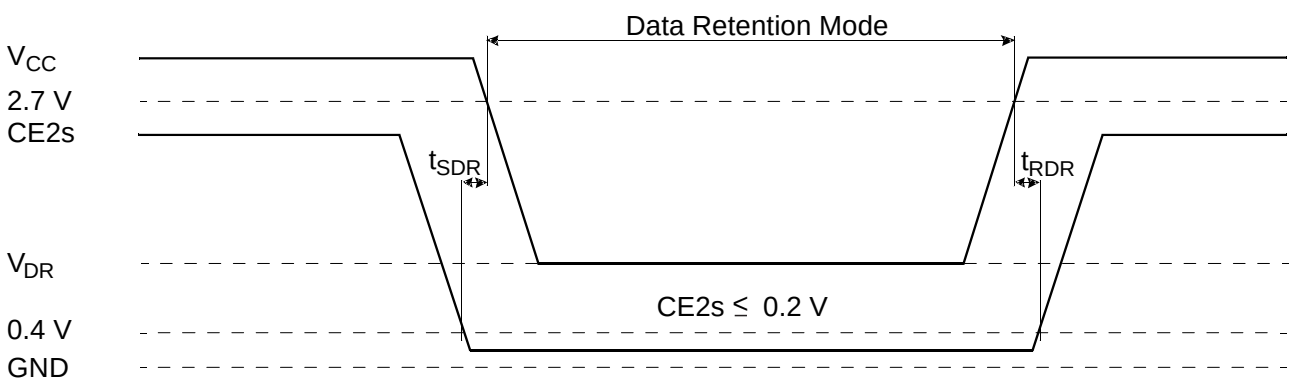
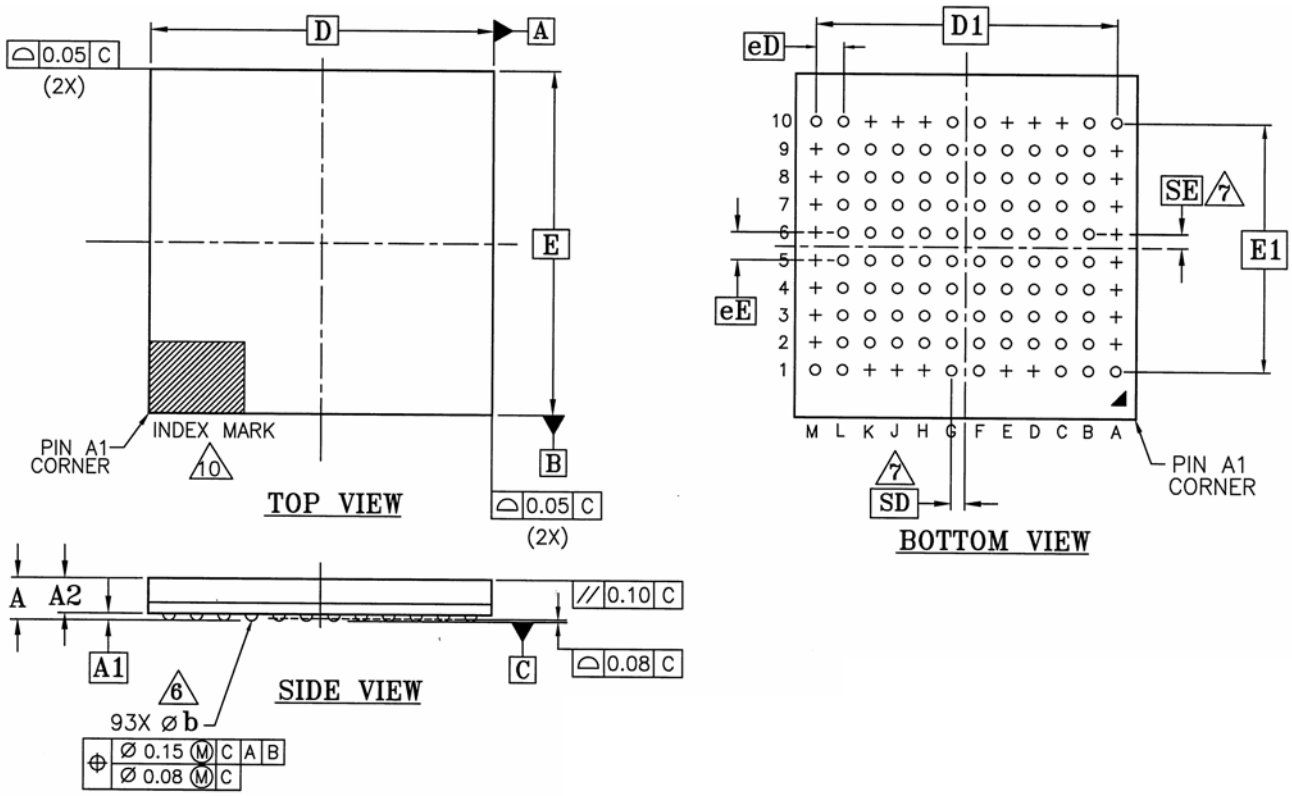


Figure 51. CE2s Controlled Data Retention Mode

PHYSICAL DIMENSIONS

FNA093—93-Ball Fine-Pitch Grid Array 10 x 10 mm
PRELIMINARY



PACKAGE	XFNA 093			NOTE
JEDEC	N/A			
	10.00mm X 10.00mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	1.30	1.40	1.50	PROFILE
A1	0.25	0.30	0.35	BALL HEIGHT
A2	1.05	--	1.23	BODY THICKNESS
D	10.00 BSC			BODY SIZE
E	10.00 BSC			BODY SIZE
D1	8.80 BSC			MATRIX FOOTPRINT
E1	7.20 BSC			MATRIX FOOTPRINT
MD	12			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	93			BALL COUNT
ø b	0.30	0.35	0.40	BALL DIAMETER
eE	0.80 BSC			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT
	A2,A3,A4,A5,A6,A7,A8,A9, C10,D1,D10,E1,E10,H1,H10 J1,J10,K1,K10, M2,M3,M4,M5,M6,M7,M8,M9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95–1, SPP–010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. "X" PRECEDING THE PACKAGE CODE DENOTES PART IS UNDER QUALIFICATION.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

REVISION SUMMARY

Revision A (October 25, 2002)

Initial release.