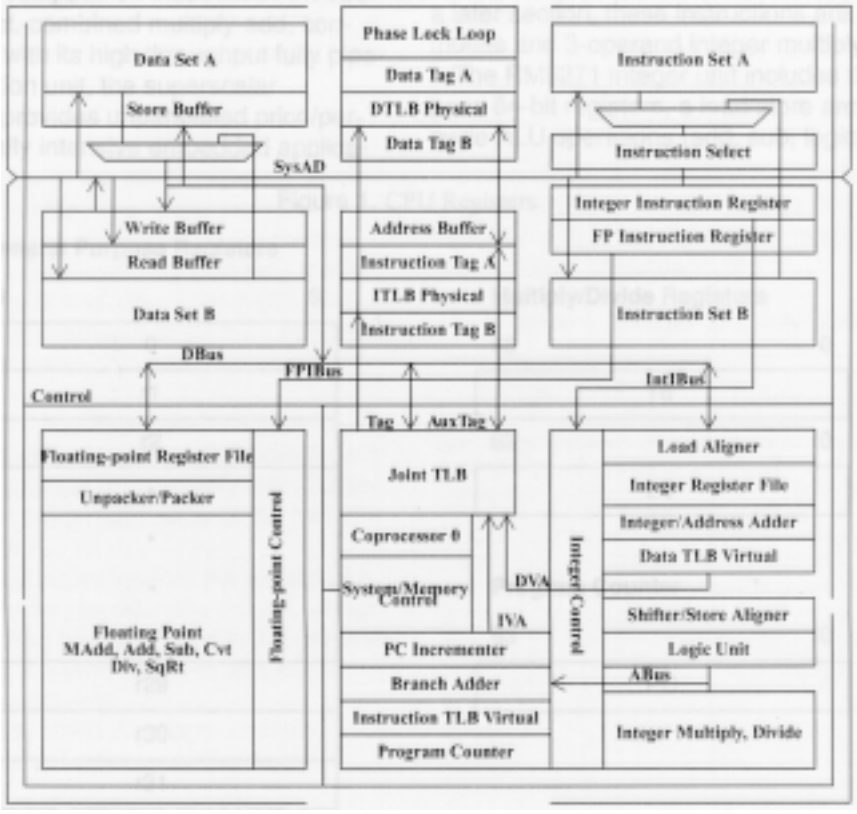
ACT5271
64-Bit Superscaler Microprocessor

Features

- **Full militarized QED RM5271 microprocessor**
- **Dual Issue superscalar microprocessor - can issue one integer and one floating-point instruction per cycle**
  - 150, 200, 250 MHz operating frequencies – Consult Factory for latest speeds
  - 345 Dhrystone2.1 MIPS maximum
  - SPECInt95 7.3, SPECfp95 8.3 maximum
- **High performance system interface compatible with RM7000, RM5270, RM5260, RM5261, R4600, R4700 and R5000**
  - Up to 125MHz memory bus operation for a 1000MBps bandwidth from CPU to L2 cache and main memory
  - 64-bitmultiplexed system address/data bus for optimum price/ performance with high performance write protocols to maximize uncached write bandwidth
  - Supports 1/2 clock divisors (2, 2.5, 3, 3.5, 4, 4.5, 5, 6, 7, 8, 9)
  - IEEE 1149.1 JTAG boundary scan
- **Integrated on-chip caches**
  - 32KB/32KB instruction/data -both 2 way set associative
  - Virtually indexed, physically tagged
  - Write-back and write-through on per page basis
  - Pipeline restart on first double for data cache misses
- **Integrated secondary cache controller (R5000 compatible)**
  - Supports 512K or 2MByte block write-through secondary
- **Integrated memory management unit**
  - Fully associative joint TLB (shared by I and D translations)
  - 48 dual entries map 96 pages
  - Variable page size (4KB to 16MB in 4x increments)
- **High-performance floating point unit - up to 532 MFLOPS**
  - Single cycle repeat rate for common single precision operations and some double precision operations
  - Two cycle repeat rate for double precision multiply and double precision combined multiply-add operations
  - Single cycle repeat rate for single precision combined multiply-add operation
- **MIPS IV instruction set**
  - Floating point multiply-add instruction increases performance in signal processing and graphics applications
  - Conditional moves to reduce branch frequency
  - Index address modes (register + register)
- **Embedded application enhancements**
  - Specialized DSP integer Multiply-Accumulate instruction and 3 operand multiply instruction
  - I and D cache locking by set
  - Optional dedicated exception vector for interrupts
- **Fully static CMOS design with power down logic**
  - Standby reduced power mode with WAIT instruction
  - 4.2 Watts typical power @ 200MHz
  - 2.5V core with 3.3V IO's
- **208-lead CQFP, cavity-up package (F17)**
- **208-lead CQFP, inverted footprint (F24), Intended to duplicate the commercial QED footprint**
- **179-pin PGA package (*Future Product)* (P10)**

BLOCK DIAGRAM



Preliminary

DESCRIPTION

The Aeroflex ACT5271 is a highly integrated superscalar microprocessor that implements a superset of the MIPS IV Instruction Set Architecture(ISA). It has a high performance 64-bit integer unit, a high throughput, fully pipelined 64-bit floating point unit, an operating system friendly memory management unit with a 48-entry fully associative TLB, a 32 KByte 2-way set associative instruction cache, a 32 KByte 2-way set associative data cache, and a high-performance 64-bit system interface with support for an optional external secondary cache. The ACT5271 can issue both an integer and a floating point instruction in the same cycle.

The ACT5271 is ideally suited for high-end embedded control applications such as internetworking, high performance image manipulation, high speed printing, and 3-D visualization.The ACT5271 is also applicable to the low end workstation market where its balanced integer and floating-point performance and direct support for a large secondary cache (up to 2MB) provide outstanding price/performance

HARDWARE OVERVIEW

The ACT5271 offers a high-level of integration targeted at high-performance embedded applications. The key elements of the ACT5271 are briefly described below.

Superscalar Dispatch

The ACT5271 has an efficient asymmetric superscalar dispatch unit which allows it to issue an integer instruction and a floating-point computation instruction simultaneously. With respect to superscalar issue, integer instructions include alu, branch, load/store, and floating-point load/ store, while floating-point computation instructions include floating-point add, subtract, combined multiply-add, converts, etc. In combination with its high throughput fully pipelined floating-point execution unit, the superscalar capability of the ACT5271 provides unparalleled price/performance in computationally intensive embedded applications.

CPU Registers

Like all MIPS ISA processors, the ACT5271 CPU has a simple, clean user visible state consisting of 32 general purpose registers, two special purpose registers for integer multiplication and division, a program counter, and no condition code bits.

Pipeline

For integer operations, loads, stores, and other non-floating-point operations, the ACT5271 uses the simple 5-stage pipeline also found in the ACT52xx family, R4600, R4700, and R5000. In addition to this standard pipeline, the ACT5271 uses an extended seven stage pipeline for floating-point operations. Like the ACT5270 and R5000, the ACT5271 does virtual to physical translation in parallel with cache access.

Integer Unit

Like the other members of the ACT52xx family and R5000, the ACT5271 implements the MIPS IV Instruction Set Architecture, and is therefore fully upward compatible with applications that run on processors implementing the earlier generation MIPS I-III instruction sets. Additionally, the ACT5271 includes two implementation specific instructions not found in the baseline MIPS IV ISA but that are useful in the embedded market place. Described in detail in the QED RM5271 datasheet, these instructions are integer multiply-accumulate and 3-operand integer multiply.

The ACT5271 integer unit includes thirty-two general purpose 64-bit registers, a load/store architecture with single cycle ALU operations (add, sub, logical, shift) and an autonomous multiply/ divide unit. Additional register resources include: the HI/LO result registers for the two-operand integer multiply/divide operations, and the program counter(PC).

Register File

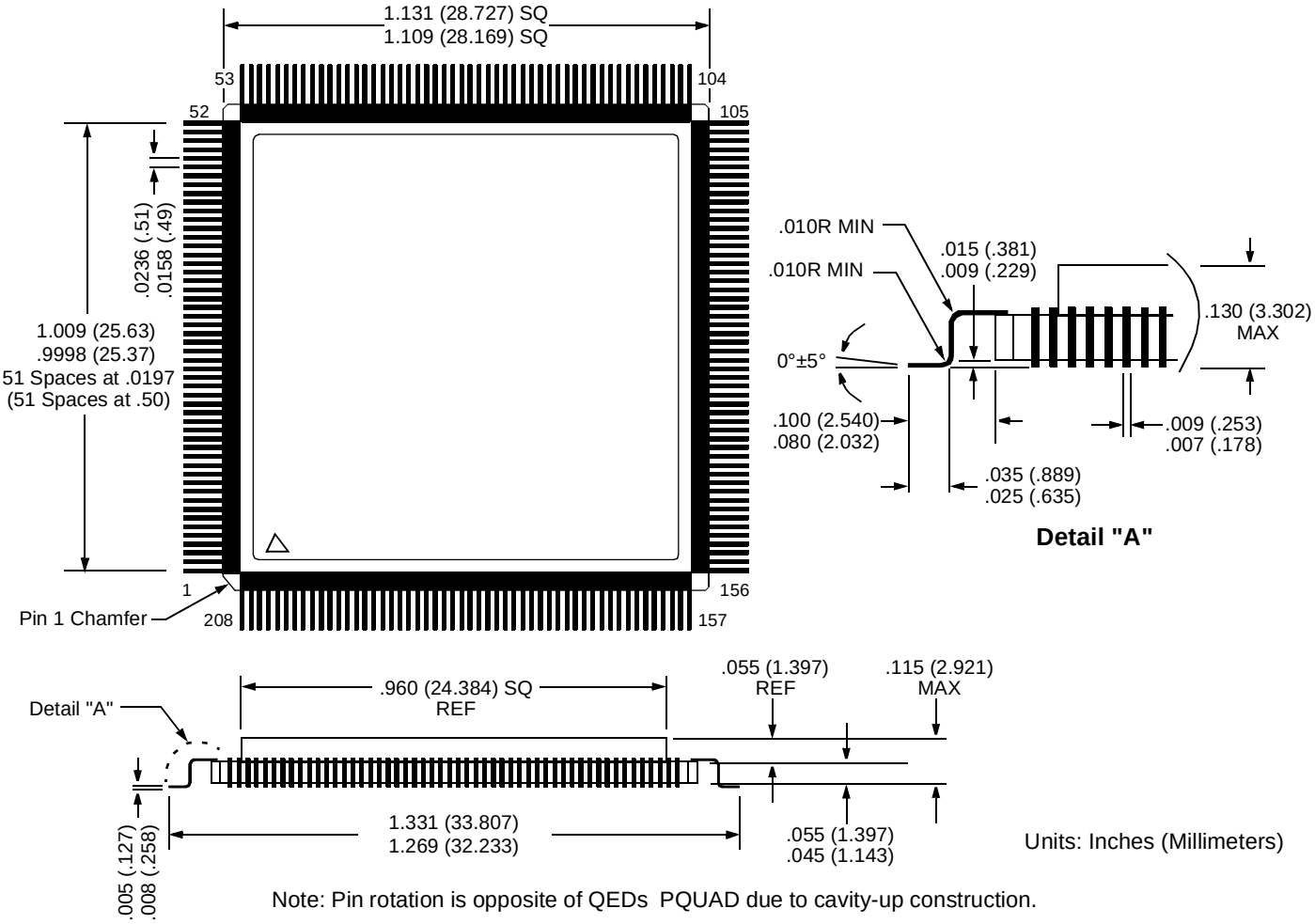
The ACT5271 has thirty-two general purpose registers with register location 0 hard wired to zero. These registers are used for scalar integer operations and address calculation. The register file has two read ports and one write port and is fully bypassed to minimize operation latency in the pipeline.

ALU

The ACT5271 ALU consists of the integer adder/ subtractor, the logic unit, and the shifter. The adder performs address calculations in addition to arithmetic operations, the logic unit performs all logical and zero shift data moves, and the shifter performs shifts and store alignment operations. Each of these units is optimized to perform all tions in a single processor cycle.

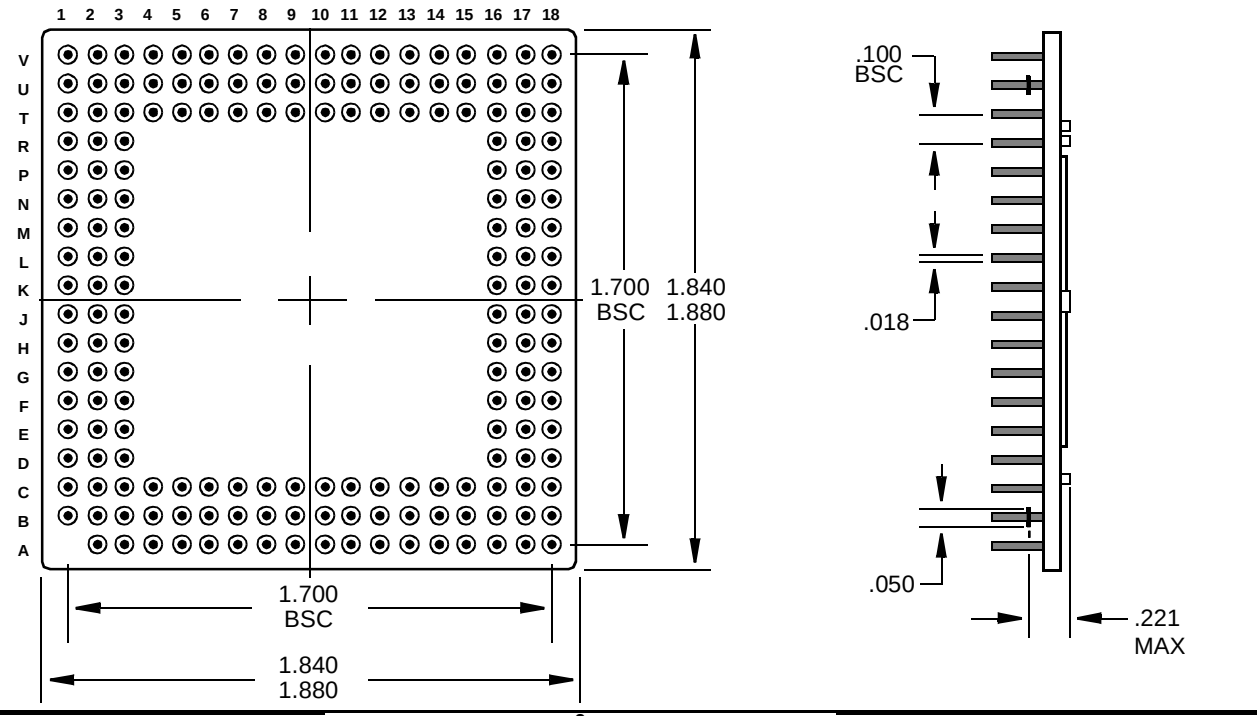
For additional Detail Information regarding the operation of the Quantum Effect Design (QED) RISCMark™ ACT5271™, 64-Bit Superscalar Microprocessor see the latest QED datasheet (Revision 1.0 July 1998).

Package Information – "F17" – CQFP 208 Leads



Note: Pin rotation is opposite of QEDs PQUAD due to cavity-up construction.

Future Package – "P10" – PGA 179 Pins *(Advanced)*



ACT5271 Microprocessor CQFP Pinouts – "F17"

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	Vcc (3.3V)	53	NC	105	Vcc (3.3V)	157	NC
2	NC	54	NC	106	NMI*	158	NC
3	NC	55	NC	107	ExtRqst*	159	NC
4	Vcc (3.3V)	56	Vcc (3.3V)	108	Reset*	160	NC
5	Vss	57	Vss	109	ColdReset*	161	Vcc (3.3V)
6	SysAD4	58	ModeIn	110	VccOK	162	Vss
7	SysAD36	59	RdRdy*	111	BigEndian	163	SysAD28
8	SysAD5	60	WrRdy*	112	Vcc (3.3V)	164	SysAD60
9	SysAD37	61	ValidIn*	113	Vss	165	SysAD29
10	Vcc (2.5V)	62	ValidOut*	114	SysAD16	166	SysAD61
11	Vss	63	Release*	115	SysAD48	167	Vcc (2.5V)
12	SysAD6	64	VccP	116	Vcc (2.5V)	168	Vss
13	SysAD38	65	VssP	117	Vss	169	SysAD30
14	Vcc (3.3V)	66	SysClock	118	SysAD17	170	SysAD62
15	Vss	67	Vcc (2.5V)	119	SysAD49	171	Vcc (3.3V)
16	SysAD7	68	Vss	120	SysAD18	172	Vss
17	SysAD39	69	Vcc (3.3V)	121	SysAD50	173	SysAD31
18	SysAD8	70	Vss	122	Vcc (3.3V)	174	SysAD63
19	SysAD40	71	Vcc (2.5V)	123	Vss	175	SysADC2
20	Vcc (2.5V)	72	Vss	124	SysAD19	176	SysADC6
21	Vss	73	SysCmd0	125	SysAD51	177	Vcc (2.5V)
22	SysAD9	74	SysCmd1	126	Vcc (2.5V)	178	Vss
23	SysAD41	75	SysCmd2	127	Vss	179	SysADC3
24	Vcc (3.3V)	76	SysCmd3	128	SysAD20	180	SysADC7
25	Vss	77	Vcc (3.3V)	129	SysAD52	181	Vcc (3.3V)
26	SysAD10	78	Vss	130	SysAD21	182	Vss
27	SysAD42	79	SysCmd4	131	SysAD53	183	SysADC0
28	SysAD11	80	SysCmd5	132	Vcc (3.3V)	184	SysADC4
29	SysAD43	81	Vcc (3.3V)	133	Vss	185	Vcc (2.5V)
30	Vcc (2.5V)	82	Vss	134	SysAD22	186	Vss
31	Vss	83	SysCmd6	135	SysAD54	187	SysADC1
32	SysAD12	84	SysCmd7	136	Vcc (2.5V)	188	SysADC5
33	SysAD44	85	SysCmd8	137	Vss	189	SysAD0
34	Vcc (3.3V)	86	SysCmdP	138	SysAD23	190	SysAD32
35	Vss	87	Vcc (2.5V)	139	SysAD55	191	Vcc (3.3V)
36	SysAD13	88	Vss	140	SysAD24	192	Vss
37	SysAD45	89	Vcc (2.5V)	141	SysAD56	193	SysAD1
38	SysAD14	90	Vss	142	Vcc (3.3V)	194	SysAD33
39	SysAD46	91	Vcc (3.3V)	143	Vss	195	Vcc (2.5V)
40	Vcc (2.5V)	92	Vss	144	SysAD25	196	Vss
41	Vss	93	Int0*	145	SysAD57	197	SysAD2
42	SysAD15	94	Int1*	146	Vcc (2.5V)	198	SysAD34
43	SysAD47	95	Int2*	147	Vss	199	SysAD3
44	Vcc (3.3V)	96	Int3*	148	SysAD26	200	SysAD35
45	Vss	97	Int4*	149	SysAD58	201	Vcc (3.3V)
46	ModeClock	98	Int5*	150	SysAD27	202	Vss
47	JTDO	99	Vcc (3.3V)	151	SysAD59	203	NC
48	JTDI	100	Vss	152	Vcc (3.3V)	204	NC
49	JTCK	101	NC	153	Vss	205	NC
50	JTMS	102	NC	154	NC	206	NC
51	Vcc (3.3V)	103	NC	155	NC	207	Vcc (3.3V)
52	Vss	104	NC	156	Vss	208	Vss

Sample Ordering Information

Part Number	Screening	Speed (MHz)	Package
ACT-5271PC-150F17C	Commercial Temperature	150	208 Lead CQFP
ACT-5271PC-200F17I	Industrial Temperature	200	208 Lead CQFP
ACT-5271PC-250F17T	Military Temperature	250	208 Lead CQFP
ACT-5271PC-250F17M	Military Screening	250	208 Lead CQFP

Part Number Breakdown

ACT– 5271 PC – 200 F17 M

Aeroflex Circuit Technology

Base Processor Type

Cache Style

PC = Primary Cache

Maximum Pipeline Freq.

150 = 150MHz
200 = 200MHz
250 = 250MHz
266 = 266MHz (Future option)

Screening

C = Commercial Temp, 0°C to +70°C
I = Industrial Temp, -40°C to +85°C
T = Military Temp, -55°C to +125°C
M = Military Temp, -55°C to +125°C, Screened *
Q = MIL-PRF-38534 Compliant/SMD if applicable

Package Type & Size

Surface Mount Package

F17 = 1.120" SQ 208 Lead CQFP
F24 = 1.120" SQ Inverted 208 Lead CQFP

Thru-Hole Package

P10 = 1.86"SQ PGA 179 pins with shoulder (Advanced)

* **Screened to the individual test methods of MIL-STD-883**

Specifications subject to change without notice.

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