WD1100-07 Host Interface Logic

FEATURES

- SINGLE +5V SUPPLY
- WAIT SIGNAL GENERATION
- TIMING CLOCK GENERATION
- INDEX PROPAGATION
- CARD ACCESS CONTROL
- COMPLIMENTS ECC ARCHITECTURE
- 20 PIN DIP PACKAGE

DESCRIPTION

The WD1100-07 Host Interface Logic chip simplifies the design of a Winchester Hard Disk Controller using the WD1100 chip series. It does this by performing logic functions that would otherwise require considerable discrete logic. Additionally, there are signals provided for ECC implementation.

The WD1100-07 is implemented in NMOS silicon gate technology and is available in a 20-pin plastic or ceramic Dual-in-Line package.

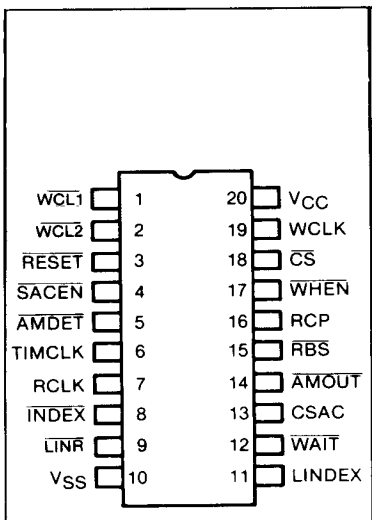

Figure 1.
WD1100-07 PIN CONNECTIONS

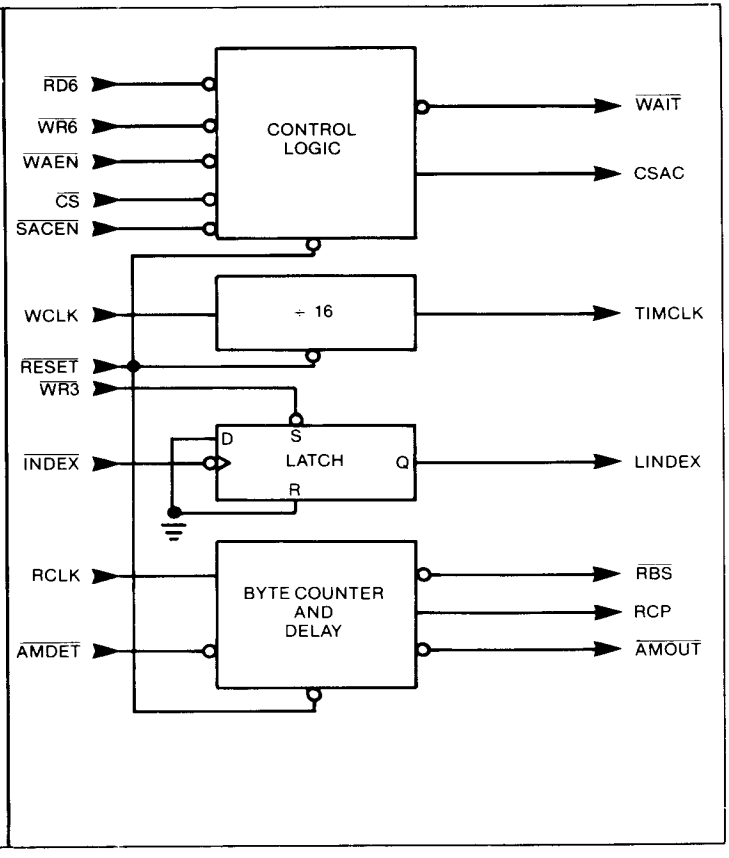

Figure 2.
WD1100-07 BLOCK DIAGRAM

PIN NUMBER	PIN NAME	SYMBOL	FUNCTION
1	WAIT CLEAR 1	$\overline{WCL1}$	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
2	WAIT CLEAR 2	$\overline{WCL2}$	This input presets a WAIT latch to a non-WAIT condition on the falling edge.
3	RESET	$\overline{RESET}$	An input used to set TIMCLK & reset $\overline{WAIT}$, $\overline{AMOUT}$ and $\overline{RBS}$.
4	SELECT ADDRESS ENABLE	$\overline{SACEN}$	This is an input signal that is used to enable card select for host access.
5	ADDRESS MARK DETECT	$\overline{AMDET}$	An input that must go active when a DATA = A1(HEX) or clock = 0A(HEX) pattern is detected in the data stream.
6	TIMING CLOCK	TIMCLK	An output used to provide reference timing signals to SA100 type drives.
7	READ CLOCK	RCLK	This input, the same as used to clock in data and clocks to the AM detector, is used to produce AMOUT.
8	INDEX PULSE	$\overline{INDEX}$	This input is provided by the drive once each revolution of the disk.
9	LINDEX RESET	$\overline{LINR}$	An input used to reset LINDEX.
10	GROUND	V_{SS}	Ground.
11	LATCHED INDEX	LINDEX	An output that is $\overline{INDEX}$ delayed by one clock time.
12	WAIT	$\overline{WAIT}$	This output goes true when controller is internally accessing data or has not accepted data from the host during a WRITE.
13	CARD SELECT ADDRESS	CSAC	An output that is the result of $\overline{CS}$ qualified with $\overline{SACEN}$.
14	ADDRESS MARK DELAYED OUTPUT	$\overline{AMOUT}$	This output is a delayed version of $\overline{AMDET}$.
15	READ BYTE STROBE	$\overline{RBS}$	This output strobes once for each byte of READ data. Initialized by $\overline{AMDET}$.
16	READ CLOCK PULSE	RCP	This output is delayed from RCLK through propagation. Not normally used.
17	WAIT ENABLE	$\overline{WAEN}$	An input that is used to enable the internal WAIT circuitry.
18	CARD SELECT	$\overline{CS}$	An input from host that selects controller.
19	WRITE CLOCK	WCLK	This input is used to produce TIMCLK on low to high transitions.
20	+5VDC	V_{CC}	+5V ± 10%.

DEVICE DESCRIPTION

Upon power up or reset, $\overline{WAIT}$, $\overline{AMOUT}$, and $\overline{RBS}$ are reset and TIMCLK is set. This is the only interactive signal between the four sections of the chip. Each section will be described separately.

Control Logic

This section provides $\overline{WAIT}$ (pin 12) and CSAC (pin 13). $\overline{WAIT}$ is set in its active low state when $\overline{WAEN}$ (pin 17) is active low by the falling edge of $\overline{CS}$ (pin 18). $\overline{WAIT}$ is reset by the falling edge of either $\overline{WCL1}$ or $\overline{WCL2}$ depending on whether in a read or write mode. CSAC (pin 13) is enabled by setting $\overline{SACEN}$ (pin 4) low after $\overline{WAIT}$ has been enabled. CSAC is reset by $\overline{WCL1}$ or $\overline{WCL2}$.

Timing Clock

TIMCLK (pin 6) is a divided by sixteen version of WCLK (pin 19). It is used with SA1000 type drives.

Index Pulse

Lindex (pin 11) is a delayed version of $\overline{INDEX}$ (pin 8). It remains high until reset by $\overline{LINR}$ (pin 9).

Read Byte Sync

$\overline{RBS}$ (pin 15) will go true on the eighth negative going transition of RCLK (pin 7) after $\overline{AMDET}$ (pin 5) goes true. $\overline{RBS}$ will remain true for one clock cycle.

Read Clock Pulse

RCP (pin 16) is a delayed version of RCLK and is normally left open by the user.

Address Mark Delayed Output

$\overline{AMOUT}$ (pin 14) is the same as $\overline{AMDET}$ delayed by two clock times.

These circuits were developed to work with the other chips in the WD1100 series. They are used on the WD1001 the timing relationships must be observed.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
under Bias .....0°C (32°F) to 50°C (122°F)
Voltage on any pin
with respect to V_{SS} .....-0.2V to +7.0V
Power Dissipation .....1 Watt
Storage Temperature
Plastic ....-55°C (-67°F) to +125°C (257°F)
Ceramic ...-55°C (-67°F) to +150°C (302°F)

NOTE:

Maximum ratings indicate operation where permanent device damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC electrical characteristics.

DC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = +5V ±10%, V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITIONS
V_{IL}	Input Low Voltage	-0.2		0.8	V	
V_{IH}	Input High Voltage	2.0			V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 3.2 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = -200µA
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
I_{CC}	Supply Current			125	mA	All Outputs Open
I_{IH}	Current Input High			<10	uA	V_{IN} = .4 to V_{CC}
I_{IL}	Current Input Low			<10	uA	V_{IN} = .4 to V_{CC}

AC Electrical Characteristics T_A = 0°C (32°F) to 50°C (122°F); V_{CC} = 5V ±10%; V_{SS} = 0V

SYMBOL	PARAMETER	MIN	TYP[1]	MAX	UNIT	CONDITIONS
f_{WC}	WCLK FREQUENCY			5.25	MHz	
t_{CW}	$\overline{CS}$↓ to $\overline{WAIT}$↓		50	160	nsec	
t_{WS}	$\overline{WCL1}$↓ or $\overline{WCL2}$↓ to $\overline{WAIT}$↑		170	195	nsec	
t_{SU}	$\overline{WAEN}$ Setup Time	50			nsec	
t_{SC}	$\overline{SACEN}$↓ to CSAC↑		5	70	nsec	$\overline{WAIT}$ TRUE
t_{CS}	$\overline{WCL1}$↓ or $\overline{WCL2}$↓ CSAC↓		45	155	nsec	$\overline{WAIT}$ TRUE
t_{WT}	WCLK↑ to TIMCLK↑			250	nsec	
t_{LI}	$\overline{INDEX}$↓ to LINDEX↑		50	100	nsec	
t_{LW}	$\overline{LINR}$↓ to LINDEX↓		30	100	nsec	
t_{PC}	RCLK↓ to RCP↓		30	75	nsec	
t_{RA}	$\overline{AMDET}$ Setup Time		30	50	nsec	
			2 CLOCK CYCLES	2 CLOCK CYCLES +45	nsec	
t_{AM}	$\overline{AMDET}$↓ to $\overline{AMOUT}$↓		8 CLOCK CYCLES +165	8 CLOCK CYCLES 90	nsec	
t_{BS}	RCLK↓ to $\overline{RBS}$↓				nsec	
t_{RB}	$\overline{RBS}$ Period		1 CLOCK CYCLE			

[1]NOTE: Typical Values are for T_A = 25°C (77°F) and V_{CC} = +5V