



Dual P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.023 @ $V_{GS} = -10$ V	-10.2
	0.035 @ $V_{GS} = -4.5$ V	-8.1

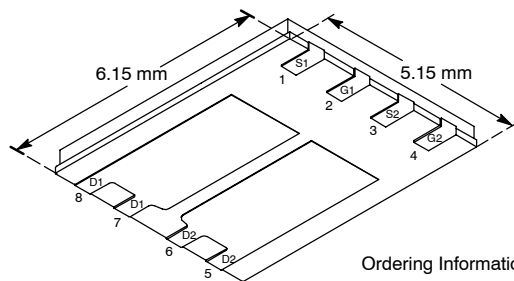
FEATURES

- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile

APPLICATIONS

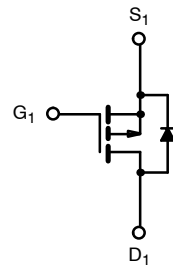
- Load Switch
 - Notebook PCs
 - Desktop PCs
 - Game Stations
- Battery Switch

PowerPAK SO-8

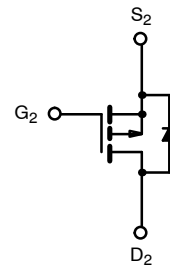


Ordering Information: Si7991DP-T1

Bottom View



P-Channel MOSFET



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	−30		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	−10.2	−6.6	A
	T _A = 70°C		−8.2	−5.3	
Pulsed Drain Current		I _{DM}	−30		
continuous Source Current (Diode Conduction) ^a		I _S	−2.9	−1.2	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	3.5	1.4	W
	T _A = 70°C		2.2	0.9	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	$t \leq 10$ sec	R_{thJA}	28	35	$^\circ\text{C/W}$
	Steady State		60	85	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	3	3.7	

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

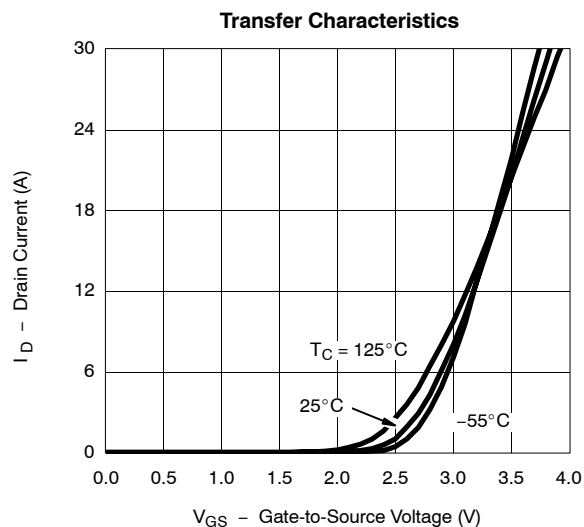
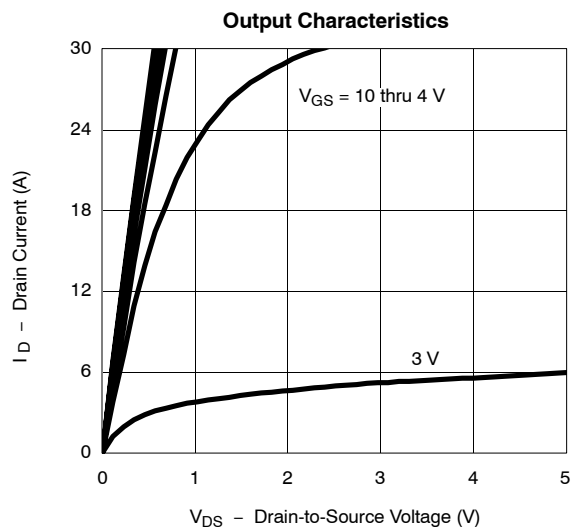
SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

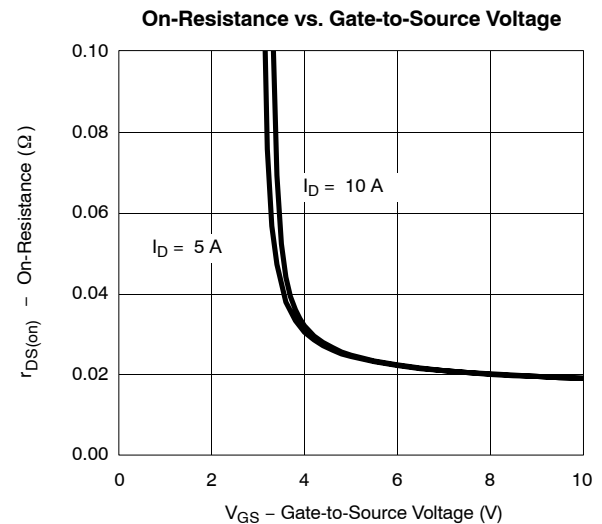
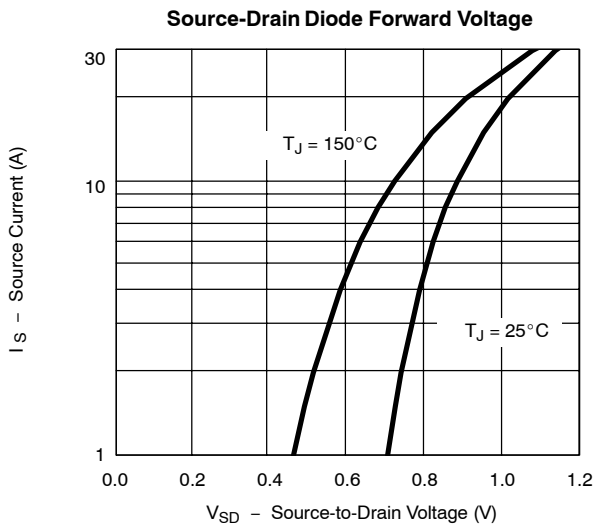
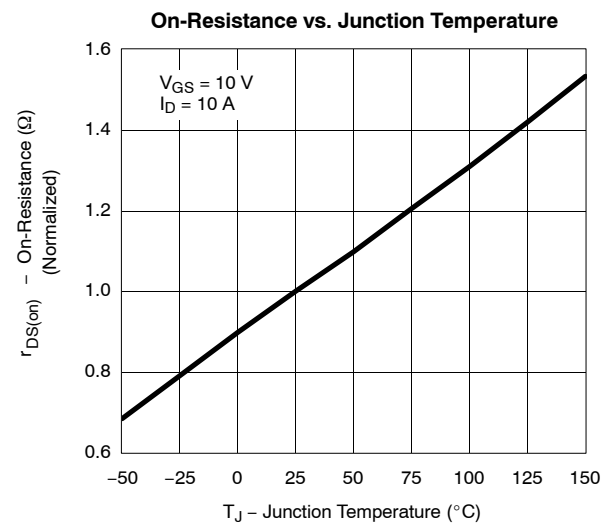
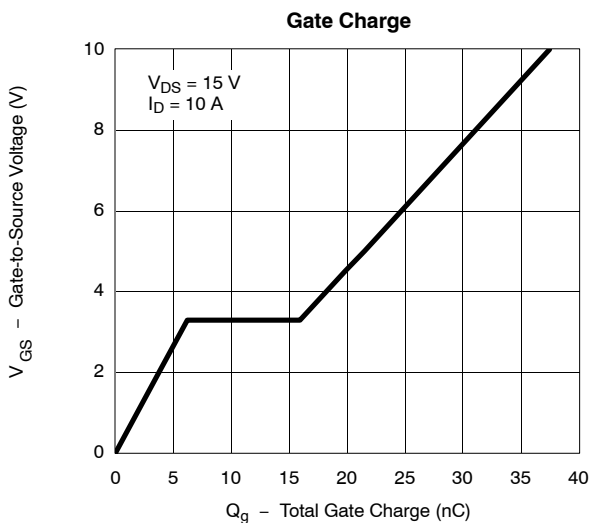
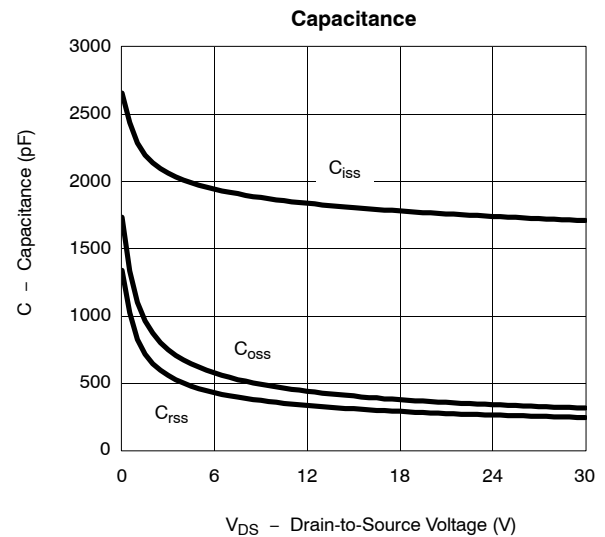
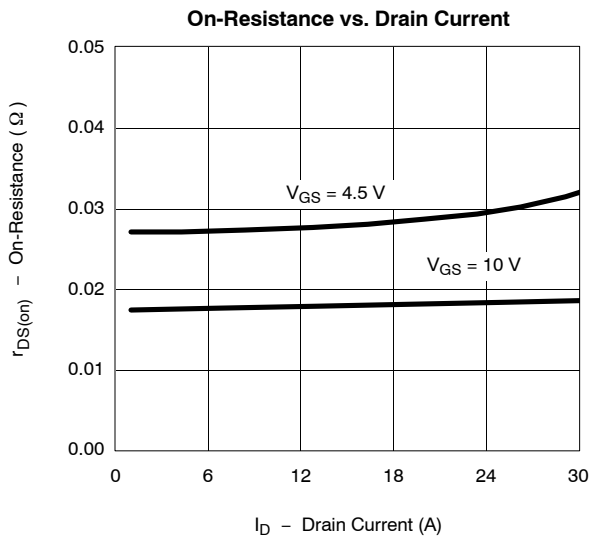
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1		-3	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\ \text{V}, V_{GS} = \pm 20\ \text{V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}$			-1	μA
		$V_{DS} = -30\ \text{V}, V_{GS} = 0\ \text{V}, T_J = 55^\circ\text{C}$			-5	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\ \text{V}, V_{GS} = -10\ \text{V}$	-30			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10\ \text{V}, I_D = -10.0\ \text{A}$		0.019	0.023	Ω
		$V_{GS} = -4.5\ \text{V}, I_D = -8.2\ \text{A}$		0.027	0.035	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15\ \text{V}, I_D = -10.0\ \text{A}$		22		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -2.9\ \text{A}, V_{GS} = 0\ \text{V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15\ \text{V}, V_{GS} = -10\ \text{V}, I_D = -10.0\ \text{A}$		38	57	nC
Gate-Source Charge	Q_{gs}			6.3		
Gate-Drain Charge	Q_{gd}			9.7		
Gate Resistance	R_g	$f = 1\ \text{MHz}$		10		Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15\ \text{V}, R_L = 15\ \Omega$ $I_D \cong -1\ \text{A}, V_{GEN} = -10\ \text{V}, R_G = 6\ \Omega$		10	15	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			130	200	
Fall Time	t_f			70	105	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -2.9\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		45	70	

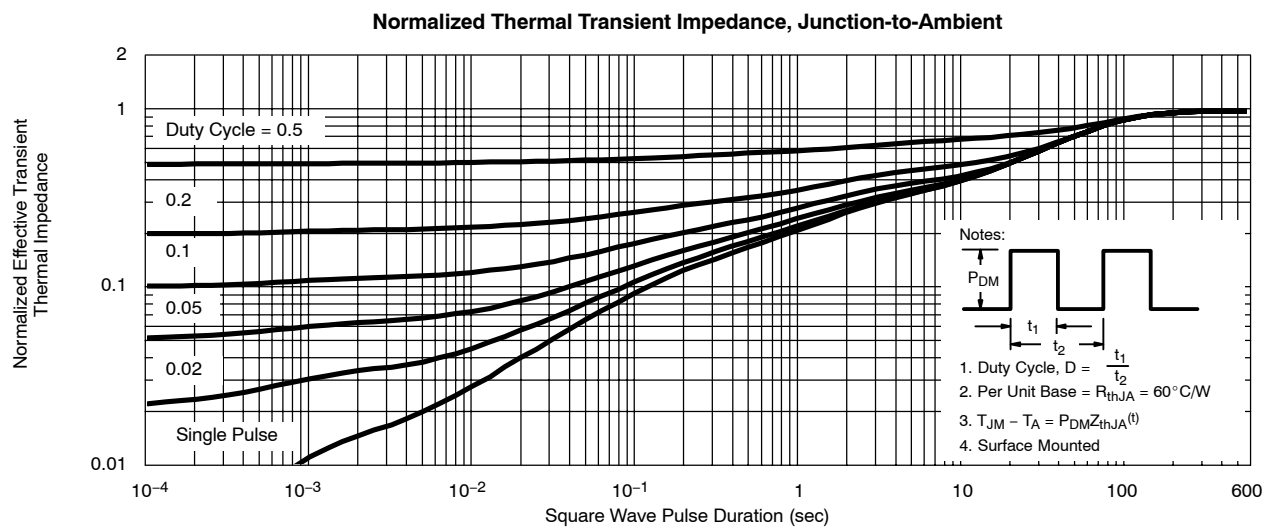
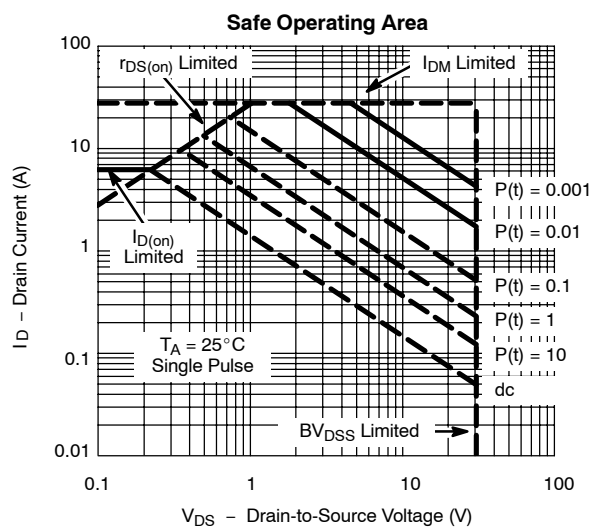
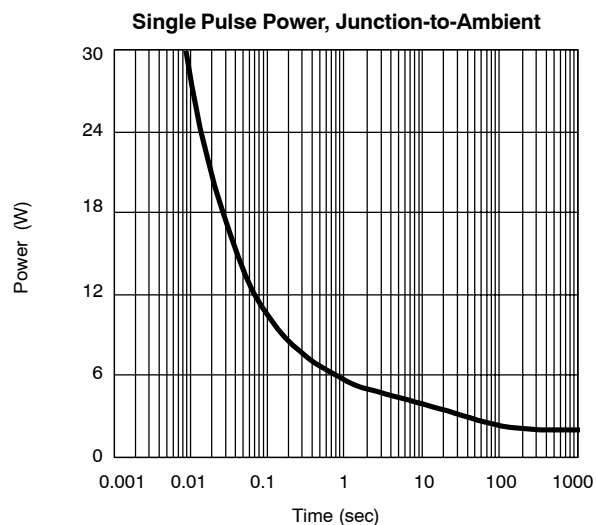
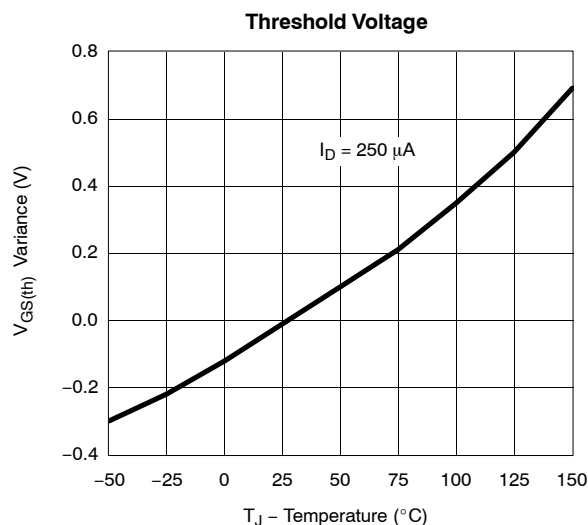
Notes

a. Pulse test; pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.

b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

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