

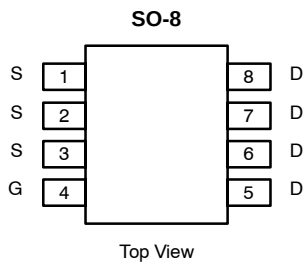


N-Channel Reduced Q_g , Fast Switching MOSFET

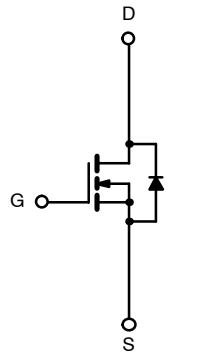
PRODUCT SUMMARY

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.022 @ $V_{GS} = 10$ V	8.5
	0.031 @ $V_{GS} = 4.5$ V	7.2

175°C Rated
Maximum Junction Temperature
TrenchFET®
Power MOSFETs



Ordering Information: Si4850EY
Si4850EY—E3 (Lead Free)
Si4850EY-T1 (with Tape and Reel)
Si4850EY-T1—E3 (Lead Free with Tape and Reel)



N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	10 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	60		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 175^\circ\text{C}$) ^a	I_D	8.5	6.0	A
		7.1	5.0	
Pulsed Drain Current	I_{DM}	40		
Avalanche Current	I_{AS}	15		
Repetitive Avalanche Energy	E_{AS}	11		mJ
Maximum Power Dissipation ^a	P_D	3.3	1.7	W
		2.3	1.2	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	36	45	$^\circ\text{C/W}$
		75	90	
Maximum Junction-to-Foot (Drain)	R_{thJF}	17	20	

Notes

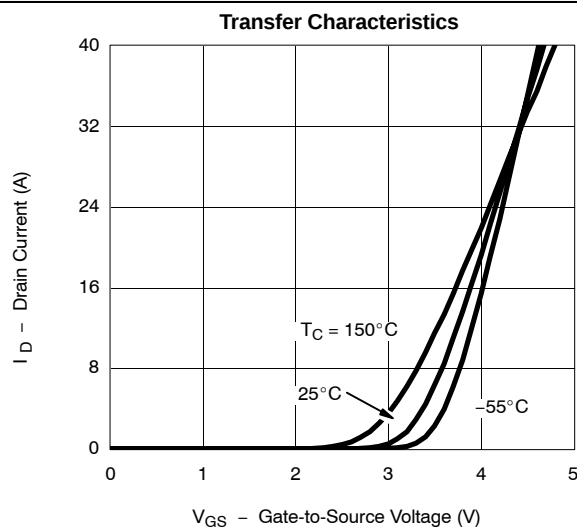
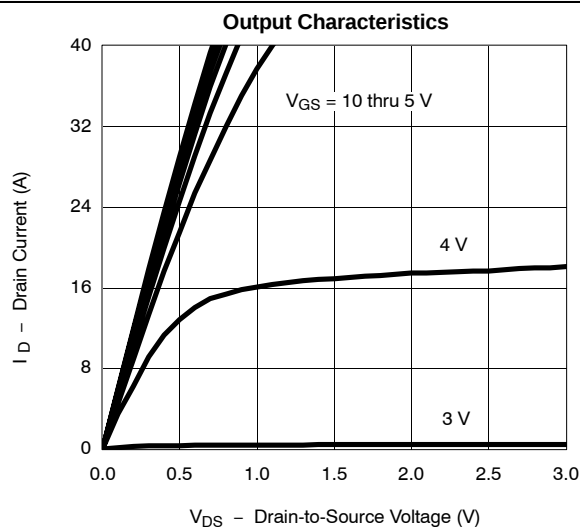
a. Surface Mounted on 1" x 1" FR4 Board.

SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			20	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 6.0\text{ A}$		0.018	0.022	Ω
		$V_{GS} = 10\text{ V}, I_D = 6.0\text{ A}, T_J = 125^\circ\text{C}$		0.031	0.037	
		$V_{GS} = 10\text{ V}, I_D = 6.0\text{ A}, T_J = 175^\circ\text{C}$		0.039	0.047	
		$V_{GS} = 4.5\text{ V}, I_D = 5.1\text{ A}$		0.025	0.031	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 6.0\text{ A}$		25		S
Diode Forward Voltage ^a	V_{SD}	$I_S = 1.7\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 6.0\text{ A}$		18	27	nC
Gate-Source Charge	Q_{gs}			3.4		
Gate-Drain Charge	Q_{gd}			5.3		
Gate Resistance	R_g	$V_{GS} = 0.1\text{ V}, f = 5\text{ MHz}$	0.5	1.4	2.4	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 30\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_g = 6\text{ }\Omega$		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	t_f			12	24	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 1.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		50	80	

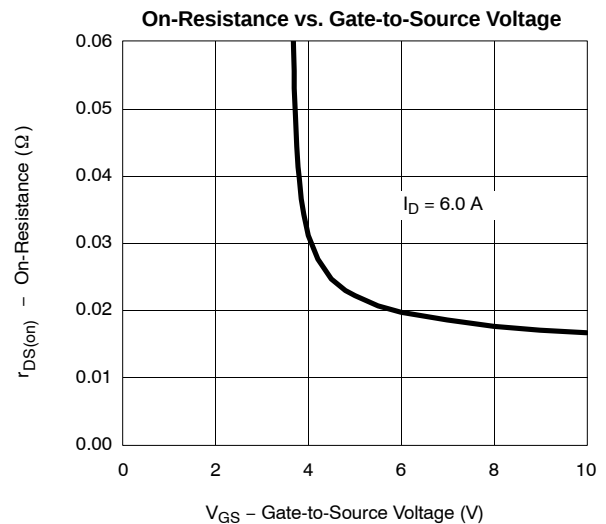
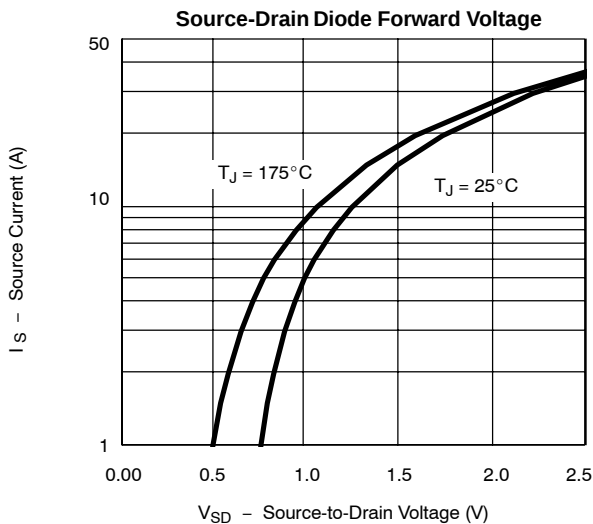
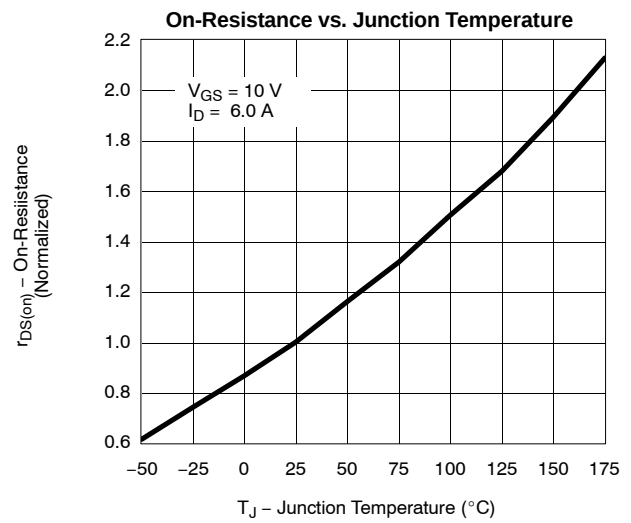
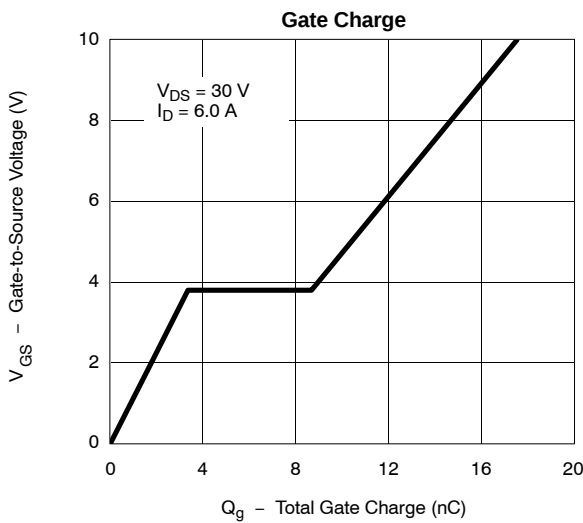
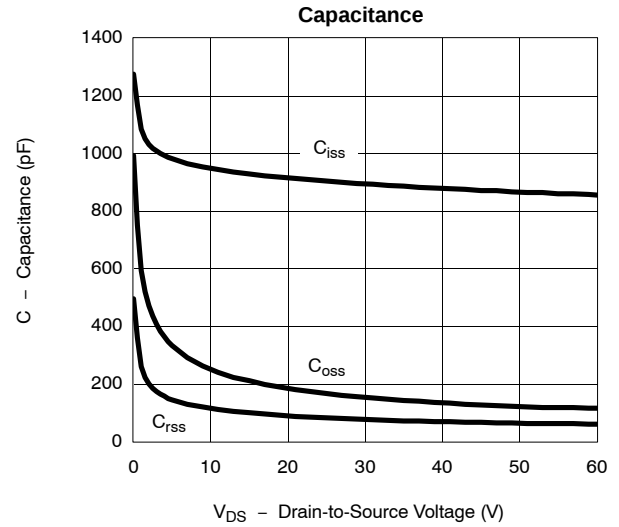
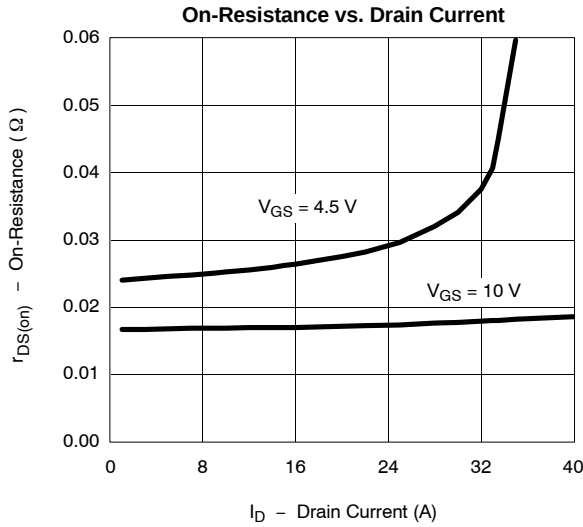
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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