



N-Channel 60-V (D-S) MOSFET

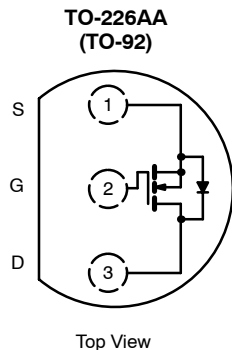
PRODUCT SUMMARY			
V_{DS} (V)	$r_{DS(on)}$ (Ω)	$V_{GS(th)}$ (V)	I_D (A)
60	2 @ $V_{GS} = 10$ V	1.0 to 2.5	0.47
	4 @ $V_{GS} = 4.5$ V		0.33

FEATURES

- TrenchFET® Power MOSFET
- ESD Protected: 2000 V

APPLICATIONS

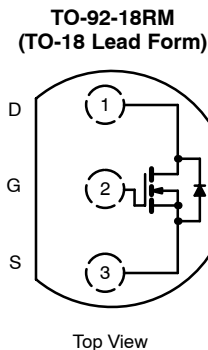
- Direct Logic-Level Interface: TTL/CMOS
- Solid State Relays
- Drivers: Relays, Solenoids, Lamps, Hammers, Displays, Memories, Transistors, etc.
- Battery Operated Systems



Device Marking Front View

"S" 2N
7000KL
xxyy

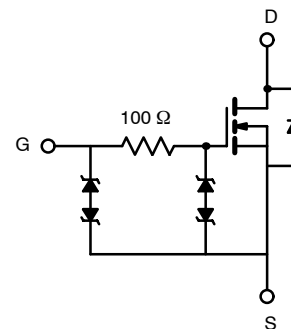
"S" = Siliconix Logo
xxyy = Date Code



Device Marking Front View

"S" BS
170KL
xxyy

"S" = Siliconix Logo
xxyy = Date Code



Ordering Information: 2N7000KL-TR1

Ordering Information: BS170KL-TR1

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_A = 25^\circ\text{C}$	I_D	0.47	A
	$T_A = 70^\circ\text{C}$		0.37	
Pulsed Drain Current ^a		I_{DM}	1.0	
Power Dissipation	$T_A = 25^\circ\text{C}$	P_D	0.8	W
	$T_A = 70^\circ\text{C}$		0.51	
Maximum Junction-to-Ambient		R_{thJA}	156	$^\circ\text{C/W}$
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Notes

a. Pulse width limited by maximum junction temperature.

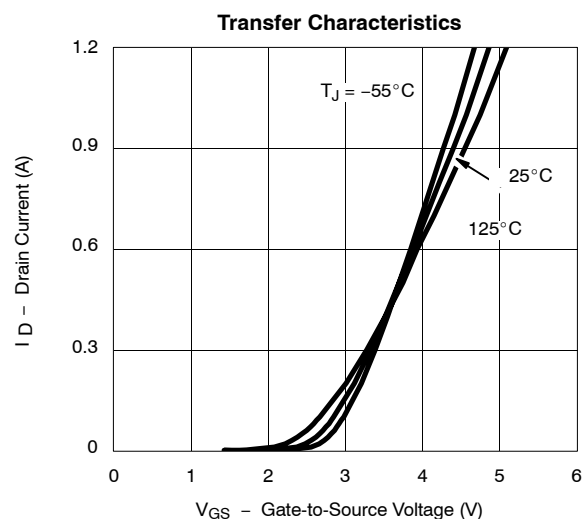
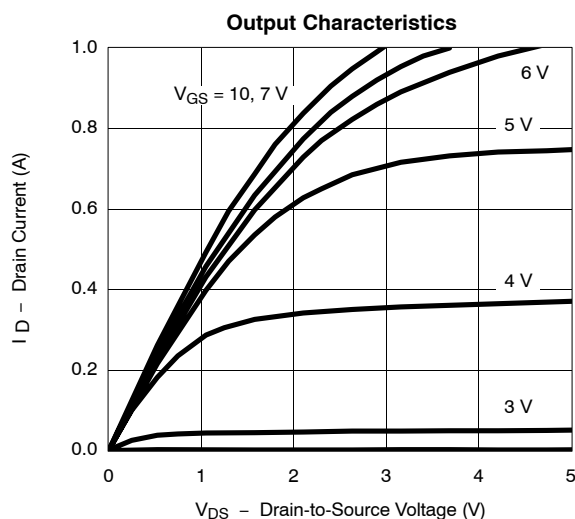
SPECIFICATIONS^a ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

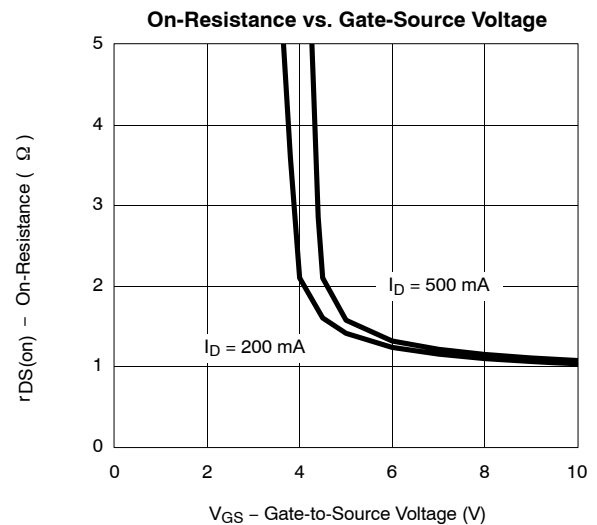
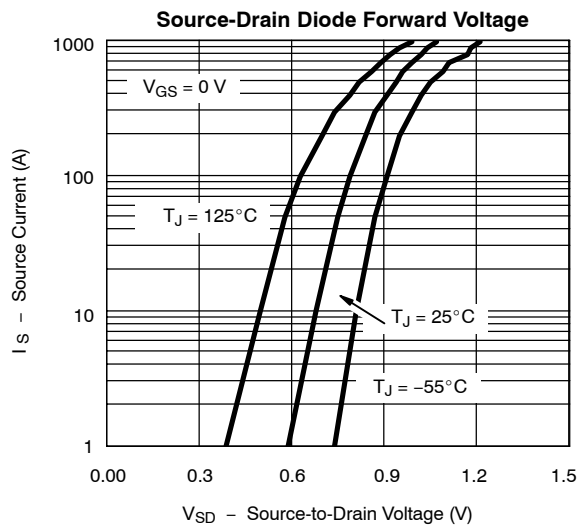
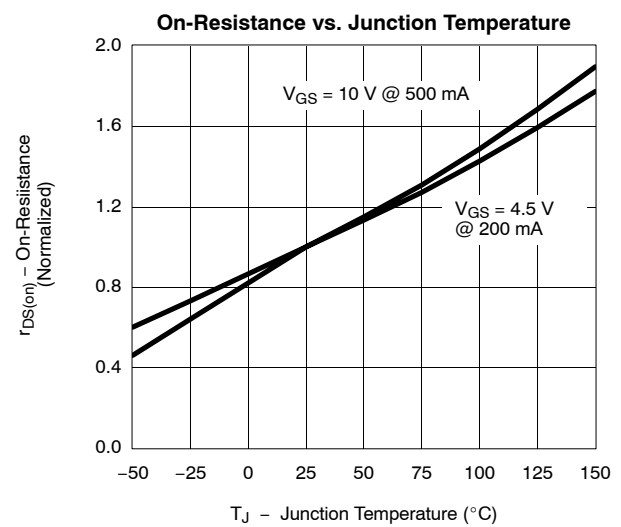
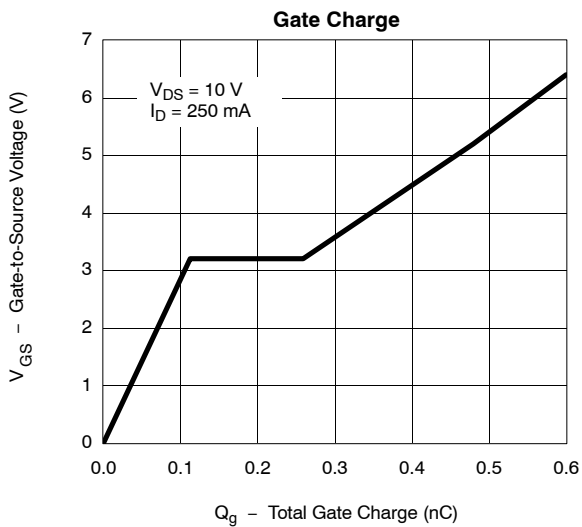
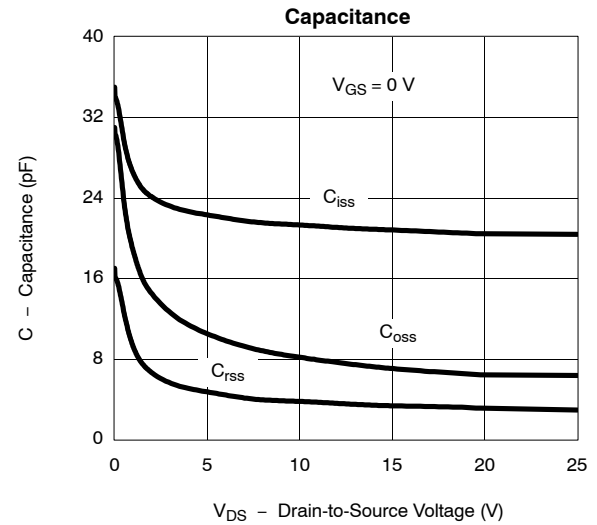
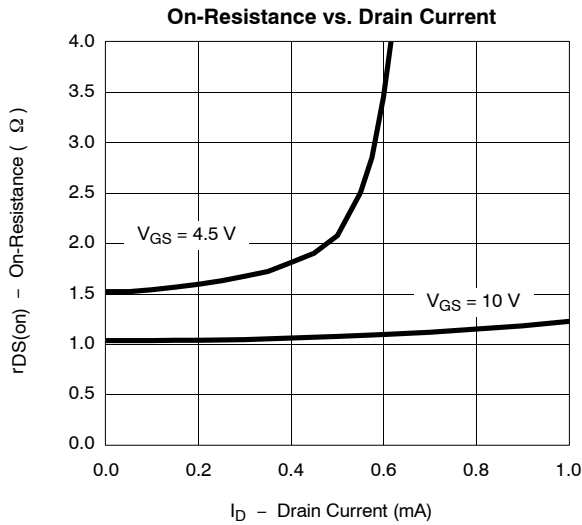
Parameter	Symbol	Test Conditions	Limits			Unit
			Min	Typ	Max	
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 10\text{ }\mu\text{A}$	60			V
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1	2.0	2.5	
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 10\text{ V}$			± 1	μA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			10	
On-State Drain Current ^b	$I_{D(on)}$	$V_{GS} = 10\text{ V}, V_{DS} = 7.5\text{ V}$	0.8			A
		$V_{GS} = 4.5\text{ V}, V_{DS} = 10\text{ V}$	0.5			
Drain-Source On-Resistance ^b	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 0.5\text{ A}$		1.1	2	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 0.2\text{ A}$		1.6	4	
Forward Transconductance ^b	g_{fs}	$V_{DS} = 10\text{ V}, I_D = 0.5\text{ A}$		550		mS
Diode Forward Voltage	V_{SD}	$I_S = 0.3\text{ A}, V_{GS} = 0\text{ V}$		0.87	1.3	V
Dynamic ^b						
Total Gate Charge	Q_g	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}$ $I_D \approx 0.25\text{ A}$		0.4	0.6	nC
Gate-Source Charge	Q_{gs}			0.11		
Gate-Drain Charge	Q_{gd}			0.15		
Gate Resistance	R_g			173		Ω
Turn-On Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 150\text{ }\Omega$ $I_D \approx 0.2\text{ A}, V_{GEN} = 10\text{ V}$ $R_g = 10\text{ }\Omega$		3.8	10	ns
	t_r			4.8	15	
Turn-Off Time	$t_{d(off)}$			12.8	20	
	t_f			9.6	15	

Notes

a. Pulse test: $PW \leq 300\text{ }\mu\text{s}$ duty cycle $\leq 2\%$.

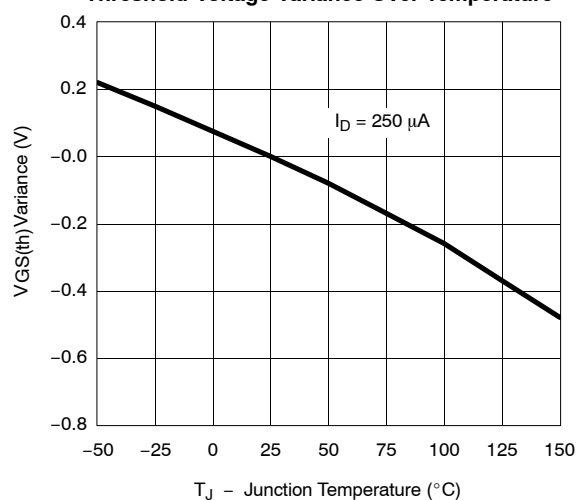
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

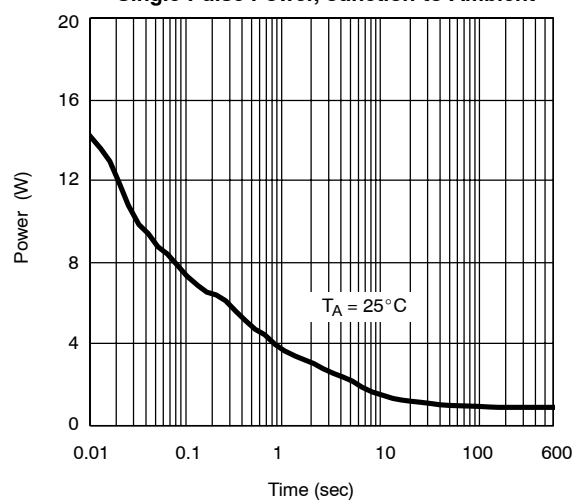
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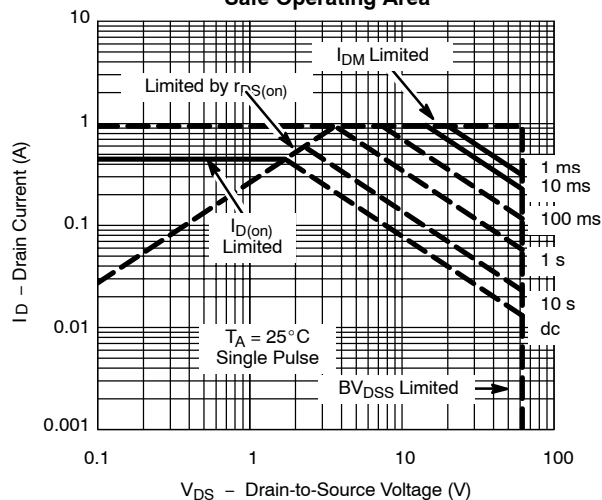
Threshold Voltage Variance Over Temperature



Single Pulse Power, Junction-to-Ambient



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

