



DOCUMENT NUMBER AND REVISION
VL-FS-MGLS12864TZ-10 REV. A
(MGLS12864TZ-HT-LED03)

DOCUMENT TITLE:
SPECIFICATION
OF
LCD MODULE TYPE
MODULE NO.: MGLS12864TZ-10

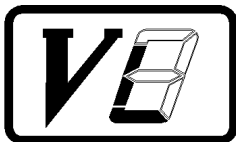
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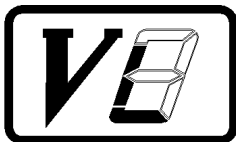
DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO	DATE	DESCRIPTION	CHANGED BY	CHECKED BY
A	2004.05.25	First Release. Based on a.) Test Specification VL-TS-MGLS12864TZ-XX REV.I, 2004-05-25. b.) VL-QUA-012A, REV. R, 2004.03.20. According to VL-QUA-012A, LCD size is small because Unit Per Laminate=12 which is more than 6pcs/Laminate.	ZHU LING JUN	TANG ZHAO BIN



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Specification of LCD Module Type Model No.: MGLS12864TZ-10

1. General Description

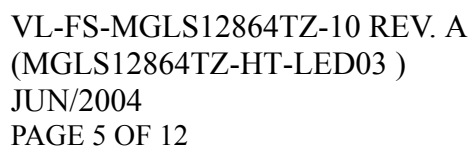
- 128 x 64 dot matrix STN Positive Yellow Transflective LCD graphic module.
- Driving scheme: 1/64 duty, 1/9 bias.
- Viewing direction: 6 O'clock.
- 'TOSHIBA' T6963C-0101 (Flat pack) or equivalent LCD controller.
- 'DRAGON DRIVER' SA3086A (Die form) LCD Segment/Common Drivers or equivalent.
- 8K bytes display SRAM.
- Yellow-Green LED03 backlight.

2. Mechanical Specifications

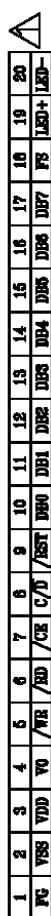
The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	78.0(W) x 70.0(H) x 13.5 MAX. (D)	mm
Viewing area	62.0(W) x 44.0(H)	mm
Active area	56.27(W) x 38.35(H)	mm
Display format	128(Horizontal) x 64(Vertical)	dots
Dot size	0.39(W) x 0.55(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.44(W) x 0.60(H)	mm
Weight	TBD	grams



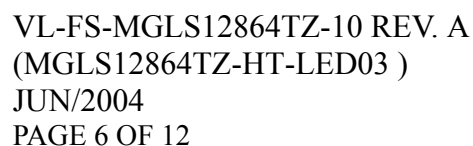
TITLE: SPECIFICATION OF MODULE	
PROJECT NO: MGLS12864TZ	
TOLERANCE IN MM X.X ± 0.3 X.XX ± 0.1	
MATERIAL:	FINISH:
TOLERANCES DO NOT ON SCALE	
THICKNESS:	
THIRD ANGLE PROJECTION	
NAME	SIGN DATE
DRAWN	WAI YONG LING
CHECKED	TANG ZHAO BEN
APPROVED	CHARM
ITEM NO. MGLS12864TZ-XX	
DESCRIPTION: MGLS12864TZ	
FILE NO: MGLS12864TZ-XX R2.DWG REV 2	
QUANTITY	NO.



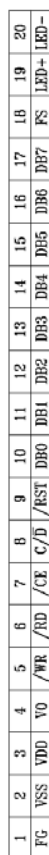
NOTES: 1. ♦ : SPECIAL CHARACTERISTIC
2. + : SAFETY CHARACTERISTIC
3 ▽ : CRITICAL DIMENSION
4.(...): REFERENCE DIMENSION


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Figure 1(a): Module Specification 1



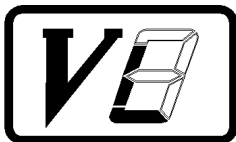
TITLE: SPECIFICATION OF MODULE			
PROJECT NO: MGLS12864TZ			
TO EXAM: UNL358		XX ± 0.3	
WHENEVER SPECIFIED:		XXX ± 0.1	
DIMENSIONS IN MM		FINISH:	
MATERIAL:		THICKNESS:	
THIRD ANGLE PROJECTION			
NAME		SIGN	DATE
DRAWN	WAI YONGLIANG		
CHECKED	TANG ZHAOBIN		
APPROVED	CHARM		
ITEM NO. MGLS12864TZ-XX			
DESCRIPTION: MGLS12864TZ			
FILE NO: MGLS12864TZ-XX R2.DWG REV 2			
SHEET		OF	



* T6963C OR EQUIVALENT


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Figure 1(b): Module Specification 2

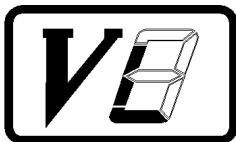


3. Interface signals

Table 2

Pin No.	Symbol	Description
1	FG	Frame ground (see note 1).
2	VSS	Ground (0V).
3	VDD	Power supply for logic (+5V).
4	V0	Power supply for LCD drive.
5	/WR	Data write. Write data to controller T6963C when "L".
6	/RD	Data read. Read data from controller T6963C when "L".
7	/CE	Chip enable for T6963C. /CE must be "Low" when CPU communicates with T6963C.
8	C/D	/WR = "Low" C/D = "High": Command Write C/D = "Low": Data Write. /RD = "Low" C/D = "High": Status Read C/D = "Low": Data Read.
9	/RST	"High": Normal (T6963C has internal pull-up resistor). "Low": Initialize T6963C. Text and graphic have addresses and text and graphic area settings are retained.
10	DB0	Data input/output (LSB).
11	DB1	Data input/output.
12	DB2	Data input/output.
13	DB3	Data input/output.
14	DB4	Data input/output.
15	DB5	Data input/output.
16	DB6	Data input/output.
17	DB7	Data input/output (MSB).
18	FS	Font select. "H" for 6 x 8 font & "L" for 8 x 8 font
19	LED+	Anode of LED backlight
20	LED-	Cathode of LED backlight

Note 1: This pin is electrically connected to the metal bezel (frame).
User can choose to connect this pin to VSS or leave it open.



4. Absolute Maximum Ratings

4.1 Electrical Maximum Ratings (Ta = 25 °C)

Table 3

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Supply voltage (LCD drive)	VLCD=VDD – V0	0	+30.0	V
Input voltage	Vin	-0.3	VDD +3.0	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

4.2 Environmental Condition

Table 4

Item	Operating Temperature (Topr)		Storage Temperature (Tstg)		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity	95% max. RH for Ta ≤ 40°C < 95% RH for Ta > 40°C				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: 981 m/s ² = 100g Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions



5. Electrical Specifications

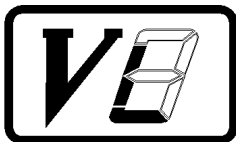
5.1 Typical Electrical Characteristics

At $T_a = 25\text{ }^{\circ}\text{C}$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	VDD-VSS		4.75	5.0	5.25	V
Supply voltage (LCD)	VLCD =VDD-V0	VDD = 5V, Note (1)	15.5	16.0	16.5	V
Input signal voltage	VIN	“H” level	VDD-2.2	-	VDD	V
		“L” level	0	-	0.8	V
Supply current (Logic & LCD)	IDD	Character mode, VDD = 5V. Note (1)	-	7.3	11.0	mA
		Checker board mode, VDD = 5V. Note (1)	-	7.5	11.3	mA
Supply Current (LCD)	I0	Character mode, Note (1)	-	3.4	5.1	mA
		Checker board mode, Note (1)	-	3.4	5.1	mA
Supply current of yellow-green LED03 backlight	VLED03	Forward current =100mA No. of LED chips =20.	3.8	4.0	4.2	V

Note (1): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.



5.2 Timing Specifications

At $T_a = -20^{\circ}\text{C}$ To $+70^{\circ}\text{C}$, $V_{DD} = 5\text{V} \pm 5\%$, $V_{SS} = 0\text{V}$

Refer to Fig. 3, the bus timing diagram.

Table 6

Parameter	Symbol	Min.	Max.	Unit
C/ $\overline{\text{D}}$ Set-up time	t_{CDS}	100	-	ns
C/ $\overline{\text{D}}$ Hold Time	t_{CDH}	10	-	ns
/CE,/RD,/WR Pulse Width	$t_{\text{CE}}, t_{\text{RD}}, t_{\text{WR}}$	80	-	ns
Data Set-up Time	t_{DS}	80	-	ns
Data Hold Time	t_{DH}	40	-	ns
Access Time	t_{ACC}	-	150	ns
Output Hold Time	t_{OH}	10	50	ns

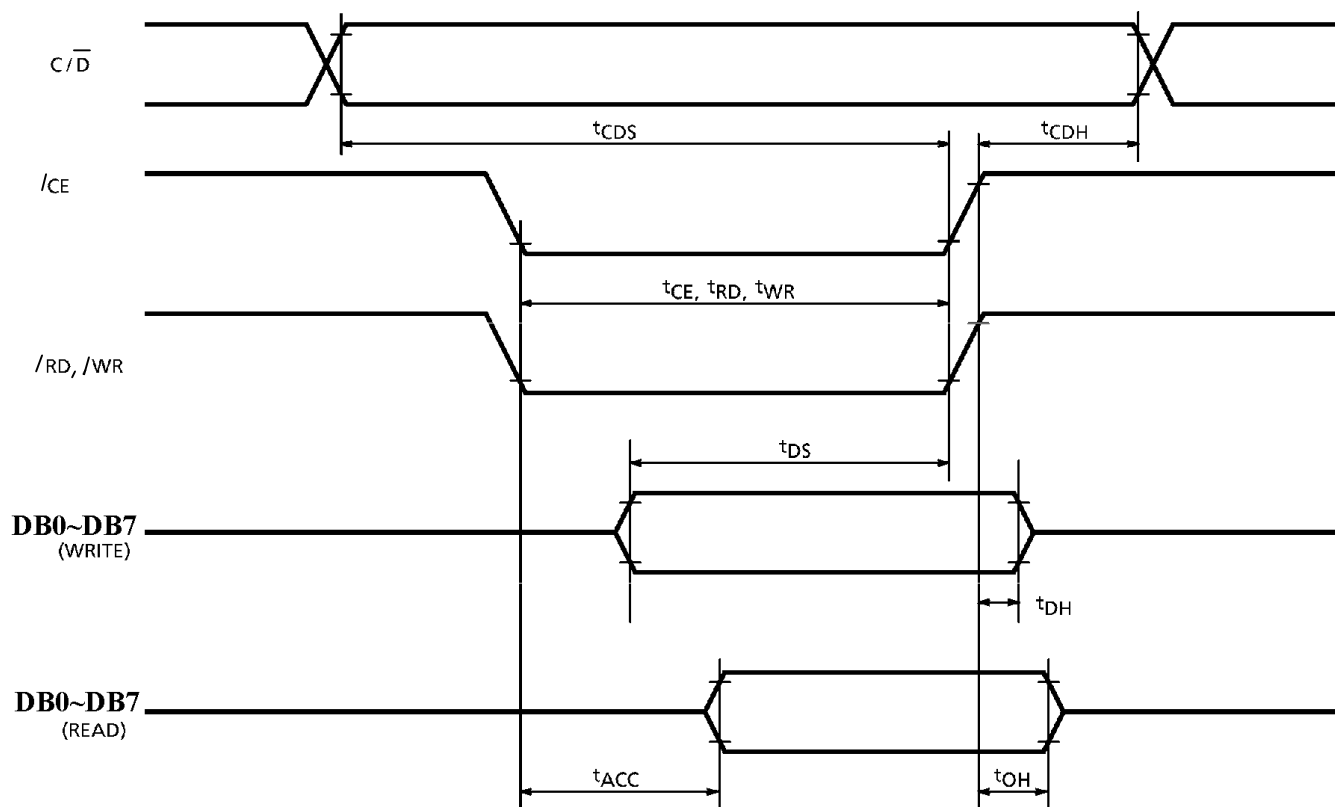
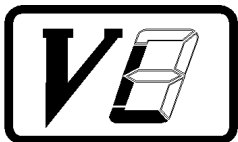


Figure 2: Bus Timing Diagram



5.3 Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 4, the timing diagram of VDD against V0.

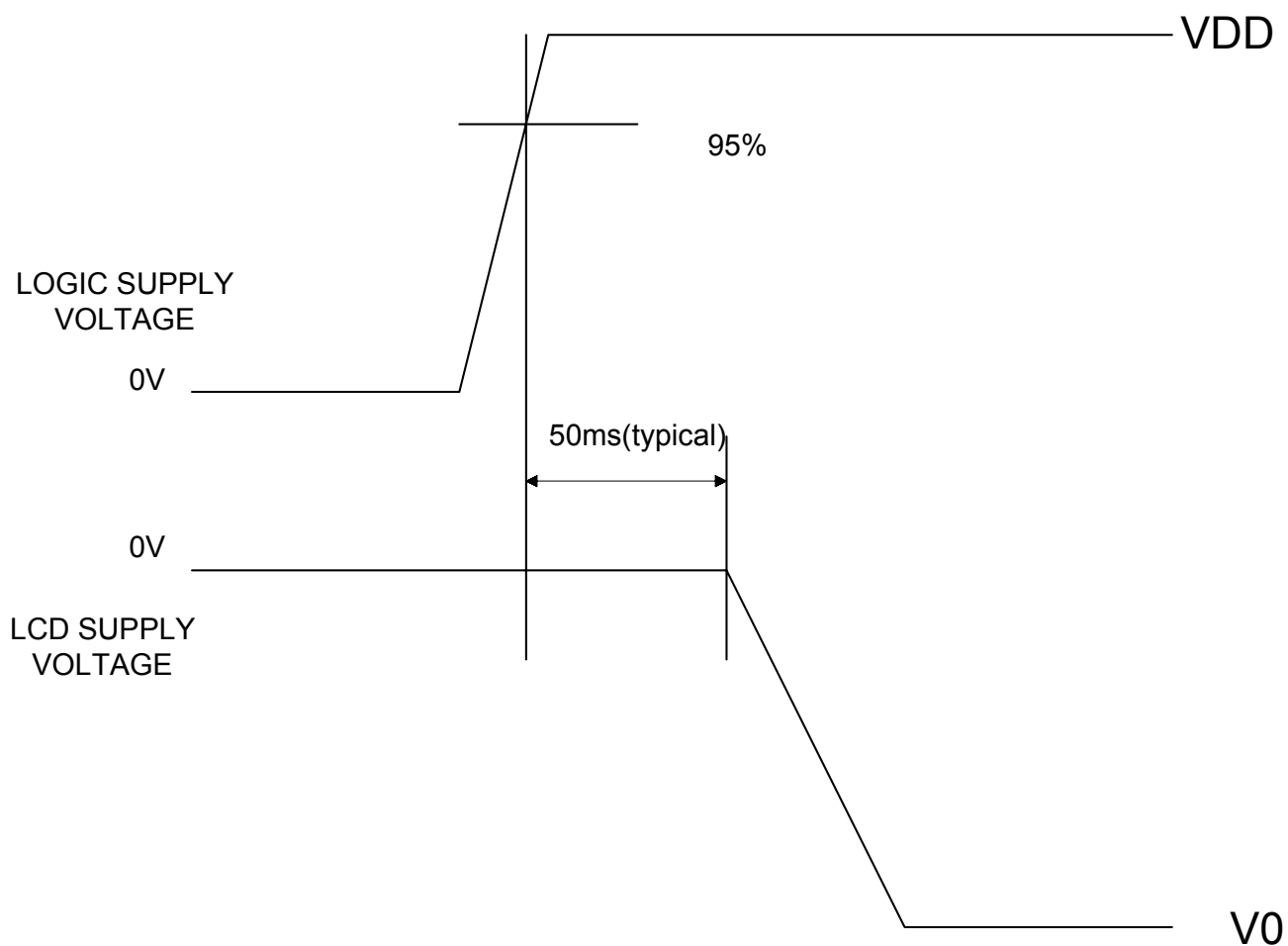
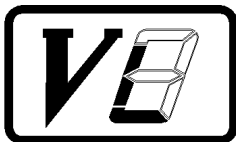


Figure 3: Timing Diagram of VDD Against V0.



6.0 LCD Cosmetic Conditions.

Refer to VL-QUA-012A.

Remark: LCD size of the product is small.

“Varitronix Limited reserves the right to change this specification.”

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URL:<http://www.varitronix.com>

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