

TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

TC74HC4051AP, TC74HC4051AF, TC74HC4051AFT
TC74HC4052AP, TC74HC4052AF, TC74HC4052AFT
TC74HC4053AP, TC74HC4053AF, TC74HC4053AFN, TC74HC4053AFT

TC74HC4051AP/AF/AFT 8-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
TC74HC4052AP/AF/AFT DUAL 4-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER
TC74HC4053AP/AF/AFN/AFT TRIPLE 2-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

The TC74HC4051A/4052A/4053A are high speed CMOS ANALOG MULTIPLEXER/DEMULTIPLEXER fabricated with silicon gate C²MOS technology. They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The TC74HC4051A has an 8 channel configuration, the TC74HC4052A has a 4 channel×2 configuration and the TC74HC4053A has a 2 channel×3 configuration.

The digital signal to the control terminal turns "ON" the corresponding switch of each channel a large amplitude signal ($V_{CC}-V_{EE}$) can then be switched by the small logical amplitude ($V_{CC}-GND$) control signal.

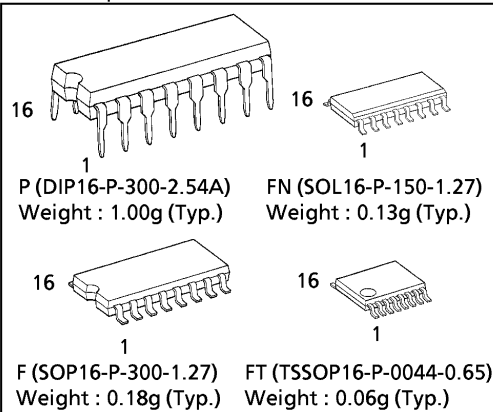
For example, in the case of $V_{CC}=5V$, $GND=0V$, $V_{EE}=-5V$, signals between -5V and +5V can be switched from the logical circuit with a single power supply of 5V. As the ON-resistance of each switch is low, they can be connected to circuits with low input impedance.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

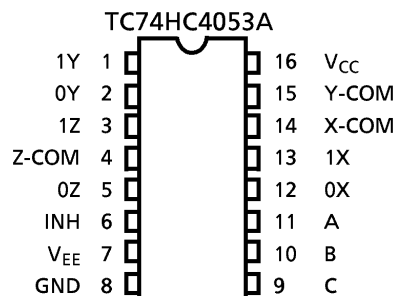
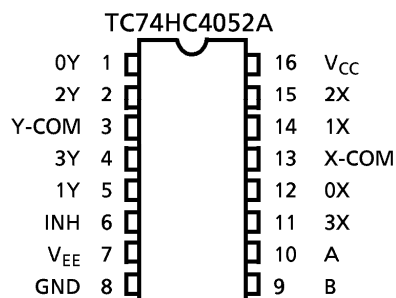
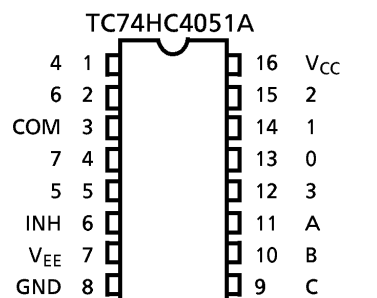
FEATURES:

- High Speed..... $t_{pd} = 15ns$ (typ.) at $V_{CC} = 5V$
 $V_{EE} = 0V$
- Low Power Dissipation..... $I_{CC} = 4\mu A$ (Max.) at $T_a = 25^\circ C$
- High Noise Immunity..... $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (Min.)
- Low ON Resistance..... $R_{ON} = 50\Omega$ (typ.)
at $V_{CC}-V_{EE} = 9V$
- High Noise Immunity..... $THD = 0.02\%$ (typ.)
at $V_{CC}-V_{EE} = 9V$
- Pin and Function Compatible with 4051/4052/4053B

(Note) The JEDEC SOP (FN) is not available in Japan.



PIN ASSIGNMENT



(TOP VIEW)

TRUTH TABLE

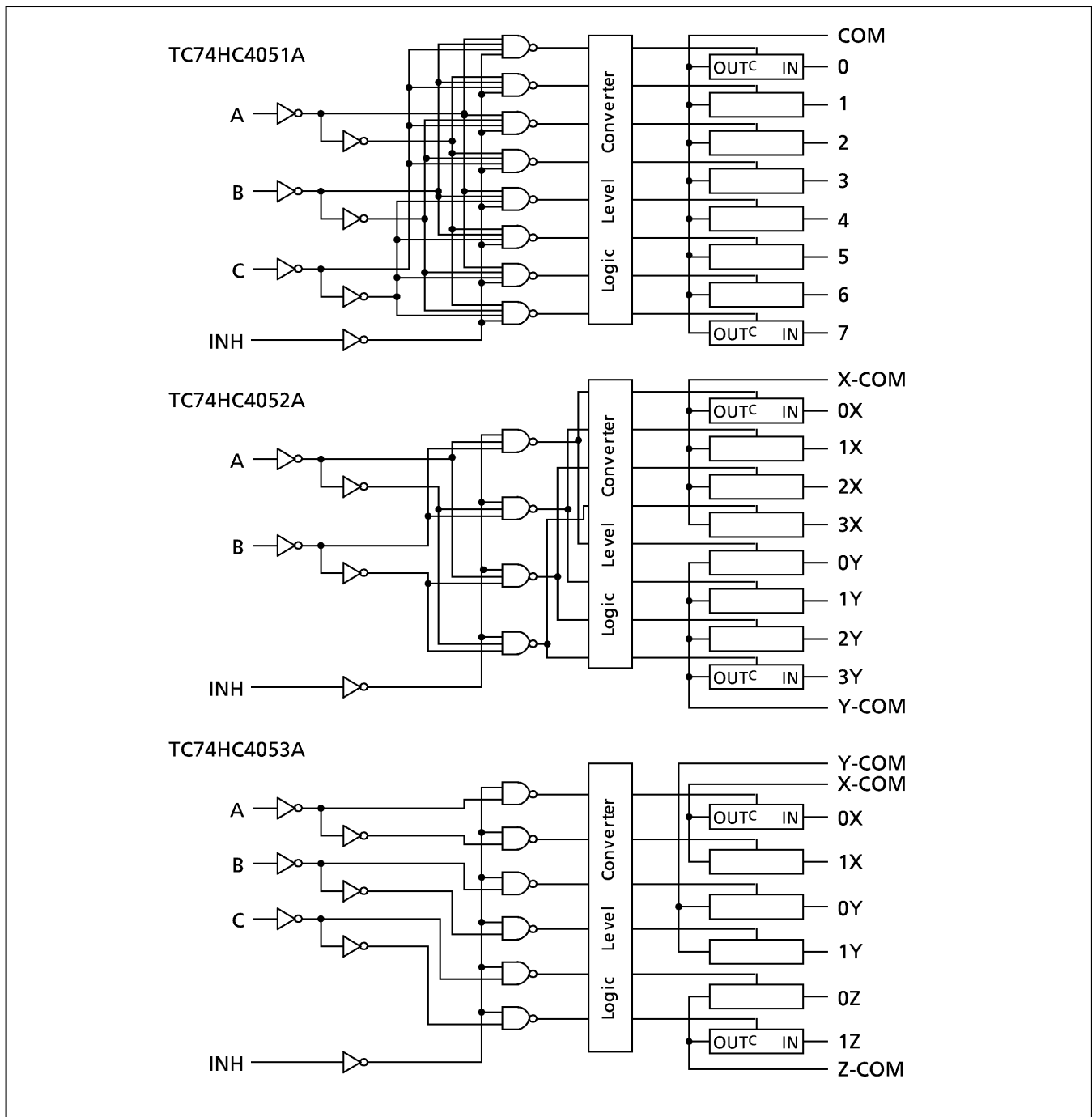
CONTROL INPUTS				"ON" CHANNEL		
INHIBIT	C*	B	A	HC4051A	HC4052A	HC4053A
L	L	L	L	0	0X, 0Y	0X,0Y,0Z
L	L	L	H	1	1X, 1Y	1X,0Y,0Z
L	L	H	L	2	2X, 2Y	0X,1Y,0Z
L	L	H	H	3	3X, 3Y	1X,1Y,0Z
L	H	L	L	4	--	0X,0Y,1Z
L	H	L	H	5	--	1X,0Y,1Z
L	H	H	L	6	--	0X,1Y,1Z
L	H	H	H	7	--	1X,1Y,1Z
H	X	X	X	NONE	NONE	NONE

X: Don't Care, *: Except HC4052A

961001EBA2

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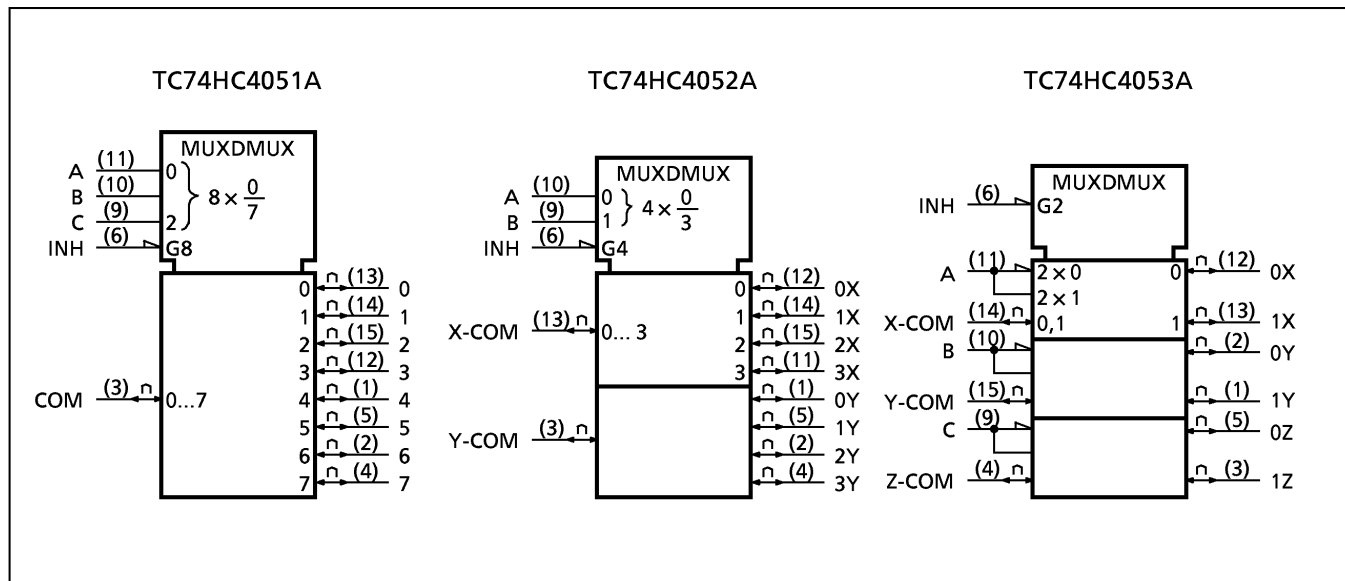
SYSTEM DIAGRAM



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IEC LOGIC SYMBOL



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$-0.5 \sim 7$	V
Supply Voltage Range	$V_{CC} - V_{EE}$	$-0.5 \sim 13$	V
Control Input Voltage	V_{IN}	$-0.5 \sim V_{CC} + 0.5$	V
Switch I/O Voltage	$V_{I/O}$	$V_{EE} - 0.5 \sim V_{CC} + 0.5$	V
Control Input Diode Current	I_{ICK}	± 20	mA
I/O Diode Current	I_{IOK}	± 20	mA
Switch through Current	I_T	± 25	mA
DC V_{CC} or Ground Current	I_{CC}	± 50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP, TSSOP)	mW
Storage Temperature	T_{stg}	$-65 \sim 150$	°C

*500mW in the range of $T_a = -40^\circ\text{C} \sim 65^\circ\text{C}$. From $T_a = 65^\circ\text{C}$ to 85°C a derating factor of $-10\text{mW}/^\circ\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	$2 \sim 6$	V
Supply Voltage Range	V_{EE}	$-6 \sim 0$	V
Supply Voltage Range	$V_{CC} - V_{EE}$	$2 \sim 12$	V
Control Input Voltage	V_{IN}	$0 \sim V_{CC}$	V
Switch I/O Voltage	$V_{I/O}$	$V_{EE} \sim V_{CC}$	V
Operating Temperature	T_{opr}	$-40 \sim 85$	°C
Control Input Rise and Fall Time	t_r, t_f	$0 \sim 1000 (V_{CC} = 2.0\text{V})$ $0 \sim 500 (V_{CC} = 4.5\text{V})$ $0 \sim 400 (V_{CC} = 6.0\text{V})$	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{EE} (V)	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim 85^\circ\text{C}$		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
High - Level Control Input Voltage	V_{IHC}			2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low - Level Control Input Voltage	V_{ILC}			2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	
ON Resistance	R_{ON}	$V_{IN} = V_{ILC}$ or V_{IHC} $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O} \leq 2\text{mA}$	GND — 4.5 — 6.0	4.5 4.5 6.0	— — —	85 55 50	180 120 100	— — —	225 150 125	Ω
		$V_{IN} = V_{ILC}$ or V_{IHC} $V_{I/O} = V_{CC}$ or V_{EE} $I_{I/O} \leq 2\text{mA}$	GND GND — 4.5 — 6.0	2.0 4.5 4.5 6.0	— — — —	150 70 50 45	— 150 100 80	— — — —	— 190 125 100	
Difference of ON Resistance Between Switches	ΔR_{ON}	$V_{IN} = V_{ILC}$ or V_{IHC} $V_{I/O} = V_{CC}$ to V_{EE} $I_{I/O} \leq 2\text{mA}$	GND — 4.5 — 6.0	4.5 4.5 6.0	— — —	10 5 5	30 12 10	— — —	35 15 12	
Input / Output Leakage Current (SWITCH OFF)	I_{OFF}	$V_{OS} = V_{CC}$ or GND $V_{IS} = \text{GND}$ or V_{CC} $V_{IN} = V_{ILC}$ or V_{IHC}	GND — 6.0	6.0 6.0	— —	— —	± 60 ± 100	— —	± 600 ± 1000	nA
Switch Input Leakage Current (SWITCH ON)	I_{IZ}	$V_{OS} = V_{CC}$ or GND $V_{IN} = V_{ILC}$ or V_{IHC}	GND — 6.0	6.0 6.0	— —	— —	± 60 ± 100	— —	± 600 ± 1000	
Control Input Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	GND	6.0	—	—	± 0.1	—	± 1.0	μA
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	GND — 6.0	6.0 6.0	— —	— —	4.0 8.0	— —	40.0 80.0	

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$, GND = 0V)

PARAMETER	SYMBOL	TEST CONDITION	V_{EE} (V)	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
					MIN.	TYP.	MAX.	MIN.	MAX.	
Phase difference between Input and Output	ϕ I/O	ALL TYPES	GND GND GND -4.5	2.0 4.5 6.0 4.5	— — — —	25 6 5 4	60 12 10 —	— — — —	75 15 13 —	ns
Output Enable Time	t_{pZL} t_{pZH}	*1 4051	GND GND GND -4.5	2.0 4.5 6.0 4.5	— — — —	64 18 15 18	225 45 38 —	— — — —	280 56 48 —	
			GND GND GND -4.5	2.0 4.5 6.0 4.5	— — — —	64 18 15 18	225 45 38 —	— — — —	280 56 48 —	
			GND GND GND -4.5	2.0 4.5 6.0 4.5	— — — —	50 14 12 14	225 45 38 —	— — — —	280 56 48 —	
		*1 4052	GND GND GND -4.5	2.0 4.5 6.0 4.5	— — — —	100 33 28 29	250 50 43 —	— — — —	315 63 54 —	
			GND GND GND -4.5	2.0 4.5 6.0 4.5	— — — —	100 33 28 29	250 50 43 —	— — — —	315 63 54 —	
			GND GND GND -4.5	2.0 4.5 6.0 4.5	— — — —	95 30 26 26	225 45 38 —	— — — —	280 56 48 —	
Control Input Capacitance	C_{in}	ALL TYPES	—	—	—	5	10	—	10	pF
COMMON Terminal Capacitance	C_{IS}	4051 4052 4053	— 5.0	5.0	— — —	36 19 11	70 40 20	— — —	70 40 20	
SWITCH Terminal Capacitance	C_{OS}	4051 4052 4053	— 5.0	5.0	— — —	7 7 7	15 15 15	— — —	15 15 15	
Feedthrough Capacitance	C_{IOS}	4051 4052 4053	— 5.0	5.0	— — —	0.95 0.85 0.75	2 2 2	— — —	2 2 2	
Power Dissipation Capacitance	C_{PD}	*2 4051 4052 4053	GND	5.0	— — —	70 71 67	— — —	— — —	— — —	

* 1: $R_L = 1\text{k}\Omega$ * 2: C_{PD} is defined as the value of the internal equivalent capacitance of IC which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation :

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

ANALOG SWITCH CHARACTERISTICS (GND = 0V, Ta = 25°C)

PARAMETER	SYMBOL	TEST CONDITION		V _{EE} (V)	V _{CC} (V)	TYP.	UNIT
Sine Wave Distortion (T . H . D)		RL = 10kΩ CL = 50pF fIN = 1kHz	VIN = 4.0VP-P VIN = 8.0VP-P VIN = 11.0VP-P	- 2.25 - 4.5 - 6.0	2.25 4.5 6.0	0.025 0.020 0.018	%
Frequency Response (Switch ON)	fMAX	Adjust fIN Voltage to obtain 0dBm at VOS Increase fIN Frequency until dB Meter reads - 3dB RL = 50Ω, CL = 10pF fIN = 1MHz, Sine Wave	*1 ALL	- 2.25	2.25	120	MHz
			*2 4051 4052 4053			45 70 95	
			*1 ALL	- 4.5	4.5	190	
			*2 4051 4052 4053			70 110 150	
			*1 ALL	- 6.0	6.0	200	
			*2 4051 4052 4053			85 140 190	
Feed through Attenuation (Switch OFF)		Vin is centered at (VCC - VEE) / 2 Adjust input for 0dBm RL = 600Ω, CL = 50pF fIN = 1MHz, Sine Wave	- 2.25 - 4.5 - 6.0	2.25 4.5 6.0	- 50 - 50 - 50	dB	
Crosstalk (Control Input to Signal Output)		RL = 600Ω, CL = 50pF fIN = 1MHz, Square Wave (tr = tf = 6ns)	- 2.25 - 4.5 - 6.0	2.25 4.5 6.0	60 140 200	mV	
Crosstalk (Between any switches)		Adjust VIN to obtain 0dBm at Input RL = 600Ω, CL = 50pF fIN = 1MHz, Sine Wave	- 2.25 - 4.5 - 6.0	2.25 4.5 6.0	- 50 - 50 - 50	dB	

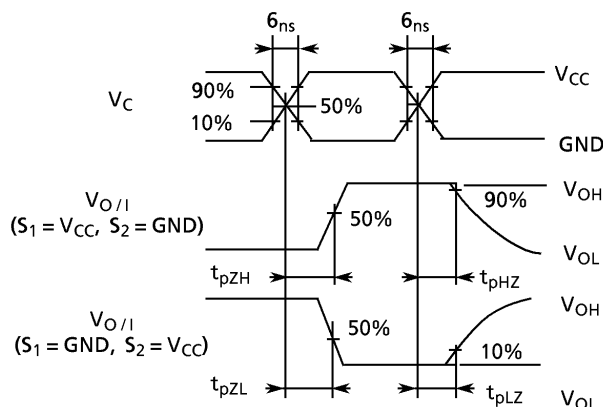
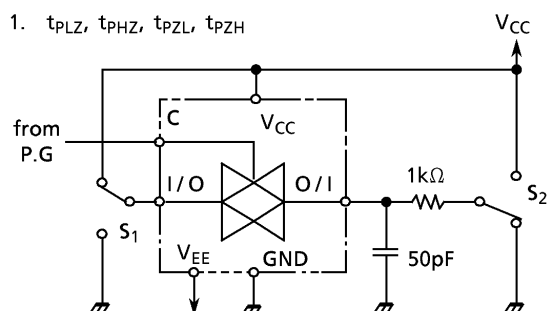
* 1 : Input COMMON Terminal, and measured at SWITCH Terminal.

* 2 : Input SWITCH Terminal, and measured at COMMON Terminal.

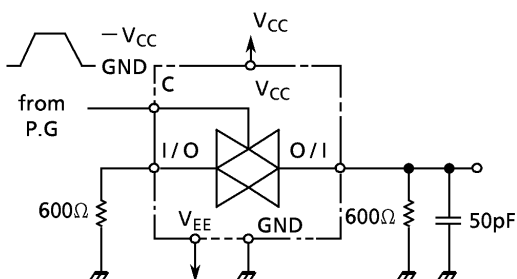
NOTE : These characteristics are determined by design of devices.

SWITCHING CHARACTERISTICS TEST CIRCUITS

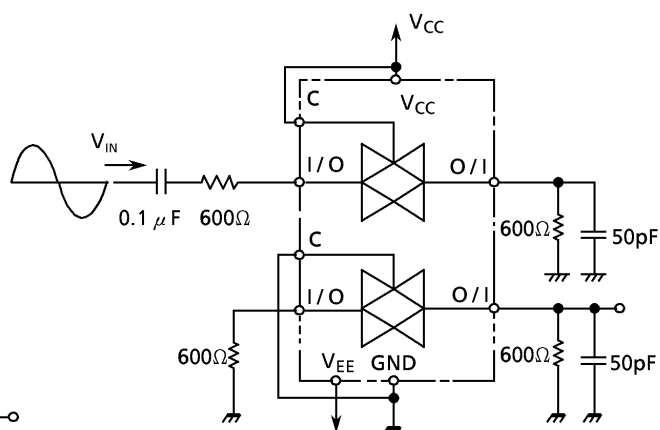
1. t_{PLZ} , t_{PHZ} , t_{PZL} , t_{PZH}



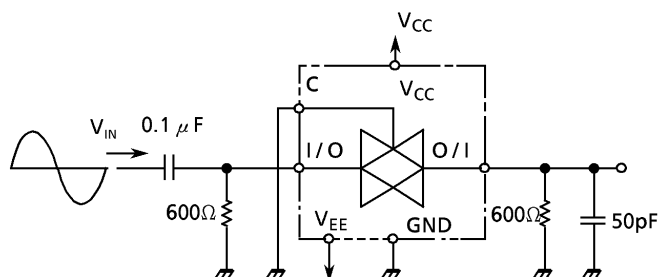
2. CROSS TALK (CONTROL INPUT – SWITCH OUTPUT)
 $f_{in} = 1\text{MHz}$ duty = 50% $t_r = t_f = 6\text{ns}$



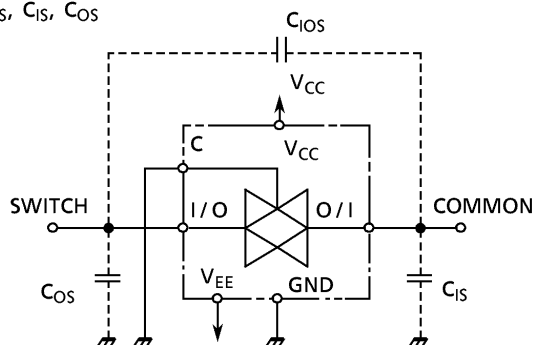
5. CROSS TALK (BETWEEN ANY TWO SWITCHES)



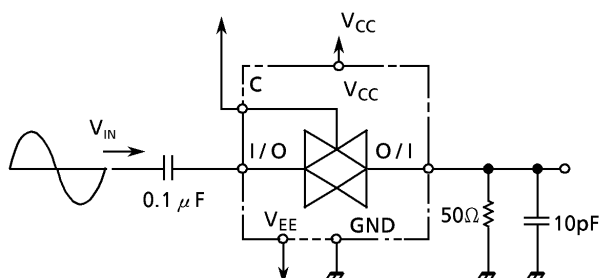
3. FEEDTHROUGH ATTENUATION



4. C_{IOS} , C_{IS} , C_{OS}

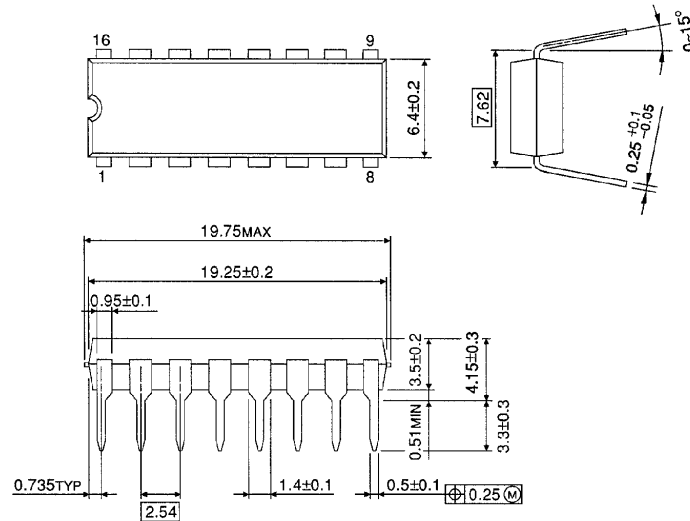


6. FREQUENCY RESPONSE (SWITCH ON)



DIP 16PIN OUTLINE DRAWING (DIP16-P-300-2.54A)

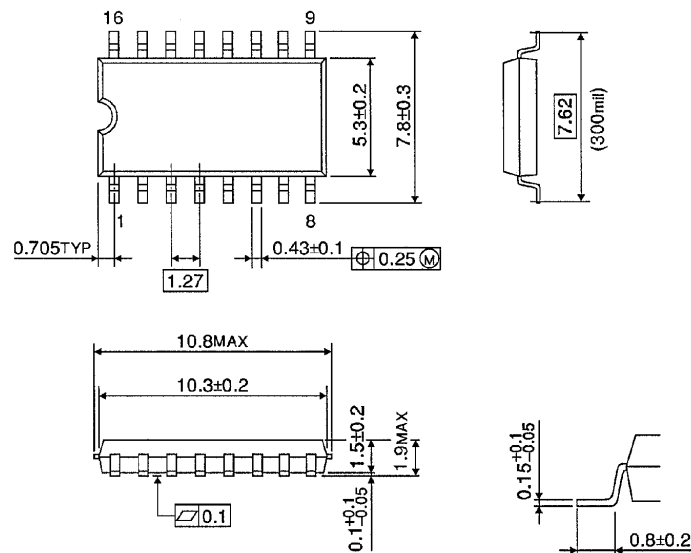
Unit in mm



Weight : 1.00g (Typ.)

SOP 16PIN (200mil BODY) OUTLINE DRAWING (SOP16-P-300-1.27)

Unit in mm

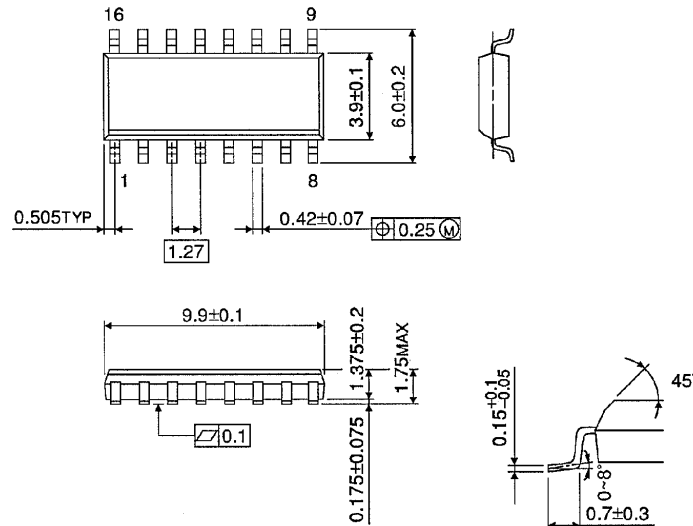


Weight : 0.18g (Typ.)

SOP 16PIN (150mil BODY) OUTLINE DRAWING (SOL16-P-150 -1.27)

Unit in mm

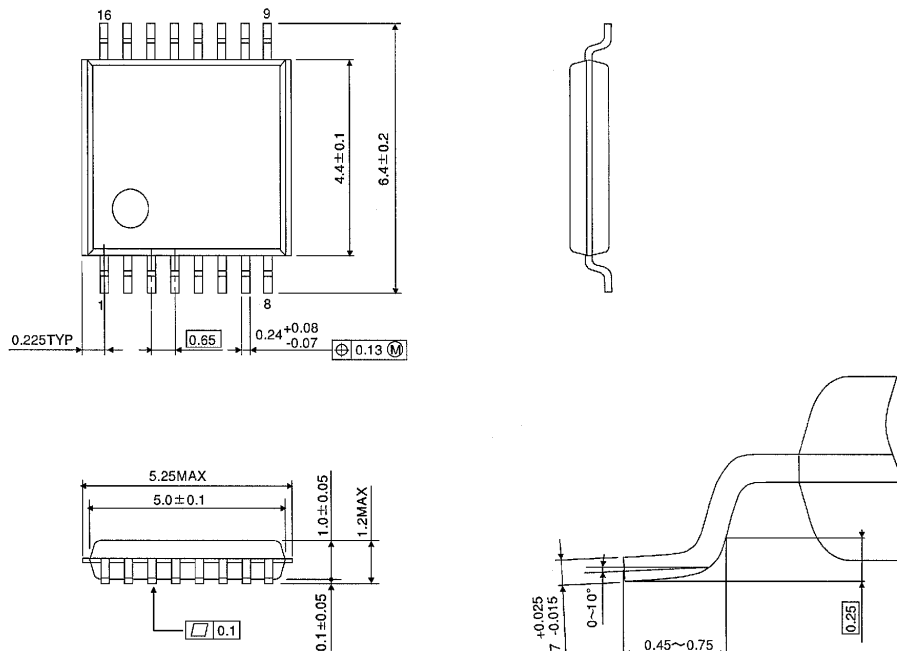
(Note) This package is not available in Japan.



Weight : 0.13g (Typ.)

TSSOP 16PIN OUTLINE DRAWING (TSSOP16-P-0044-0.65)

Unit in mm



Weight : 0.06g (Typ.)